Annex A:Operational Description of Circuitry

RULE PART NUMBER: 2.1033 (c)(10)

1 PURPOSE

This report has been prepared to support the application for FCC Certification Per Code Of Federal Regulations, Title 47, Parts 2 And 90 for the MCUA5R radio-modem comprised of the JDT Model 242-3422-xxx Transceiver and Dataradio 210-3315-xxx Modem. The report presents necessary information concerning electrical circuit description, measured performance and physical construction and configuration. Also parts 4 and 5 present active circuit devices functions for Transceiver and, accordingly, for Modem.

2 DL-3422 TRANSCEIVER

The main subassemblies of this transceiver are the RF board, VCO board, TCXO and modem assembly. A block diagram of the transceiver is located in Figure 2.

The VCO board is enclosed by a metal shield and soldered directly to the RF board. The VCO is not serviceable.

The DL-3422 has a reference oscillator stability of ±2.5 PPM. The TCXO (Temperature Compensated Crystal Oscillator) is soldered directly to the RF board. The TCXO is not serviceable.

2.1 SYNTHESIZER

The synthesizer output signal is produced by a VCO (voltage controlled oscillator). The VCO frequency is controlled by a DC voltage produced by the phase detector in U811. The phase detector senses the phase and frequency of the two input signals and causes the VCO control voltage to increase or decrease if they are not the same. The VCO is then "locked" on frequency.

Programming of the synthesizer provides the data necessary for the internal prescaler and counters. One input signal is the reference frequency. This frequency is produced by the reference oscillator (TCXO). The other input signal is the VCO frequency.

VOLTAGE-CONTROLLED OSCILLATOR

Oscillator (Q872)

The VCO is formed by Q872, several capacitors and varactor diodes, and air wound inductor L872. It oscillates at the transmit frequency in transmit mode and first injection frequency in the receive mode (132-174 MHz in transmit and 153.45 - 195.45 MHz in receive).

Biasing of Q872 is provided by R873, R874 and R876. An AC voltage divider formed by C872, C874 and C875 initiates and maintains oscillation and also matches Q872 to the tank circuit. air wound inductor L872 is grounded at one end to provide shunt inductance to the tank circuit.

Frequency Control and Modulation

The VCO frequency is controlled by a DC voltage across varactor diodes CR852, CR853, and CR854. As voltage across a reverse-biased varactor diode increases, its capacitance decreases. Therefore, VCO frequency increases as the control voltage increases. CR852/CR853 and CR854 are paralleled varactors to divide the capacitance and improve linearity. The varactors CR852/CR853 are biased at -

2.0V so the control line voltage can operate closer to ground. CR854 is pin shifted in when transmitting to increase the VCO gain in transmit. The control line is isolated from tank circuit RF by choke L852/L853. The amount of frequency change produced by CR852/CR853/CR854/ is controlled by series capacitor C854.

The -2.0V applied to the VCO is derived from the 14.85 MHz TCXO frequency that is amplified by Q902, rectified by CR902 and filtered by C912, C917, C918 and C920 on the RF board.

The VCO frequency is modulated using a similar method. The transmit audio/data signal from J201, pin 6 is applied across varactor diode CR861 which varies the VCO frequency at an audio rate. Series capacitors C855/C856 set the amount of deviation produced along with CR862 and C865. R863 provides a DC ground on the anodes of CR861/CR862, and isolation is provided by R862, and C863.

The DC voltage across CR862 provides compensation to keep modulation relatively flat over the entire bandwidth of the VCO. This compensation is required because modulation tends to increase as the VCO frequency gets higher (capacitance of CR852/CR853/CR855 gets lower). CR862 also balances the modulation signals applied to the VCO and TCXO. The D/A Converter U911 can be programmed to apply a compensating voltage to CR862 to adjust the modulation sensitivity between the TCXO and VCO.

The DC voltage applied across CR862 comes from the modulation adjust control R827 on the RF board. R826 applies a DC biasing voltage to CR86. C821 provides DC blocking. RF isolation is provided by C865, and R862.

VCO AND REFERENCE OSCILLATOR MODULATION

Both the VCO and reference oscillator (TCXO) are modulated in order to achieve the required frequency response. If only the VCO was modulated, the phase detector in U811 would sense the frequency change and increase or decrease the VCO control voltage to counteract the change (especially at the lower audio frequencies). If only the reference oscillator frequency is modulated, the VCO frequency would not change fast enough (especially at the higher audio frequencies). Modulating both VCO and reference oscillators produces a flat audio response. Potentiometer R827 sets the VCO modulation sensitivity so that it is equal to the reference oscillator modulation sensitivity.

CASCADE AMPLIFIERS/VCO (Q871/Q872)

The output signal on the collector of Q871 is coupled to buffer amplifier Q872 which forms a cascade amplifier. This is a shared-bias amplifier which provides oscillation, amplification and isolation from the stages which follow. The signal is coupled and matched from the collector of Q872 through inductors and capacitors and a T-pad to amplifier Q882.

AMPLIFIER (Q882)

Q882 provides final amplification of the VCO signal. Biasing of Q882 is provided by Q881 and several resistors. Matching to the transmitter and receive first injection is provided by L891 and C892. A 6dB T-pad is used to isolate the transmitter and receive first injection.

VOLTAGE FILTER (Q901)

Q901 on the RF board is a capacitance multiplier to provide filtering of the 8.6V supply to the VCO. R901 provides transistor bias and C901 provides the capacitance that is multiplied. If a noise pulse or other voltage change appears on the collector, the base voltage does not change significantly because of C901. Therefore, base current does not change and transistor current remains constant. CR901 decreases the charge time of C901 when power is turned on. This shortens the startup time of the VCO. C902, and C903 are RF decoupling capacitors.

VCO FREQUENCY SHIFT (Q841)

The VCO must be capable of producing frequencies from 132 - 195.45 MHz to produce the required receive injection and transmit frequencies.
If this large of a shift was achieved by varying the VCO control voltage, the VCO gain would be undesirably high. Therefore, capacitance is switched in and out of the tank circuit to provide a coarse shift in frequency.

This switching is controlled by the T/R pin shift (RX_EN) on J201, pin 4, Q841/Q842 and pin diode CR851. When a pin diode is forward biased, it presents a vary low impedance to RF; and when it is reverse biased, it presents a very high impedance. The capacitive leg is switched in when in transmit and out when in receive.

When J201, pin 4 is high in receive (+5V), Q173 is turned on and the collector voltage goes low. A low on the base of Q172 turns the transistor on and the regulated +9.6V on the emitter is on the collector for the receive circuitry. Q171 applies a low on the base of Q841 the transistor is off and the collector is high. With a high on the base of Q842 and a low on the emitter, this reverse biases CR850 for a high impedance.

The capacitive leg on the VCO is formed by C852, CR851, and C853. When J201, pin 4 is low in transmit, Q842 is turned on and a high is on the emitter, Q171 is turned off and the collector voltage goes high. A low on the base of Q173 turns the transistor off and the regulated +9.6V is removed from the receive circuitry. With a high on the base of Q841 the transistor is on and the collector is low. With a low on the base of Q842 and a high on the emitter, this forward biases CR851 and provides an RF ground through C852 and C853 is effectively connected to the tank circuit. This decreases the resonant frequency of the tank circuit.

2.2 SYNTHESIZER INTEGRATED CIRCUIT (U811)

Introduction

This device contains the following circuits: R (reference), Fractional-N, NM1 and NM2; phase and lock detectors, prescaler and counter programming circuitry. Refer to Figure 1 for Synthesizer IC block diagram.

Channel Programming

Frequencies are selected by programming the R, Fractional-N, NM1 and NM2 in U811 to divide by a certain number. These counters are programmed by Loader board or a user supplied programming circuit.

As previously stated, the counter divide numbers are chosen so that when the VCO is oscillating on the correct frequency, the VCO-derived input to the phase detector is the same frequency as the reference oscillator-derived frequency.

The VCO frequency is divided by the internal prescaler and the main divider to produce the input to the phase detector.

LOCK DETECT

When the synthesizer is locked on frequency, the SYNTH LOCK output of U811, pin 18 (J201, pin 7) is a high voltage. Then when the synthesizer is unlocked, the output is a low voltage. Lock is defined as a phase difference of less than 1 cycle of the TCXO.

2.3 RECEIVER CIRCUIT DESCRIPTION

PRESELECTOR FILTER, RF AMPLIFIER (Q202)

Capacitor C201 couples the receive signal from the antenna switch to the LC preselector filter composed of L201, L202, L203, CR281, CR282, C202, C203, C204, C205, C206, and C207. (The antenna switch is described in later.) The preselector filter is a two pole discrete LC varactor tuned bandpass filter adjusted to pass only a narrow band of frequencies to the receiver. This attenuates the image and other unwanted spurious frequencies. The preselector filter is tuned in frequency by varying the reverse bias voltage of the varactors CR 281 and CR 282. The filter control voltage is generated by Digital to Analog Converter (DAC) U911 and amplified by U831 to generate a higher voltage swing to the varactors and minimize filter loss. R206 and capacitors C281 through C285 filter the varactor voltage and provide RF isolation.

Impedance matching between the preselector filter and RF amplifier Q202 is provided by C207 and L204. CR201 protects the base-emitter junction of Q202 from excessive negative voltages that may occur during high signal conditions. Q201 is a switched constant current source which provides a base bias for Q202. Q201 base bias is provided by R202/R203. Current flows through R201 so that the voltage across it equals the voltage across R202 (minus the base/emitter drop of Q201). In the transmit mode the receive +9.6V is removed and Q201 is off. This removes the bias from Q202 and disables the RF amplifier in transmit mode. This prevents noise and RF from being amplified by Q202 and fed back on the first injection line.

Additional filtering of the receive signal is provided by a three pole discrete LC varactor tuned bandpass filter composed of filter L212, L213, L214, L221, L222, L223, L224, CR283, CR284, CR285, C214, C215, C216, C217, C221, C222, and C223. L211 and C213 provide impedance matching between Q202 and this filter. Resistor R205 is used to lower the Q of L211 to make it less frequency selective. The same control voltage that adjusts to two pole filter on frequency adjusts this filter as well. The inductors are factory tuned to align the filter tracking and should not be adjusted.

MIXER (Q232)

First mixer Q232 mixes the receive frequency with the first injection frequency to produce the 21.45 MHz first IF. Since high-side injection is used, the injection frequency is 21.45 MHz above the receive frequency. Q231 biases Q 232 in similar fashion to Q201 described above. The RF signal is coupled to the mixer through C233. R226 attenuates high voltage excursions on the base of Q232. The LO injection is proved across L232 and R236 on the emitter of Q232. Emitter injection is used to provide isolation between the LO port and the RF port. L233 and C238 provide a low impedance on the emitter at the IF frequency improving noise performance and conversion gain.

FIRST L.O. AMPLIFIER/BUFFER (Q301, Q302)

The first L.O. amplifier provides amplification and buffering of the receive first injection. R305, R306, and R307 form a 3dB 50 ohm pad C303 couples the signal to C304 and L301 which match Q302 to 50 ohms L302 and C307 match Q302 to the mixer Q232. Q301, R301, R302, R303, and R304 provide biasing for Q302 R308 enhances the stability of Q302. C302 and C306 provide RF decoupling.

CRYSTAL FILTER (Z231/Z232)

The output of Q232 is matched to the crystal filter, Z231 and Z232 by L231, C234, and C237. This filter presents a low impedance to 21.45 MHz and attenuates the receive, injection, and other frequencies outside the 21.45 MHz passband.

Z221 and Z222 form a 2-section, 4-pole crystal filter with a center frequency of 21.45 MHz and a -3 dB passband of 8 kHz (12.5 kHz BW) or 15 kHz (25 kHz BW). This filter establishes the receiver selectivity by attenuating the adjacent channel and other signals close to the receive frequency. C241 and C242 adjust the coupling of the filter. L242, C244, C245 and R243 provide impedance matching between the filter and 241.

SECOND LO OSCILLATOR (U241), BUFFER (Q251)

The second LO oscillator is built into U241 which provides the base and emitter connections for an internal oscillator transistor. The oscillator tank circuit consists of L251, C253, and CR251. Oscillator feedback is provided by C254, C256 and C257. The oscillator frequency is adjusted by applying a control voltage across R253 to CR251. The control voltage is provided by the charge pump of the auxiliary synthesizer in U811. The emitter of the oscillator transistor is connected to the common collector buffer amplifier Q251 by C251. R257, R258, R259 and R254 provided bias for Q251. R254 additionally provides an RF load to decrease the buffer level. C258, C259, and L252 filter the unwanted harmonics from the oscillator output. The output of Q251 is coupled to the auxiliary synthesizer phase detector by C814. The oscillator is phase locked at 21.9 MHz with L251 adjusted to center the control voltage.

SECOND MIXER/DETECTOR (U241)

Oscillator and Mixer

U241 contains the second oscillator, second mixer, limiter, detector, and squelch circuitry. The 21.45 MHz IF signal is mixed with a 21.9 MHz signal produced by second LO amplifier Q401 from TCXO Y801.

Second IF Filter

The output of the internal double-balanced mixer is the difference between 21.45 MHz and 21.9 MHz which is 450 kHz. This 450 kHz signal is fed out on pin 3 and applied to second IF filters Z241 and Z242. These filters have passbands of 9 kHz (12.5 kHz BW), or 20 kHz (25 kHz BW) at the -6 dB points and are
used to attenuate wideband noise.

Limiter-Amplifier

The output of Z241/Z242 is applied to a limiter-amplifier circuit in U241. This circuit amplifies the 450 kHz signal and any noise present; then limits this signal to a specific value. When the 450 kHz signal level is high, noise pulses tend to get clipped off by the limiter; however, when the 450 kHz signal level is low, the noise passes through the limiter. C275/C276 decouple the 450 kHz signal.

Quadrature Detector

From the limiter stage the signal is fed to the quadrature detector. An external phase-shift network connected to pin 8 shifts the phase of one of the detector inputs 90× at 450 kHz (all other inputs are unshifted in phase). When modulation occurs, the frequency of the IF signal changes at an audio rate as does the phase of the shifted input. The detector, which has no output with a 90× phase shift, converts this phase shift into an audio signal. L253 is tuned to provide maximum undistorted output from the detector. R255 is used to lower the Q of L253. From the detector the audio and data signal is fed out on pin 9. The audio/data output of U241, pin 9 is applied to J201, pin 13.

Receive Signal Strength Indicator (RSSI)

U241, pin 5 is an output for the RSSI circuit which provides a current proportional to the strength of the 450 kHz IF signal. The voltage developed across R275 is applied to J201, pin 12.

2.4 TRANSMITTER CIRCUIT DESCRIPTION

BUFFER (Q501)

The VCO RF output signal is applied to R892, R893 and R894 that form a resistive splitter for the receive first local oscillator and the transmitter. The VCO signal is then applied to a 50 ohm pad formed by R501, R502, and R503. This pad provides attenuation and isolation. Q501 provides amplification and additional isolation between the VCO and transmitter. Biasing for this stage is provided by R504 and R505, and decoupling of RF signals is provided by C503 . Impedance matching to the predriver is provided by L511 and C512.

PRE-DRIVER (Q511)

Pre-driver Q511 is biased class A by R511 and R512 and R515. L513, Q517 and C518 match Q511 to U531. R514 provides a resistive feedback path to stabilize Q511 and C515 provides DC blocking. C516 bypasses RF from the DC line, and R513 provides supply voltage isolation and ties the +9V transmit supply to the circuit.

FINAL (U531), COMPARATOR (U111C)

RF module U531 has an RF output of 1 to 5W and operates on an input voltage from 10-16V.

Power control is provided by U581, U111, Q531 and a stripline directional coupler. The power is adjust by Power Set Control R535 that provides a reference voltage to U111C. U111C drives Q531 and PA module U531.

One end of the balun directional coupler is connected to a forward RF peak detector formed by R591, CR591, C591 and U581A. The other end of the stripline directional coupler is connected to a reverse RF peak detector formed by R593, CR592, C593 and U581B.

If the power output of U531 decreases due to temperature variations, etc., the forward peak detector voltage drops. This detector voltage drop is buffered by U581A and applied to inverting amplifier U111C which increases the forward bias on Q531. The increase on Q531 increases the power output level of U531. If the power output of U531 increases, the forward peak detector voltage increases and U111C decreases the forward bias on Q531. The decrease on Q531 decreases the output power of U531.

The output of CR591 and CR592 are fed to U581A/B respectively. If the output of either buffer increases, the increase is applied to the inverting input of U111C. The output of U111C then decreases and Q531 decreases the input voltage to U531 to lower the power. The control voltage is isolated from RF by ferrite bead EP532 and C531 decouples RF.

The forward/reverse power voltages from U581A/B are also applied to U913/U912 for diagnostics outputs on J201.

The low-pass filter consists of L551, C552, L552, C553, L553, C555, L554 and C856. The filter attenuates spurious frequencies occurring above the transmit frequency band. The transmit signal is then fed through the antenna switch to antenna jack J501.

ANTENNA SWITCH (CR561, CR562)

The antenna switching circuit switches the antenna to the receiver in the receive mode and the transmitter in the transmit mode.
In the transmit mode, +9V is applied to L555 and current flows through diode CR561, L561, diode CR562, and R561. When a diode is forward biased, it presents a low impedance to the RF signal;

conversely, when it is reverse biased (or not conducting), it presents a high impedance (small capacitance). Therefore, when CR561 is forward biased, the transmit signal has a low-impedance path to the antenna through coupling capacitor C562.

L561, and C564 form a discrete quarter- wave line. When CR561 is forward biased, this quarter-wave line is effectively AC grounded on one end by C564. When a quarter-wave line is grounded on one end, the other end presents a high impedance to the quarter-wave frequency. This blocks the transmit signal from the receiver. C561 and C563 matches the antenna to 50 ohms in transmit and receive.

TRANSMITTER KEY-UP CONTROL

Q121, Q122, and Q123 act as switches which turn on with the RX_EN line. When the line goes low the Q121 is turned of which turns Q122 on turning Q123 on. This applies 13.6V to U111 before the TX_EN line goes high. U111A/B provides the key-up and key-down conditioning circuit. C116 and R117 provide a ramp up and ramp down of the 9.0TX during key-up and key-down which reduces load pull of the VCO during key-up. The conditioning provides a stable 5.5V output by balancing the 5.5V reference with the 5.5V regulated supply. The output on U111B, pin 7 is applied to comparator U111D, pin 12, the non-inverting input. The output of U111D, pin 14 is applied to the base of current source Q124. The output of Q124 is on the emitter and is applied back to the inverting input of comparator U111D, pin 13. A decrease or increase at U111D, pin 13 causes a correction by U111D to stabilize the 9V transmit output. R125/R126 establish the reference voltage on U111D, pin 13. C123 provides RF bypass, C124 provides RF decoupling and C125 stabilizes the output. The 9V transmit voltage is then distributed to the circuits.

2.5 VOLTAGE REGULATORS

+9.6V REGULATED

The 5V applied on J201, pin 5 is applied to the base of Q131 turning the transistor on. This causes the collector to go low and applies a low to the control line of U141, pin 1 and R131 is a pull up resistor. The 13.6V from J201, pin 2 is on U141, pin 6 to produce a +9.6V reference output on U141, pin 4. C145 stabilizes the voltage and C146 provides RF decoupling. C144 provides RF bypass and C118 provides RF decoupling. C137 provides is a bypass capacitor for U131.

+5.5 REGULATED

When 5.0V is applied to J201, pin 5 it is applied to the base of Q131 turning the transistor on. This causes the collector to go low and applies a low to the control line of U131, pin 1. C136 decouples RF and R131 is a pull up resistor. The 13.6V from J201, pin 2 is on U131, pin 6 to produce a +5.5V regulated output on U131, pin 4. C135 stabilizes the voltage and C136 provides RF decoupling. C137 provides is a bypass capacitor for U131.

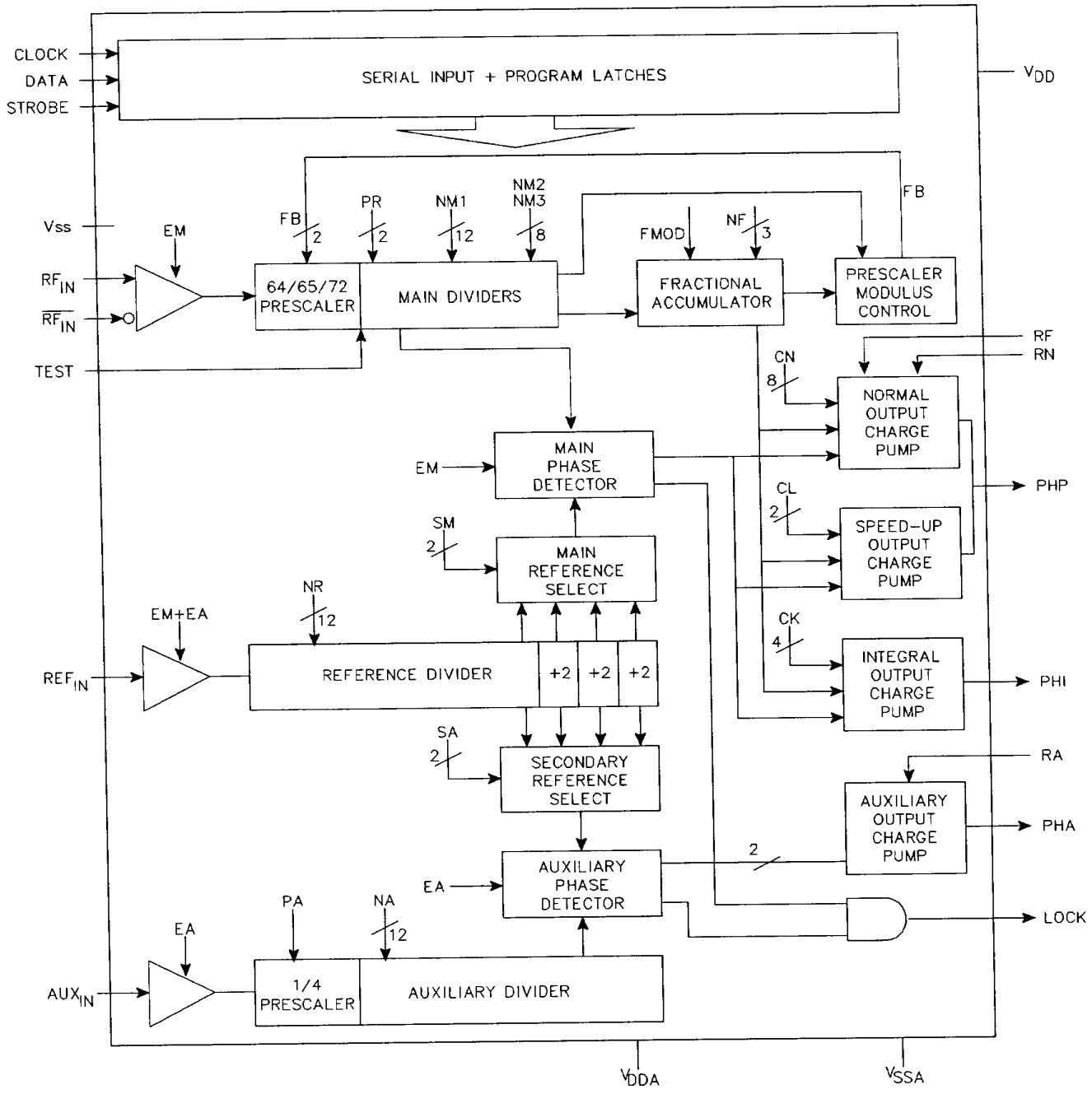


Figure 1: DL-3422 SYNTHESIZER INTEGRATED CIRCUIT (U811)

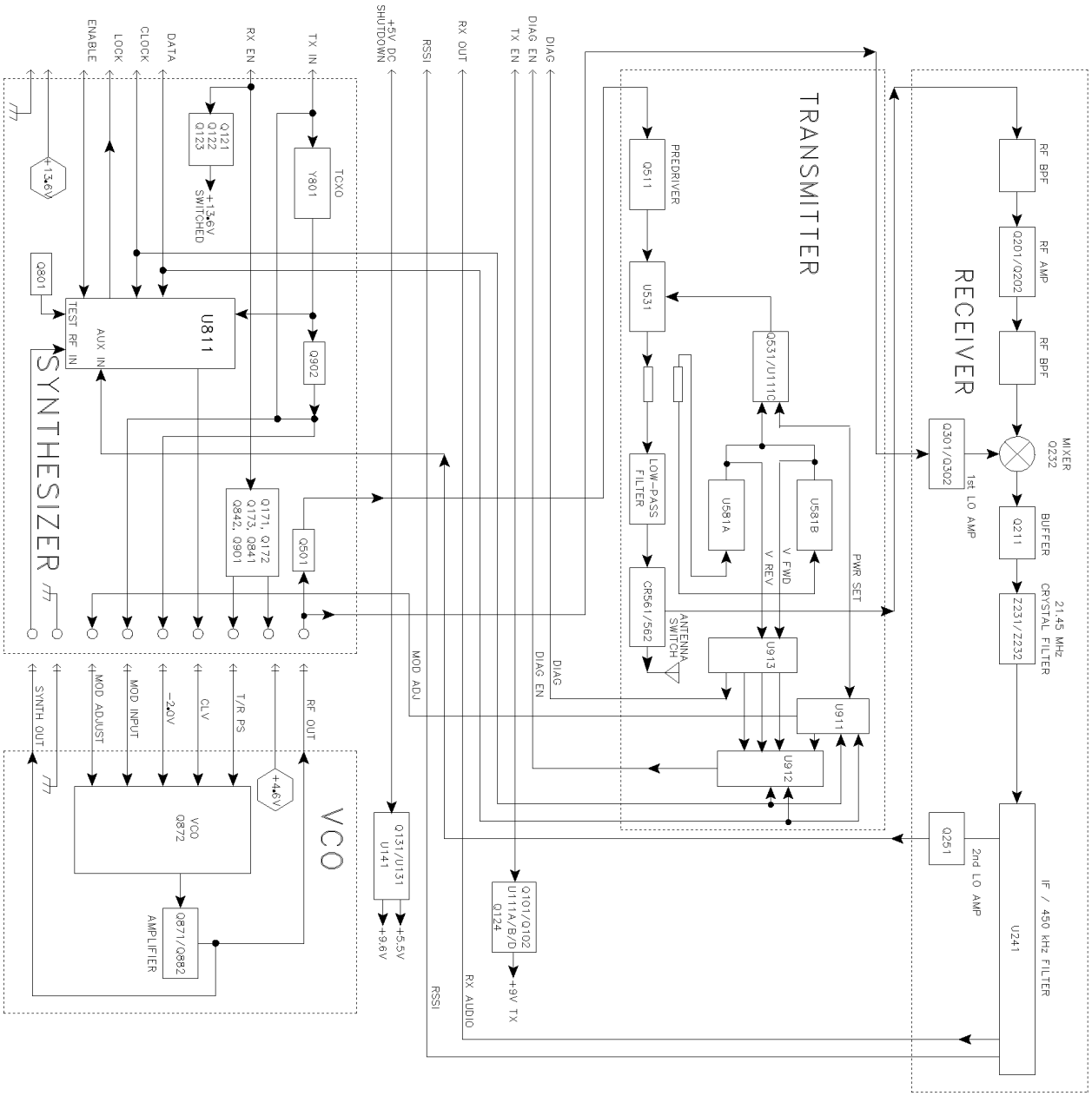


Figure 2: DL-3422 TRANSCEIVER BLOCK DIAGRAM

3. INTEGRA R- 3315 LOADER/MODEM

The Logic Board is divided into 6 sub-sections on the Block Diagram

1 CPU
2 RS232
3 Modem
4 Integra-T A/D and Digipot
5 Wake-Up Circuit
6 PSU

A block diagram of the MCU-R is located at the end of this section.

3.1MICROPROCESSOR CIRCUIT

For the microprocessor section, two Z84015 CMOS low power Intelligent Peripheral Controllers are used. Each IPC is an 8-bit microprocessor integrated with CTC, SIO, PIO Clock Generator Controller and Watch Dog Timer.
One of the Z84015s (U17) is used in the normal mode. The other Z84015 (U21) is used in the evaluation mode and as such only the CTC, SIO and PIO section are used. The CPU section is disabled.
The first Z84015 Clock Generator uses a 19.6608 MHz crystal which provides a CPU clock rate of 9.8304 MHz for both Z84015s. The 9.8304 MHz clock is further divided by 2 to feed all 8 CTC (4 in each Z84015).

The 64K memory space of the Z84015 is divided into two blocks of 32k each. The lower 32K is used for the firmware program and the upper 32K by the CMOS RAM (U18).). The memory IC used for the program is a CMOS FLASH (U22) with 1024 sectors of 128 bytes each.

The dual Z84015 circuit provides up to 8 CTC, 4 SIO (Serial I/O) and 32 PIO (Parallel Input/Output) lines.
The CPU also provides the clock for the CPLD modem.

3.2RS232

The RS232 IC (U15) is used to interface the application DE-9 connector to the SIO_B section of U17, and the set-up DE-9 connector to the SIO_A section of U21. When in sleep mode, two receivers remain enabled, this is needed for fast wakeup.

3.3MODEM

The modem section is used to interface the serial digital data to the transceiver.
The CPLD modem IC (U16) with a programmable Raise-Cosine filter (U10), operates in DRCMSK mode at 4800, 9600 and 19200 bits/sec. It incorporates a 7-bit hardware scrambler and uses Differential (NRZI) encoding in DRCMSK mode to minimize data pattern-sensitivity. Electronic potentiometer U5B (E-Pot), controlled by CPU U17, is used to set the transmitter deviation by amplitude adjustment of the baseband signal. Electronic potentiometer U5C is also provided to adjust the frequency of the RF carrier.

TRANSMIT & RECEIVE DATA

Transmit Data from the RS-232 port is level-shifted to TTL by U15, then passed through the CPU for further processing and conversion from asynchronous to synchronous format. The CPLD modem, U16 takes the digital data stream from SIO-A of the CPU and synthesizes to the constant-amplitude analog baseband signal, which is filtered by U10, buffered by U9B then applied to radio module TXA at P1-6.

Received signals are applied to the RXA pin on P1-13 amplified by U3A, whose gain is set by the electronic potentiometer U5D, and then filtered by U10. The same filter circuit is used for transmission and reception: two analog multiplexer/demultiplexer gates (U8A and B) controlled by TX_EN line are used for sharing. The filter U10 cut-off frequency is programmable by the CPLD, based on the data rate. The analog signal is then buffered by U1D and fed to Peak Detectors U3C, U3D and U3B, and to the slicer circuit U1C via U1B. The raw data is then passed to the CPLD modem U16 for descrambling and receive clock recovery. The resulting synchronous bit stream is then fed to CPU, SIO-A for further processing and convertion to asynchronous format before delivery to the RS-232 driver and to the user port.

3.4INTEGRA-T A/D AND DIGIPOT

An 8 channel, 8-bit successive approximation A/D converter, type ADC0838 (U4), is interfaced to CPU (U17) and Peripheral (U21).
CH0 and CH1 are connected to the positive and negative peak detector of the modem section. The software can thus read the positive or negative value of an RX signal, or using the differential mode, the actual peak-to-peak RX signal value.
CH3 is used to measure the radio RSSI signal which was amplified by U7A.
CH4 is connected to the radio diagnostic signal (P3-14). This pin is used to output an analog signal corresponding to the power output and the reflected signal.
CH5 is connected to U6 (LM50), a temperature sensor with a -40 to +125°C range.
CH6 is used to read the SWB+ voltage after proper scaling into the 0-5 V range.
CH7 and CH8 are connected to EXT SIGNAL 1 and 2. A 2:1 divider and protection circuit is inserted between both external signals and the A/D.
The EXTERNAL SIGNAL 1 and 2 pins are also connected to U21 at PB6 and PB7 through transistors Q3 and Q4, and thus can be used for ANALOG INPUT or DIGITAL OUTPUT (available on some Integra versions).
EXT_SIGNAL2 is also connected to the rx test point RX-TP through U8A (74HC4066). Under software control the RX-TP (scaled down by 2) is thus available on the power connector for trouble-shooting purposes.
A 4 channel digital potentiometer type (U5) is used to adjust the RX SIGNAL, TX MODULATION, CARRIER FREQUENCY and CARRIER DETECT THRESHOLD.
An 8 channel, 8-bit successive approximation A/D converter, type AD0838 (U9), is interfaced to CPU (U18) and Peripheral (U20).
U19 generates a power-on reset for the CPU and U6 is a temperature sensor used by the firmware to compensate for variations in RSSI.

The RSSI signal from the transceiver is amplified and filtered by U7A, it is then compared to a threshold value set by a digital potentiometer (U5A). The output of the comparator (U7B) is used to change the hold time of both peak detectors at the beginning of the receive packet.

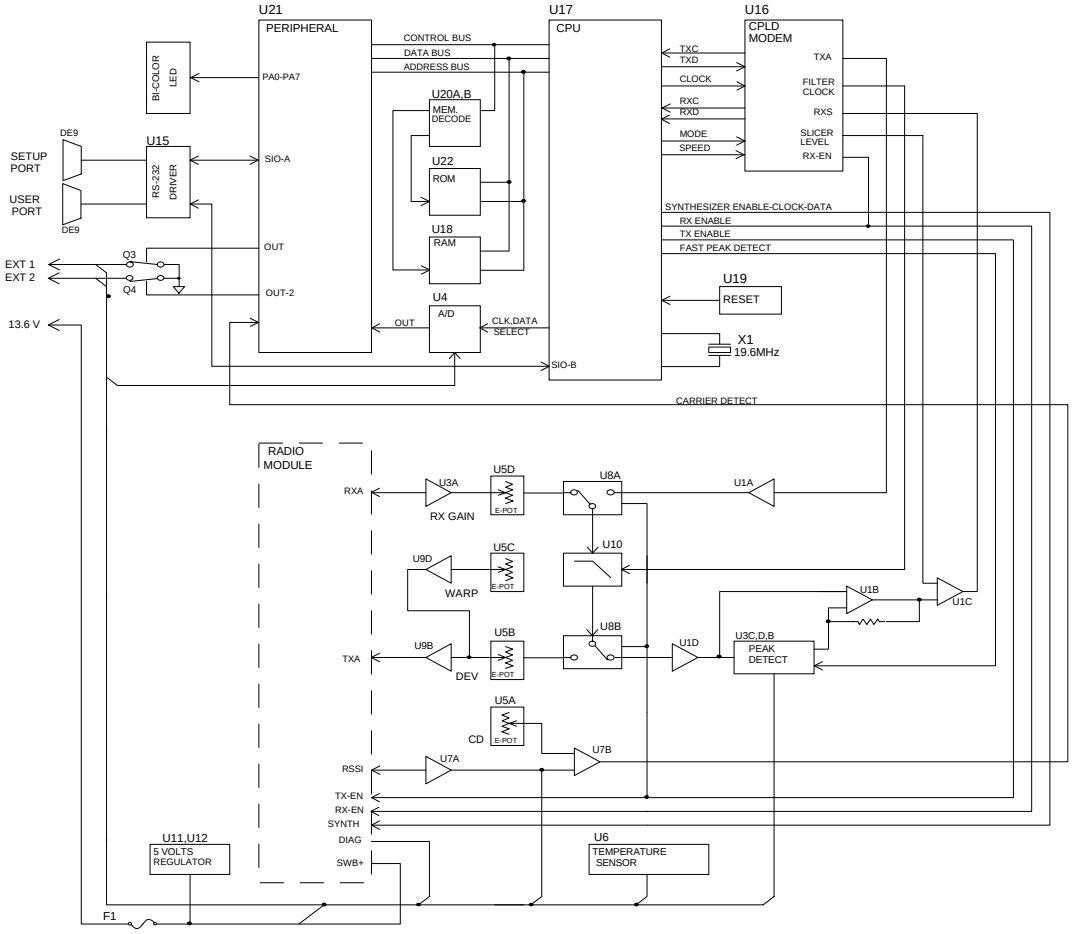
3.5WAKE-UP CIRCUIT

The wake-up circuit for Integra-T consists of a 50 ms monostable circuit that is triggered by the rising edge of a SLEEP signal from the CPU (U18). The falling edge of this 50 ms pulse (end of pulse) is connected to the \NMI of the CPU and thus will wake up the CPU from SLEEP mode after 50 ms.
When exiting SLEEP mode on a \NMI, the CPU firmware will increment a counter, then return to SLEEP until it reaches a limit set by a software parameter. When the programmed count is reached the CPU will wake up the radio and the RS232 driver, program the synthesizer, and watch for channel activity.
While in sleep mode (during the 50 ms pulse) an active RTS from either communication port will reset (terminate) the 50 ms pulse so that its falling edge will restart the CPU immediately.
The CPU will check to see if either RTS signal is valid each time it is restarted by the \NMI. The firmware will only start the sleep timer after checking that all "wakeup" inputs are inactive.

3.6POWER SUPPLY

The 13.3 volt DC power input is protected by a 3 amp fuse and reverse protected by a diode.
A 5 volt, low voltage regulator (U12) is used to power all digital functions and another 5 volt, low voltage regulator is used to control the analog +5V_SW voltage in the sleep mode.

Block diagram



4. DL-3422 ACTIVE CIRCUITS DESCRIPTION

Designator	Function	JEDEC or Vendor Type
CR561	Antenna switch	MMBV3401
CR562	Antenna switch	MMBV3401
CR591	Directional coupler	MMBD701LT
CR592	Directional coupler	MMBD701LT
CR851	Pin shift diode	MMBV3401
CR852	Rectifier	MMBV609
CR853	Rectifier	MMBV609
CR861	Varactor	BB535E7908
CR862	Varactor	BB535E7908
CR901	Varactor	BB535E7908
CR902	Rectifier	BAV99LT1
Q101	Tx enable	MUN5213T1
Q102	Tx enable	MUN2114T1
Q121	Rx enable	MUN5213T1
Q122	Rx enable	MUN5213T1
Q123	Rx enable	MUN2114T1
Q124	Soft key up control	PZT2222AT1
Q131	5 volt shutdown	MUN5213T1
Q171	Pin shift	MUN5213T1
Q172	Pin shift	MUN2114T1
Q501	RF buffer	MSA-2111
Q511	RF driver	NE85633
Q531	Power control	PZT2222AT1
Q801	Constant voltage source	MSD1819A-RT1
Q841	Pin shift	MUN5213T1
Q842	Pin shift	MUN2114T1
Q871	VCO buffer	NE85619-T1
Q872	Oscillator	NE85619-T1
Q881	Bias regulator	MSB1218A-AT1
Q882	Amplifier	NE85633
Q901	Capacitance multiplier	MSD1819A-RT1
Q902	Amplifier	MMBT918LT1
U111A	Soft key up control	LMC660AMI
U111B	Soft key up control	LMC660AMI
U111C	Power control	LMC660AMI
U111D	Soft key up control	LMC660AMI
U131	Voltage regulator	TK11900MTL
U141	Voltage regulator	TK11900MTL
U531	RF power module	M57732
U581A	V-fwd amp	MC33172DT
U581B	V-rev amp	MC33172DT
U811	Synthesizer	SA7025DK-T
Y801	TCXO	14.85 / 17.5 MHz

5.INTEGRA R 210-3315-XXX ACTIVE CIRCUITS DESCRIPTION

Designator	function	Type
D1	DIODE, HOT CARRIER, SOT-23	MMBD301LT1
D2	DIODE, HOT CARRIER, SOT-23	MMBD301LT1
D3	DIODE, SOT-23	BAV99LT1
D4	DIODE, SOT-23	BAV99LT1
D5	DIODE, SOT-23	BAV99LT1
D6	DIODE,RECTF,1A/100V	1N4001
DS1	LED,3MM,BICOLOR,RED/GREEN SMT	591-3001-102
DS2	LED,3MM,BICOLOR,RED/GREEN SMT	591-3001-102
DS3	LED,3MM,BICOLOR,RED/GREEN SMT	591-3001-102
DS4	LED,3MM,BICOLOR,RED/GREEN SMT	591-3001-102
Q1	TRANSISTOR, GENERAL PURPOSE,SOT-23	MMBT3904LT1
Q2	TRANSISTOR, GENERAL PURPOSE,SOT-23	MMBT3904LT1
Q3	TRANSISTOR, GENERAL PURPOSE,SOT-23	MMBT3904LT1
Q4	TRANSISTOR, GENERAL PURPOSE,SOT-23	MMBT3904LT1
U1	QUAD, OP-AMP , -40/+85 SO-14	TLC2274ID
U2	HEX INVERTER CMOS	74HC04AD
U3	QUAD OP-AMP	LMC6484AIM
U4	8 BIT A/D,-40/+85C SO-20W	ADC0838CIWM
U5	POTENTIOMETER 4 DIGITAL	AD8403AR50
U6	TEMPERATURE SENSOR,SOT-23	LM50CIM3
U7	DUAL OP-AMP,-40/+85 S0-8	TLC2272ID
U8	ANALOG MULTIPLEXERS/ DEMULTIPLEXERS SOIC 16	MC74HC4053D
U9	QUAD, OP-AMP , -40/+85 SO-14	TLC2274ID
U10	FILTER, LINEAR PHASE LOW PASS S0-8	LTC1069-7
U11	REGULATOR,MICROPOWER VOLTAGE ,S0-8	LP2951CD
U12	REGULATOR,LOW DROPOUT,Q PACKAGE	LT1129IQ-5
U13	DUAL MONOSTABLE, SOIC	74HC4538AD
U14	QUAD NAND GATE	74HC00AD
U15	CONVERTER RS-232	ADM223AR
U16 (TO BE PROGRAMMED)	CPLD 64 MACROCELL	PZ5064-I12A44
U17	MICROPROCESSOR ,10MHz	Z8401510FEC
U18	RAM,CMOS,32K x 8, -40/=85, SOP-28	TC55257DFI-85L or TC55257DFL-85L (SCREENED -40 +85)
U19	RESET CIRCUIT, -40+85 ,S0-8	MC33064D-5
U20	HEX OR GATE,CMOS	74VHC32AD
U21	MICROPROCESSOR ,10MHz	Z84C1510FEC /Z8401510FEC
U22 (TO BE PROGRAMMED)	EPROM, FLASH 1 MEGABIT, -40/+85 PLCC	AT29C010A-90J1
X1	XTAL, FPX SERIES 19.6608 MHz	FPX196-20PF