Annex B

DESCRIPTION OF CIRCUITRY

RULE PART NUMBER: 2.1033 (c)(10)

Table of contents

Paragon/PD D212 BDLC will become the modulation source for the T881 Exciter module after all changes described here are applied. A brief functional description of the Base Data Link Controller (BDLC) is provided in the Paragon/PD technical manual, Annex A of this report. If a more detailed description of the modulation source along with the block diagram and the active part list are requested, they will be the object of another appendix.

1.Changes undergone by T881

1.1. Class II type Permissive changes - T881 series II 800 MHz Exciter

By-pass the Audio Processor (up to and including the low-pass filtering)

The resistor R 291 which connects the output of the audio low-pass filter (IC260) to the input of the buffer toward the splitter between the input of the VCO (R293, IC260) and the Modulator reference (R296, IC 220 EPOT) has been removed. Its output pad has been connected to the TXA signal through a soldered wire.

The TxA signal has been brought in using CTCSS input (pin 8) whose line has been disconnected from original PCB removing R259 and C265 and extended via a soldered wire up to the pad mentioned before. All the steps are detailed appropriately in the production procedure nr. 164-20006-051, which is provided as Annex C.

Changes in Active parts list

None.

All the removals undergo passive parts.

1.2.Class I type Permissive changes

Addition of a flash ROM (EEPROM) memory module block powered from T881 9V power supply line. In order to provide room on the board the line match potcore T4030 and C 201 were removed.

The memory module records settings related to the module for which values are found through calibration during production procedures. They concern reference level and deviation level settings to adjust the modulation and the frequency drift.

The board 030-03375-001 hosts the memory chip U1 (DS2433) and a line signal booster circuitry (Q1, CR1, CR2, R1 and C1) which corrects edge timings for data I/O signals for proper read/write/enable r/w commands. Although U1 is self powered from I/O line, the signal conditioner uses 9V line provided by T881.

Changes in Active parts list

Active parts added with the board 03375 (Memory module)

Reference designator	Function	Type
CR1	Diode, transient suppressor	1N4148
CR2	Diode, Zener, transient suppressor	1N4133AT
Q1	Voltage regulator	MC78L05ABP
U1	serial 1024 bits EEPROM	DS2433

2. Original Circuit description of Audio Processor Block form T881 service manual

T881 Circuit Operation. In the service manual the corresponding part is 2.5. The circuitry of sections 2.5.1, 2.5.2, 2.5.4 and the first paragraph of 2.5.5 have been functionally replaced by the DSP via the modifications described earlier. The sections (marked *) 2.5.3 and last two paragraphs of 2.5.5 still apply.

2.5 AUDIO PROCESSOR

2.5.1 GENERAL

The audio processor comprises several link selectable circuit blocks, which may be configured in a variety of combinations to suit individual requirements. The pre-emphasis network and compressor may be linked individually or cascaded between either or both audio inputs and the limiter.

Refer to Section 3.5.1 for linking details.

2.5.2 AUDIO INPUTS

Two audio inputs are available: one from a 600 ohm balanced (or unbalanced) line, and the other from a local microphone. The microphone signal is passed first to a pre-amplifier (Q210) and ultimately to a multiplexer (IC 1240), but in between may pass through the compressor (depending on the linking details). The line transformer is also connected to the multiplexer and is disabled by the microphone PTT switch.

A third input for CTCSS tones is also provided.

(*)2.5.3 KEYING INPUTS

There are four ways to key the exciter:

1. Pull the Tx-key line low (pin 13 on the D-range 1 [PL100]) at the rear of the set);
2. Push the “Carrier” button on the front panel - this will inhibit all audio;
3. Use the PTT button on the local microphone, which disables audio from the line;
4. Via the opto-key inputs (pins 11 and 12 on the D-range 1[PL100]) where electrical isolation is required.

This features a constant current sink (Q270) to ensure reliable activation of the opto-coupler (IC250) at low keying voltages.

2.5.4 COMPRESSOR

The input signal is fed via a current controlled attenuator (Q230, Q220) to a high gain stage (IC 230) from which the output signal is taken. This signal is passed to a comparator (IC 230) which toggles whenever the audio signal exceeds a DC threshold determined by RV220. Thus, the comparator produces a square wave whose mark-space ratio is determined by the amplitude of the audio signal. This square wave pumps up the reservoir capacitor (C 233) which controls the attenuator (Q230, Q220), thus completing the feedback loop.

The compression level is set by adjustment of the comparator threshold (RV220).

Note: Although the high dynamic range of the compressor allows the use of very low audio signal levels, such conditions will be accompanied by a degradation of the signal to noise ratio. Very low audio input levels should therefore be avoided where possible.

2.5.5 OUTPUTS TO MODULATORS

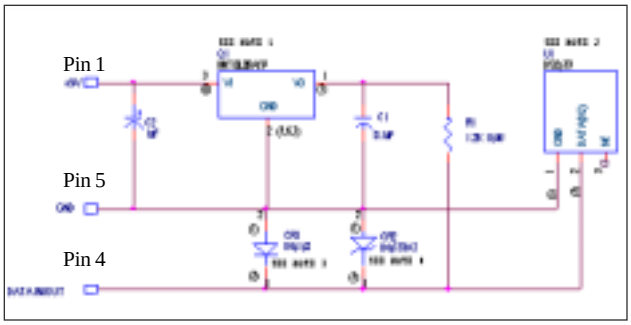
The output signal from the limiter (IC210, IC230) is added to any incoming CTCSS tone at a summing amplifier (IC 260). The signal is then low pass filtered (IC260) and split to supply the two modulators.

(*) Since the VCO modulator is a true frequency modulator, its audio is simply buffered (IC 260). The reference modulator, however, is a phase modulator and its audio must first be integrated (IC210).

(*) It is vital that the audio levels to the modulators are accurately set, relative to each other. Hence the inclusion of level adjustment in the reference modulator path. Once set, adjustments to absolute deviation may be made only by IC220, a 256-step 10k electronic potentiometere (EPOT), which is controlled via PGM800Win. The EPOT is made up of 256 resistive sections (representing approximately 39Ω each) which can be individually

addressed by the microcontroller. Each section can be switched in or out of circuit to achieve the required total resistance, thus adjusting the absolute deviation level.

3. Schematics of the memory module



The other related schematics are supplied along with the production procedure, in Appendix C.