Theory of Operation

TITLE: 100G ERT Theory of Operations
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REV	CCO	DESCRIPTION OF CHANGE	DATE	APPROVALS	
A		Initial Release	10-05-06	Project Lead	Kent Patterson
				Engineering	Jim Frost

REVISION HISTORY

1.0 PURPOSE

The purpose of this document is to describe the theory of operation for the 100G ERT® unit.

2.0 DEFINITIONS

ERT® Unit	= Encoded Receiver Transmitter
MCU	= Mobile Collector Unit – vehicle mounted reading device for the 100G unit.
FC200R	=Field Collector Unit – handheld reader / programming device for the 100G unit.
Rx	= Receive
SCM	= Standard Consumption Message
Tx	= Transmit
µP	= Micro Processor

3.0 CIRCUIT DESCRIPTION

3.1 General

The 100G is a new generation of Gas endpoints including receive capability and both high power and low power transmit capability. The unit operates in the 908 to 924 MHz band and is usable in handheld, mobile and fixed network applications. The heart of the 100G Radio section is the MICR505L RFIC, which integrates TX and RX as well as Synthesizer, Crystal Oscillator, OOK Modulator, and RFIC voltage regulator functions

3.2 Oscillator

The 16 MHZ reference frequency is provided by a shunt mode crystal working in conjunction with the MIC505L RFIC. The crystal is loaded by shunt capacitors C416 and C417 together with stray capacitance and Firmware selectable shunt capacitors within the MIC505. At initial test, the crystal output frequency is tuned to within 2 PPM. Adjustment is accomplished by measuring the RF frequency and minimizing RF frequency error by making appropriate adjustment to the reference frequency.

3.3 Transmitter

In handheld and mobile applications, the 100G operates primarily in OOK mode at +10 dBm (Low power) provided by the RFIC. Requested special messages use high power mode, described below.

In Fixed network applications the OOK output is +24 dBm (high power) provided by Q304, a single RF transistor amplifier stage driven by +10 dBm from the RFIC. Q301 and Q302 sense the Q304 collector current as a voltage drop across R302 and R303 in parallel, and adjust Q304 base to hold current constant. Low current is extremely important to allow battery life of 20 years or longer, so switch Q 303 enables the Bias control section only when the transmitted bit is a one.. By disabling PA on zero bits when no RF is desired, battery power is conserved. Operating Voltage for the high power stage is a regulated 3V, enabled for the duration of high power TX events.

3.4 Transmit Frequency Control

Transmit frequency is controlled by the transceiver synthesizer which is programmed by the microcontroller and writes to its registers via the SPI connection.

3.5 RF Switches

U201and U202 are RF switches used to connect either the High power transmitter path or the receiver and low power transmitter path to the low pass filter, antenna match and antenna.. With U301 pin 6 high and pin 4 low and U302 Pin 4 low and pin 6 high (verify) the RF path

between antenna and RFIC is selected. When the polarity of the pins on U201 and U202 is reversed, the high power RF amplifier is connected between RFIC and antenna

R318, R319, R324 and R325 are decoupling resistors. R201, R202, R203 and R204 are reference resistors for the µP. C202, C204, and C207, C346 and are bypass capacitors.

3.6 Low Pass Filter

L201, L202, C206, C208, and C209 form a 5 pole filter designed for minimal effect at the TX frequency and maximum attenuation of harmonics. The filter is directly in the path to the antenna, and is not affected by the selection of high power or low power modes.

3.7 Antenna

Depending on antenna switch control voltages the antenna connects to either the Power amplifier output or the RFIC antenna pin. The antenna is a Patch integrated on the Printed Circuit board. C8, C9, and L2 match the antenna impedance to the 50 ohm lines to either RFIC of RFPA. The antenna is tuned to operate properly when loaded by potting and the dielectric of the polycarbonate housing.

3.8 Data Transmit

Data messages, called Standard Consumption Messages (SCM), are Manchester-encoded and contain the unit ID number, meter reading and other information. The data is transmitted using Manchester encoded on/off keying (OOK) of the transceiver output and the external power amplifier. Uplink responses to programming and interrogation messages are encoded and transmitted in the same fashion

3.9 Data Receive

Downlink messages for programming and interrogation are received by the transceiver which provides NRZ data and clock signals to the microcontroller. The microcontroller interprets the downlink packet, performs the requested action, and generates the uplink response when appropriate.

3.10 Power Supply

The power supply consists of three main sections. Primary power to the 100G supply circuit is provided by a 3.68V lithium thionyl-chloride A-cell connected to J1. The battery has a nominal capacity of 3.6 Ah.

3.10.1 3V RF Power Supply voltage

All RF parts operate using voltage from the 3V regulator U1 which is turned on just prior to each RF activity and held in an off state between RF activities to conserve current.

3.10.2 RF IC regulator

The RFIC operates at 2.7 V voltage supplied by a regulator imbedded in the RF IC. This functionality resides in the chip but operates independent of the rest of the RF IC under control of the microprocessor.

3.10.3 Microprocessor supply

At 3.6 V supply, the µP sleep current drain exceeds the levels needed to allow 20 year operation on a single battery. In addition, the Micrel RFIC will not interface directly to the µP output voltages produced with 3.6 V operation. To supply the µP, Q1 and Q2 are connected as diodes, limiting µP voltage to about 2.7 V. At 2.7V, the µP IO is compatible with the RFIC and µP sleep current is reduced to about 2uA, supporting the required battery life. C7 holds sufficient charge to maintain µP voltages within required limits when the battery briefly sags during high power messages.

3.11 Read Switch

The read switch S103 is magnetically coupled to the attached meter, and changes state as the meter register rotates. The main micro detects the switch state changes, de-bounces the switch and stores the count information.

3.12 Tilt and Tamper Switches

Switch S102, along with R104, provide tilt indication to the micro. When the switch is closed by tilting the assembly, it pulls pin 24 of the micro to ground. When the switch is open, pin 24 remains high. Switch S101, along with R103; provide magnetic tamper indication to the micro. When abnormal external magnets are applied in a tamper attempt, S101 closes, pulling pin 28 of the micro to ground. When the switch is open, pin 28 remains at the µP operating voltage ~2.7 volts.

3.13 Test Points

The 100G ERT® Unit has test points available that can be utilized by test hardware and test personnel to align, monitor and trouble shoot the ERT® Unit. Refer to schematic SCH-5000-001 to locate the test points.

3.14 Main Microcontroller

The main micro, U401, is a Texas Instruments MSP430F1232IPW. In current conservation mode the µP clock is supplied by Y401, a 32.768 KHz crystal. When faster execution is necessary, the µP runs on it's internal oscillator at up to 5 MHz Further, it receives an 8 MHz clock from the TCXO (TCXO divided by two) periodically to perform accurate functions such as transmitting, receiving and real time clock updates. There are several referencing resistors on the circuit board to assure that micro pins are not left in a high impedance floating state, whereby they can sink or source high current. These include R401-R403, R407-R418 and R422-R427. An in depth description of the micro's functionality is explained in the firmware section of this document. Below is a table of the micro's pins and their functions. ERT® UNIT SPECIFICATIONS

3.15 ERT® Unit Specifications

The specifications listed apply to the 100G ERT® Unit as measured on the FCC site. The unit should be installed in housing and potted.

Item #	Description	Specification
1	Transmit High Frequency	922 MHZ
2	Transmit Low Frequency	908 MHZ
3	Receive Frequency	908-922 MHZ[2]
4	Transmit BW	<200 kHz
5	Transmit Power	FN mode: +24 dBm EIRP Mobile mode: +10 dBm EIRP
6	Receive Sensitivity	-100 dBm
7	Idle Current	<2µAmps

4.0 TUNE AND TEST

4.1 Setting Frequency

During manufacturing, it is preferred to set the unit on frequency. Although the unit is synthesized, there are slight variations in the finish frequency of the crystal as well as variations of the amount of loading capacitance on the crystal. Even though these variations are slight, they can add up to several kilohertz of offset at the transmit frequency. There is also a slight shift in frequency due to capacitive loading effects caused by potting. During manufacturing the frequency is calibrated before it is potted, with an offset to accommodate the expected change when potted.

5.0 FIRMWARE

5.1 Firmware Build Information

This firmware is built from C-language and assembler code contained in twelve different files.

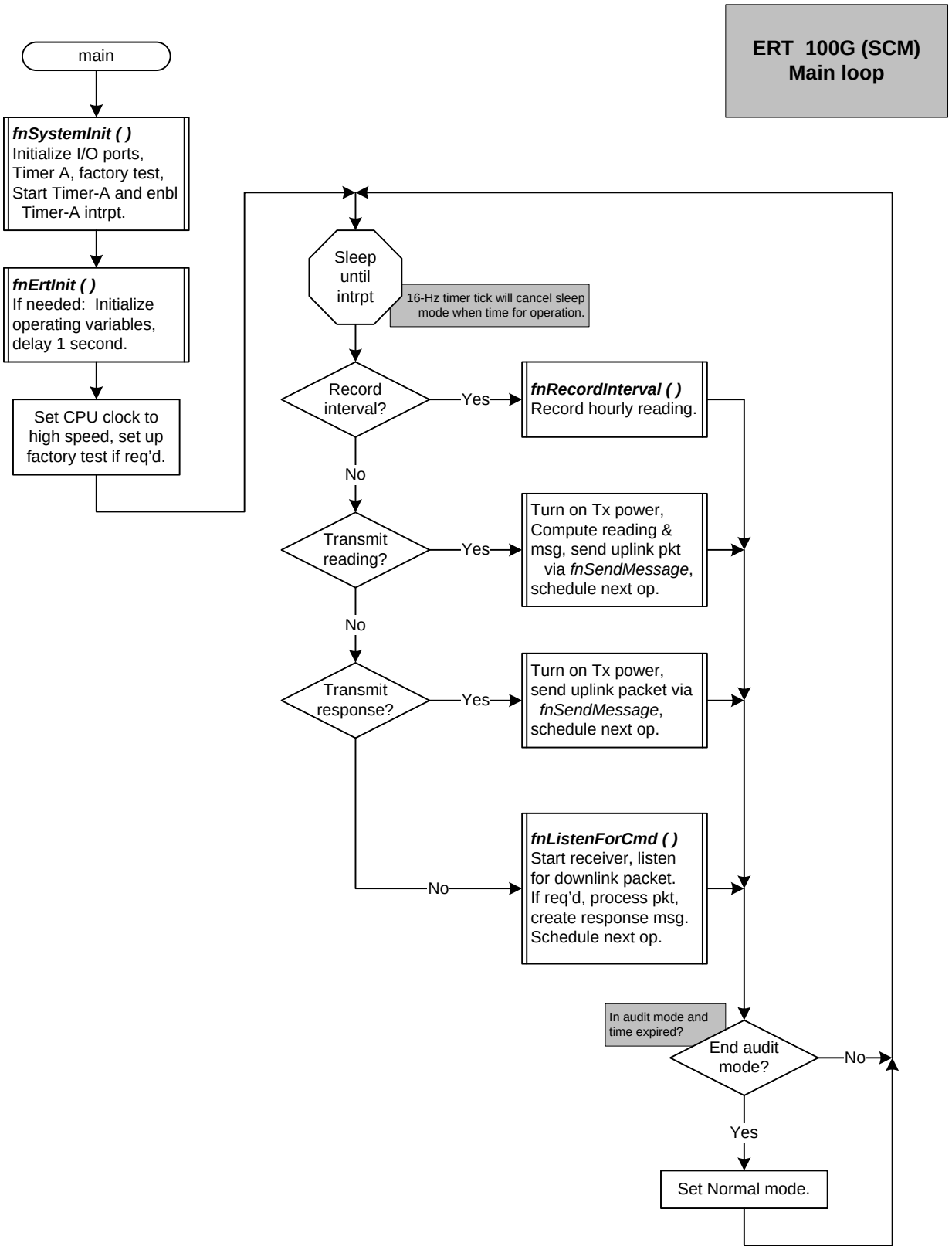
File name	Contents
ERT100Gx.c	Main source file: Main execution and reading/tamper recording for 100G ERT.
Global.h	Global-variable definitions and definitions for identifying conditional compile options.
ERT100Gx.h	Manifest-constant definitions for global use and prototypes for functions in ERT100Gx.c.
Hwdefs.h	Manifest-constant definitions for I/O ports.
RF_serv.c	RF-service routines for transmitting and receiving message.
RF-serv.h	Definitions and prototypes for 100G RF-service code.
Msg_proc.c	Code for processing downlink messages and creating uplink messages.
Msg_proc.h	Definitions and prototypes for message processes.
Xcvr_srv.c	Routines for communication with the transceiver-ASIC
Xcvr_srv.h	Definitions and prototypes for transceiver-ASIC service.
Utils.s43	Assembly-language utility functions.
Utils.h	Prototypes for functions in Utils.s43

5.2 On Chip Memory

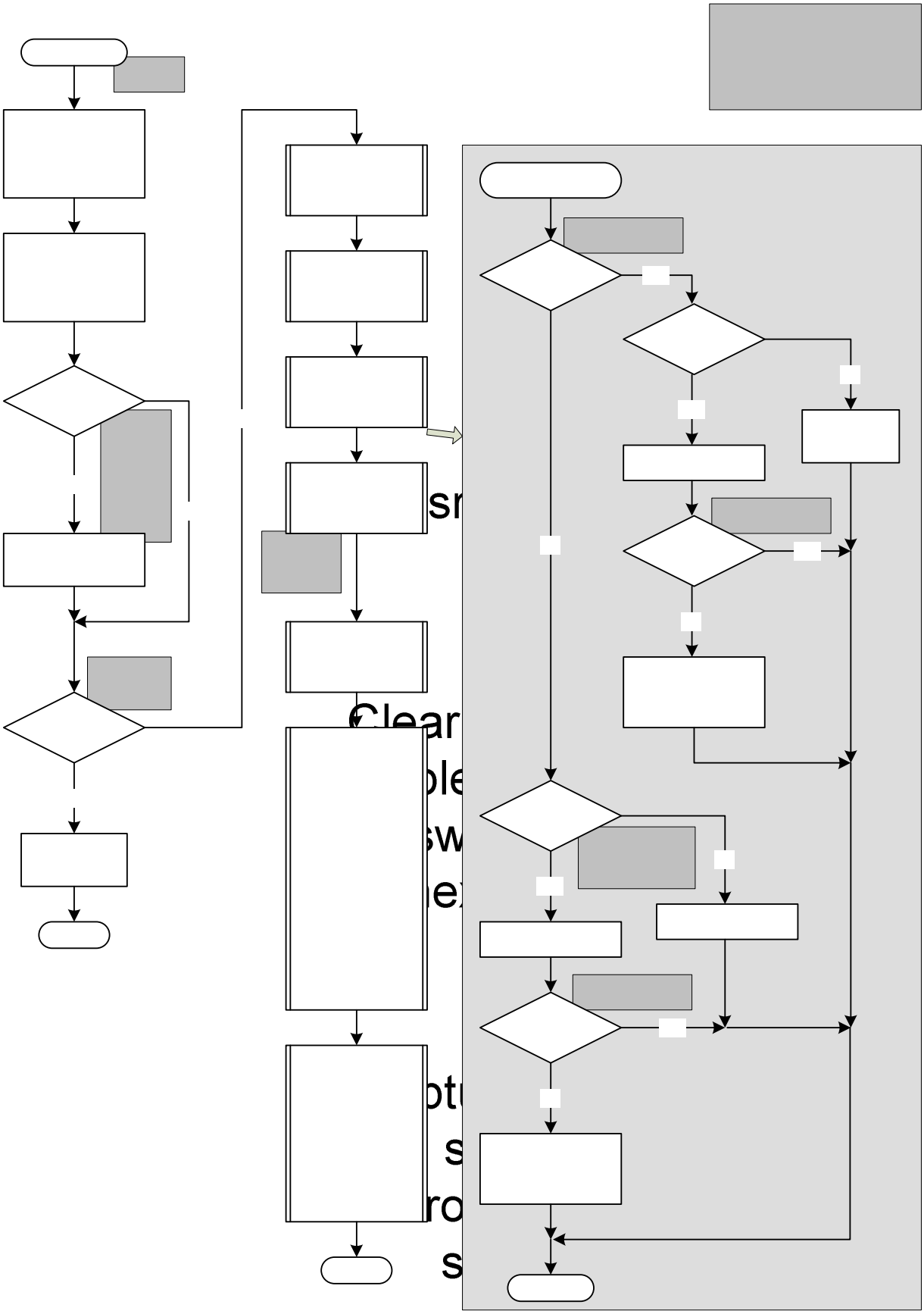
The MSP430 microcontroller has two flash-memory INFO blocks for saving ERT ID, hop tables and programmable parameters and 256 bytes of RAM used for data storage, message buffers, control variables and stack.

5.3 Main Code Flow

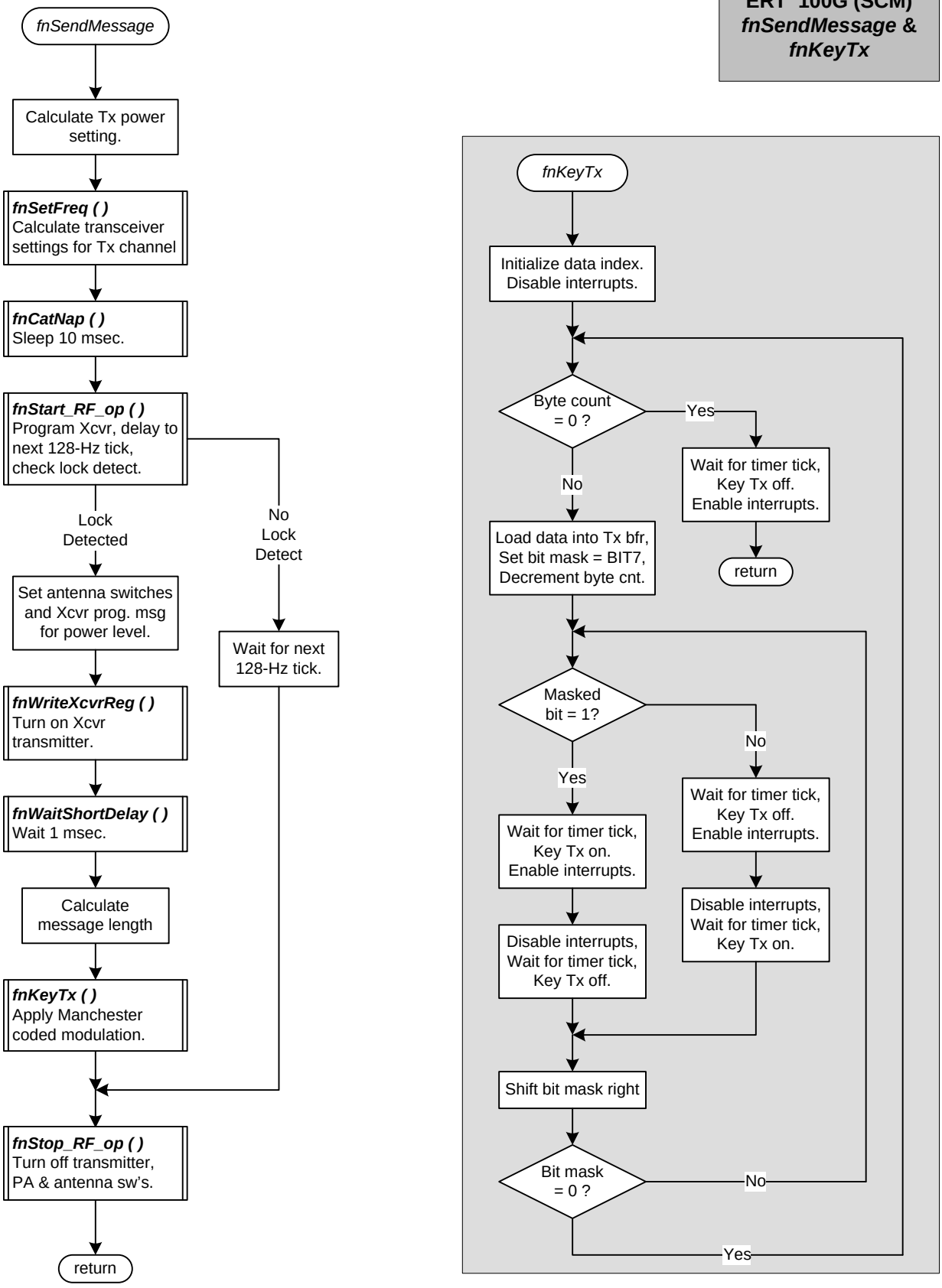
The following flowchart contains the overall view of the firmware operation for the 100G.



5.4 Timing Interrupt and Reading Debounce



5.5 100G Transmit

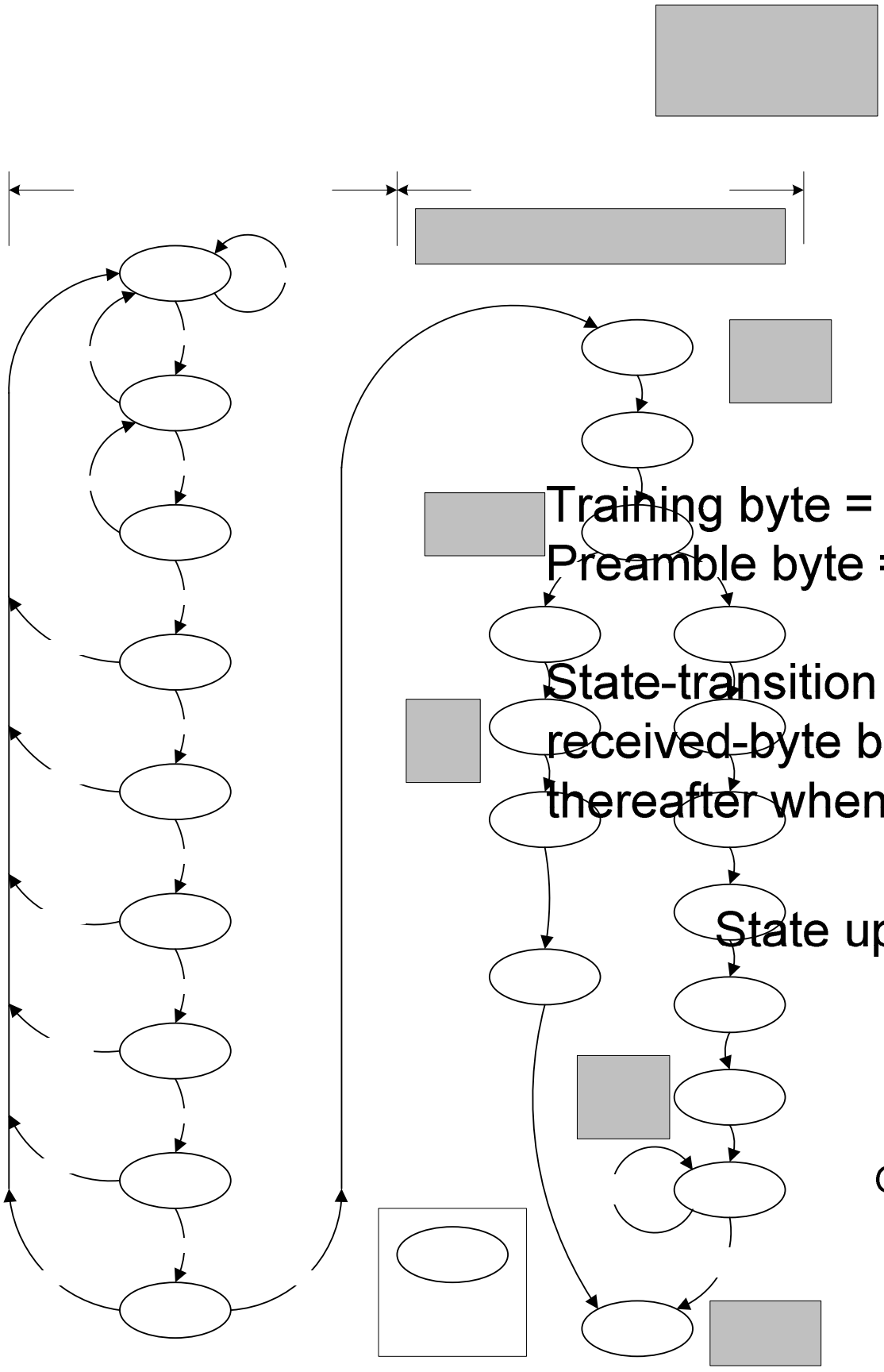


5.6 Timing Parameters for 100G Transmit

Ref.	Function	Operation	Cycles
1	fnTxKey	Send 1st chip – send 2nd chip (allows interrupts)	20
2		Send 2nd chip – send 1st chip in same byte.	31
3		Send 2nd chip – send 1st chip in next byte.	47
4		Send 2nd chip – send 1st chip in next byte during factory test.	57
5		Send last 2nd chip – Tx off.	38
6		"Just-missed-it" reread communication flag.	5
7	isrTiming	Minor tick (128 Hz) (Major tick cannot occur during message Tx.)	52
		Worst combination of operations (reference numbers):	#1, 6, 7
		Worst case number of cycles required in 30.5 µsec	77
		Minimum CPU clock frequency (MHz.) required	2.53

Analysis of the microcontroller DCO (digitally-controlled oscillator) specifications yields a worst-case minimum CPU clock frequency of 2.968 MHz at the temperature extremes.

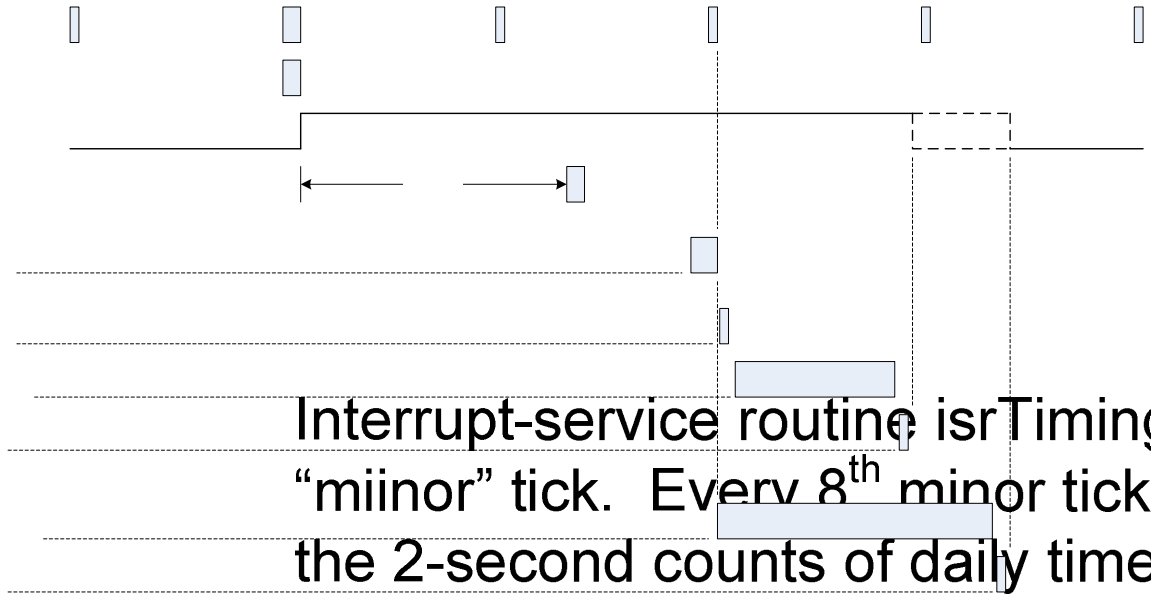
5.7 100G Receive



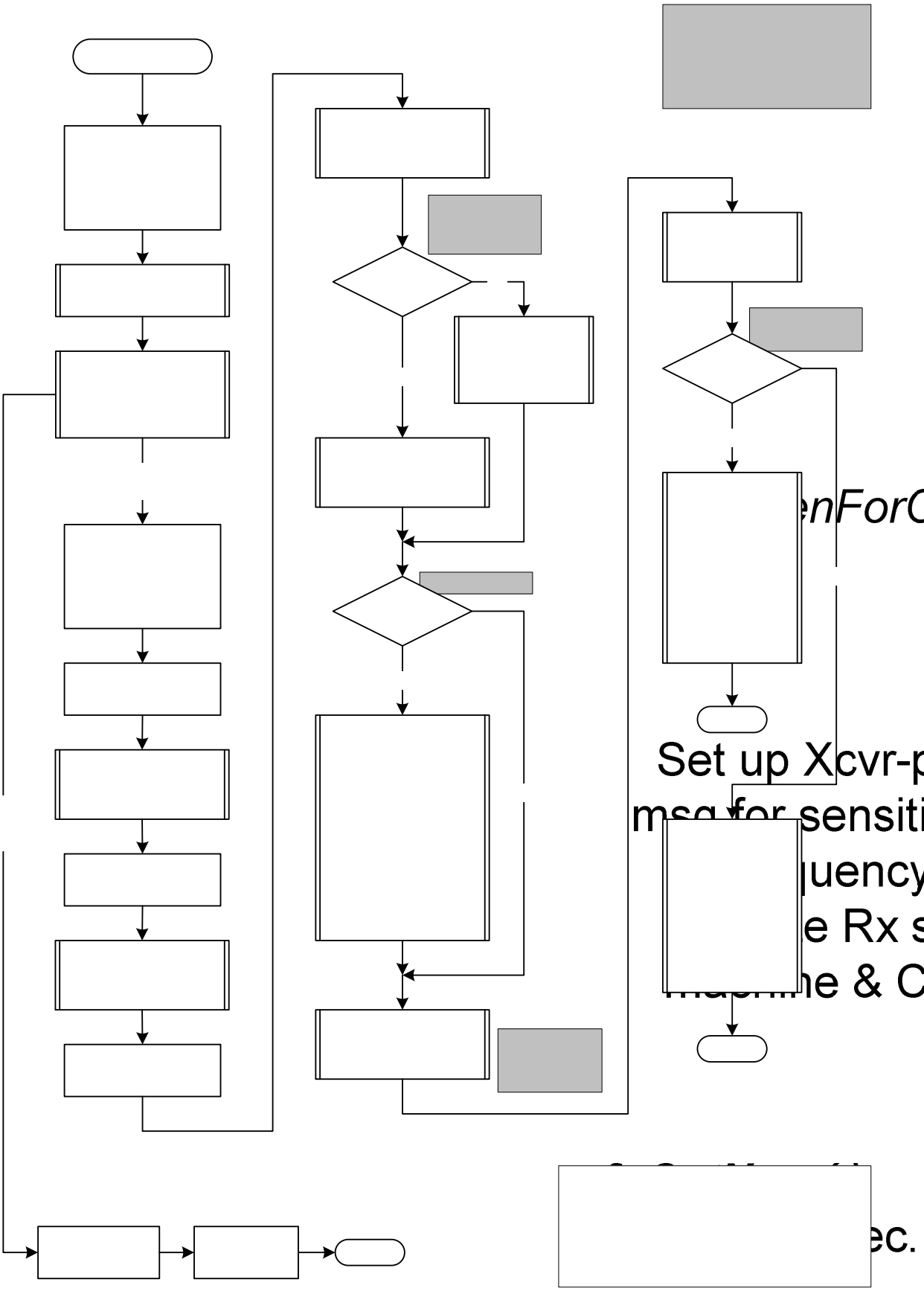
5.8 Timing Parameters for 100G Receive

Ref.	Function	Operation	Cycles
1	isrRxData	State = GET_TRAINING	55 – 61
2		State = GET_PREAM_7	62 – 64
3		State = GET_PREAM_0	61 – 70
4		States = GET_ID_0 – GET_PD_CRC: process data bit 7 – 1	70 – 77
5		State = GET_R_TIME	111 – 118
6		State = GET_PD_CRC: process bit 0 – buffer a data byte	136 – 143
7	isrTiming	Time to enable interrupts.	14
8		Minor tick (128 Hz)	52
9		Major tick (16 Hz)	161 – 278
10	fnWaitForRxState	Pass through function with 1 extra loop	35
		For completing isrRxData in time to enter again	#6, 7
		Worst case number of cycles required in 80 µsec	157
		Minimum CPU clock frequency (MHz.) required	1.97
		At 1.97 MHz check for completion of interrupted Major timing tick in time:	#6, 7, 9
		157 - 77 = 80 Cycles are available in the next 7 data periods for completing an interrupted Major timer tick. The number of additional data periods required = (278 – 14) / 80	3.3
		The 2.968 MHz minimum clock frequency will complete a worst-case Major tick interrupted by a worst case Rx-data byte in a total of 3 Rx-data-interrupt periods (240 µsec) with a CPU-cycle reserve of	137

5.9 Timing for 100G TX and RX



5.10 100G Listen



5.11 Transmit Hopping

The 100G ERT uses a table selected according to its ERT ID to control transmitter hopping. The hop table is a series of 50 values from 0 to 49 arranged in pseudo-random order. The ERT takes the hop table values in sequence for successive hopping transmissions, beginning the sequence anew when it reaches the end. The least significant byte of the ERT ID is used to select the table. The hop table is programmed in the factory at the time the ERT ID is programmed.

The ERT transmits in a split band consisting of two half bands. The locations of these are controlled by the lower-half-band offset and the upper-half-band offset – programmable parameters stored in INFO memory. Hop table values from 0 through 24 are added to the lower-half-band offset to determine the transmit frequency. Hop table values from 25 through 49 are added to the upper-half-band offset to determine the transmit frequency. The default settings for the offsets are 40 and 50, giving default full-band channels of 40 to 64 (910.0 – 914.8 MHz) for the lower half band, and full-band channels 75 to 99 (917.0 to 921.8 MHz) for the upper half band.

6.0 Modulation Process

ERT messages employ Manchester encoding at 16,384 bits / second. In Manchester coding a one is transmitted with the transmitter keyed on for the first half of the bit, off for the second half. The two bit halves are referred to as “chips”. For a zero bit the transmitter is keyed off for the first chip, on for the second. Each chip is 30.5 µsec in duration.

As soon as each chip is initiated and communicated to the RF hardware, the firmware must calculate the next and have it ready before the 30.5 µsec is up. The firmware fetches each data byte from the message, computes and sends 2 chips for each of 8 bits. The three time critical operations in the process are:

- Send first chip of bit, compute second chip.
- Send second chip, compute first chip of the next bit from the same byte.
- Send second chip, get next byte and compute first chip of its most significant bit.

The first of these is the simplest and shortest. The third is the most complicated and longest.

Actually there is one more operation that is esthetically unappealing if it doesn’t complete on time: send the second chip of the last bit of the message and prepare to set final “transmitter off”. (If it’s late the message will still be readable).

Because processor timing is independent of the 32768 Hz timing reference, the modulation routine must poll for an asynchronous notice that a chip was sent by interrupt or that the Timer has advanced before it can “do” the next chip. For this reason, the timing analysis includes a “just-missed-it” count for interrogations that need one more loop to determine that it’s time to continue. It adds a margin of safety.

In addition to the modulation operation, the 30.5 µsec period must also accommodate any other interrupt that occurs within it. The design plan for the 100G firmware is that time-scheduled operations will be set up and initiated by the 16Hz time tick which will also process tilt-switch data and mag-tamper data. Because there is a great deal of computing involved in these operations (relatively speaking), all messages must be transmitted between 16Hz ticks. (This also eases hardware requirements that would be needed to support transmission of longer messages.) Hence, the “minor” 128 Hz tick is the only (other) interrupt allowed during transmission of a message.

The timing analysis adds up the number of main-clock cycles required to execute the code within a 30.5 µsec chip time and calculates the minimum clock frequency required to accomplish that. This analysis is focused on the transmitter modulation since none of the other operations have time criticality remotely approaching the challenge of squeezing the modulation operations into 30.5 µsec slots.

7.0 Non-Volatile Data Procedures

Non-volatile data is maintained in the two 128-byte INFO blocks in the microcontroller. 100G firmware initializes the programmable values to their default settings when code in programmed into

the device. INFO memory locations for manufacturing-test frequencies, ERT ID and hop table are left in their non-programmed states by the 100G firmware. These locations are programmed in the manufacturing process.

8.0 Programmed Variables and Default Values

8.1 Rollover

Description	Binary Code	
9,999	00	
99,999	01	
999,999	10	**Default**
9,999,999	11	

8.2 Tilt Debounce

Description	Binary Code	
No Tilt Tamper	00	
100ms	01	
250ms	10	
500ms	11	**Default**

8.3 Count Rate

Multiplier	Binary Code	
Undefined	0000	
Undefined	0001	
Undefined	0010	
1.	0011	**Default**
2.	0100	
5.	0101	
10.	0110	
20.	0111	
25.	1000	
40.	1001	
50.	1010	
100.	1011	
500.	1100	
1000.	1101	
Undefined	1110	
Undefined	1111	

8.4 Lock Type

Description	Binary Value	
No Lock	00	**Default**
Soft Lock	01	
Hard Lock	10	
Undefined	11	

8.5 ERT® ID

The 26 bit ERT® Unit ID is programmed at the factory into the INFO block.

8.6 Hop Table

The 50-byte hop table appropriate for the ERT ID is programmed at the factory into the INFO block.

8.7 ERT® Type

The 4 bit ERT® Unit Type is programmed to type 12 for the 100G by the ERT firmware.

8.8 Count Debounce

The count debounce values are programmed at by the ERT firmware and cannot be altered in the field.

8.9 Meter Reading

The 24 bit meter reading is programmed at the time of installation by the Reader/Programmer device. Default value is zero for all 24 bits.

8.10 Pressure Compensation Multiplier

The 17 bit pressure compensation multiplier assumes a decimal point between the first and second bits and is programmed by the Reader/Programmer device at the time of installation. Default value is 1.0000.

8.11 Utility ID

The 16 bit Utility ID is programmed at the time of installation by the Reader/programmer device.

8.12 Tamper Fields

Two tamper fields are use to record theft attempts by Tilt and Magnetic tamper. The two bit fields for Physical tamper and Encoder Tamper are reset to the default value of zero by the Reader/Programmer with a downlink-command message.

8.13 Bubble-Up Period

The 8-bit field default value for bubble-up period is pre-set in firmware at 15 seconds. It can be altered via programming from 2 to 255 Seconds.

8.14 Transmit-Power Setting

The 4 bit code for indicating the normal-mode transmit power is pre-set in firmware to +10 dBm. It can be altered via programming to 0 dBm or to +24 dBm.

8.15 Default Programming Channel

The default programming channel is initially set to channel 30 (908.0 MHz) and may be altered via programming to any channel from channel 1 (902.2 MHz) to channel 129 (927.8 MHz).

8.16 Lower-Half-Band Offset

The lower-half-band offset is added to values from 0 through 24 retrieved from the hop table for transmitting. It is initially set to 40 (giving a lower half band from 910.0 to 914.8 MHz) and may be altered via programming to any value from 1 (lower half band at 902.2 MHz) to 80 (lower-half band at 918.0 MHz). Attempts to program the lower-half-band offset such that the lower half band overlaps or is higher than the upper-half band will be rejected by the ERT.

8.17 Upper-Half-Band Offset

The upper-half-band offset is added to values from 25 through 49 retrieved from the hop table for transmitting. It is initially set to 50 (giving an upper half band from 917.0 to 921.8 MHz) and may be altered via programming to any value from channel 1 (upper half band at 907.2 MHz) to 80 (upper half band at 923.0 MHz). Attempts to program the upper-half-band offset such that the lower half band overlaps or is higher than the upper-half band will be rejected by the ERT.