PROCEDURE 01-001

ELECTRONIC SYSTEMS TECHNOLOGY
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509-735-9092 (O)
509-783-5475 (FAX)

Date: July 17, 2001

Subject : FCC 15.247(e) Jamming Margin Test on the ESTeem Model 192E

Tools Required : See equipment list in the report.

Parts Required : 2 ea. ESTeem Model 192E

Scope:

This report presents the test procedure, test configuration and test data associated with FCC Part 15.247 (e) Jamming Margin test for indirect measurement of processing gain.

Test Background and Procedure

According to FCC regulations 15.247 (e) , a direct sequence spread spectrum system must have a processing gain, of at least 10 dB. Compliance to this requirement can be shown by demonstrating a bit error ratio (BER) performance improvement between the spread spectrum processes (coding, modulation) are engaged relative to the processes being bypassed. The ESTeem 192E process gain can not be bypassed. The processing gain can be indirectly measured by the Jamming Margin test described in FCC 15.247 (e)2

Test Procedure

Setup the simplex hardware link as shown in Figure 1. Perform all independent instrumentation calibrations prior to starting test. Set operational power levels using fixed and variable attenuators in the system to meet the following objectives:

1. Adjust signal power at receiver to approximately –60 dBm. Use the spectrum analyzer to verify.
2. Ensure that the CW Jammer generator RF output is disabled and measure the Model 192E RF power with the power meter. This measurement will be the relative signal power level.
3. Disable the Model 192E transmitter, and set CW Jammer generator RF output frequency equal to the carrier frequency and enable generator output. Set the CW Jammer reference power level at the power meter to 8.4 dB (for 11 Mbps) or 2.6 dB (for 2 Mbps) below the level of the Model 192E relative measurement measured in step 2. This will set the relative Signal to Jammer ratio, the limit to pass the 10dB processing gain test for a BER of $10^{-5.}$
4. Disable the CW Jammer and reestablish the communications link between Model 192E units 1 and 2.
5. Enable CW Jammer at a low power level and gradually increase the CW Jammer output power until the BER test indicates the reference BER level is 10^{-5}.
6. Step the CW Jammer 50 KHz then increase the output power level until the BER is equal to the reference BER. Record the Jammer power level.
7. Repeat step until the all of the receiver passband has been tested. Reference Figure 2.

   This technique is used for a fixed signal carrier frequency with uniform frequency increments of 50 KHz across the receiver passband using the CW Jammer. In this case the receiver bandpass is ± 8.5 MHz.

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The processing gain is related to the jamming margin as follows:

$G_p = BER_{REFERENCE} \leftrightarrow (S/N)_{OUTPUT} + (J/S) + L_{system}$

$BER_{reference}$ is the reference bit error ratio with its corresponding theoretical output signal noise ratio per symbol, $(S/N)_{output.}$
(J/S) is the jamming margin (jamming signal power relative to desired signal power)
L_{system} is the system implementation losses.

The ESTeem 192E utilizes the Intersil PRISM HFA3863 base band processor. The bit rates are 1, 2, 5.5, and 11 Mbps. The corresponding symbol rates are 1, 1, 1.375, and 1.375 MSps. The chip rate is always 11 MCps, so the ratio of chip rate to symbol rate is 11:1 for the 1 and 2 Mbps rates and 8:1 for the 5.5 and 11 Mbps rates [1].

For the 1 and 2 Mbps modes, the transmitter accepts data, scrambles it, differentially encodes it as either DBPSK or DQPSK and spreads it with the BPSK PN sequence. [2]. This means that for every error that occurs the differential decoding extends that to 2 errors. Thus, you can expect the theoretical BPSK 9.6 dB Es/No performance for BER of 10^{-5} to be degraded to 10.6 dB. [3] The implementation losses of 2 dB are then added for a total of 12.6 dB

$Gp = (Eb/No) + (J/S) + L_{system}$

Gp = 10.6 dB + (J/S) + 2 dB

Gp = 12.6 dB + (J/S)

The minimum processing gain is 10 dB therefore:

$Gp = 12.6\ dB + (J/S) \geq 10 dB$

The minimum jammer to signal ratio for 2 Mbps rate is as follows:

$(J/S) \geq -2.6$ dB

For 5.5 and 11 Mbps modes, the transmitter partitions the data into nibbles (4 bits) or bytes (8 bits). At 5.5 Mbps, it uses two of those bits to select one of 4 complex spread sequences from a table of CCK sequences and then QPSK modulates that symbol with the remaining 2 bits. At 11 Mbps one byte is used of which 6 bits select one of 64 spread sequences for a symbol and the other 2 are used to QPSK modulate that symbol. [2].

There are losses with complementary encoding and scrambling that cause loss in performance due to error extension. Intersil states that the Es/No is 16.4 dB at BER of 10^{-5} [1] . The implementation losses of 2 dB are then added for a total of 18.4 dB.

$Gp = (Eb/No) + (J/S) + L_{system}$

Gp = 16.4 dB + (J/S) + 2 dB

Gp = 18.4 dB + (J/S)

The minimum processing gain is 10 dB therefore:

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Gp = 18.4 dB + (J/S) $\geq$10dB

The minimum jammer to signal ratio for 11 Mbps rate is as follows:

(J/S)$\geq$ -8.4 dB

The Jammer Margin test procedure allows the worst 20% of the J/S points to be discarded.

The minimum measured processing is 10 dB. Therefore the 192E complies with the 10 dB minimum processing gain requirement.

The graphical data associated with the following radio channels and chip symbol rates is tabulated and presented for:

Channel 1: 2412 MHz 2 Mbps Figure 2
Channel 6: 2437 MHz 2 Mbps Figure 3
Channel 11: 2462 MHz 2 Mbps Figure 4
Channel 1: 2412 MHz 11 Mbps Figure 5
Channel 6: 2437 MHz 11 Mbps Figure 6
Channel 11: 2462 MHz 11 Mbps Figure 7

The test equipment used is listed below.

Equipment	Serial Number	Calibration Date
Philips PM6680 Frequency Counter	CN944606680011	4/9/01
HP 437B Power Meter w/ Power Sensor HP 8481A	3125U10268 2702A72310	4/9/01
HP 8648C Signal Gen.	3426A0072	3/7/01
HP8569B Spectrum Analyzer	2409A01015	4/7/01
Mini-Curuits ZN2PD-9G		
Kay Elemetrics PMAX 3W Step Attenuator		
Inmet 20 dB pad		

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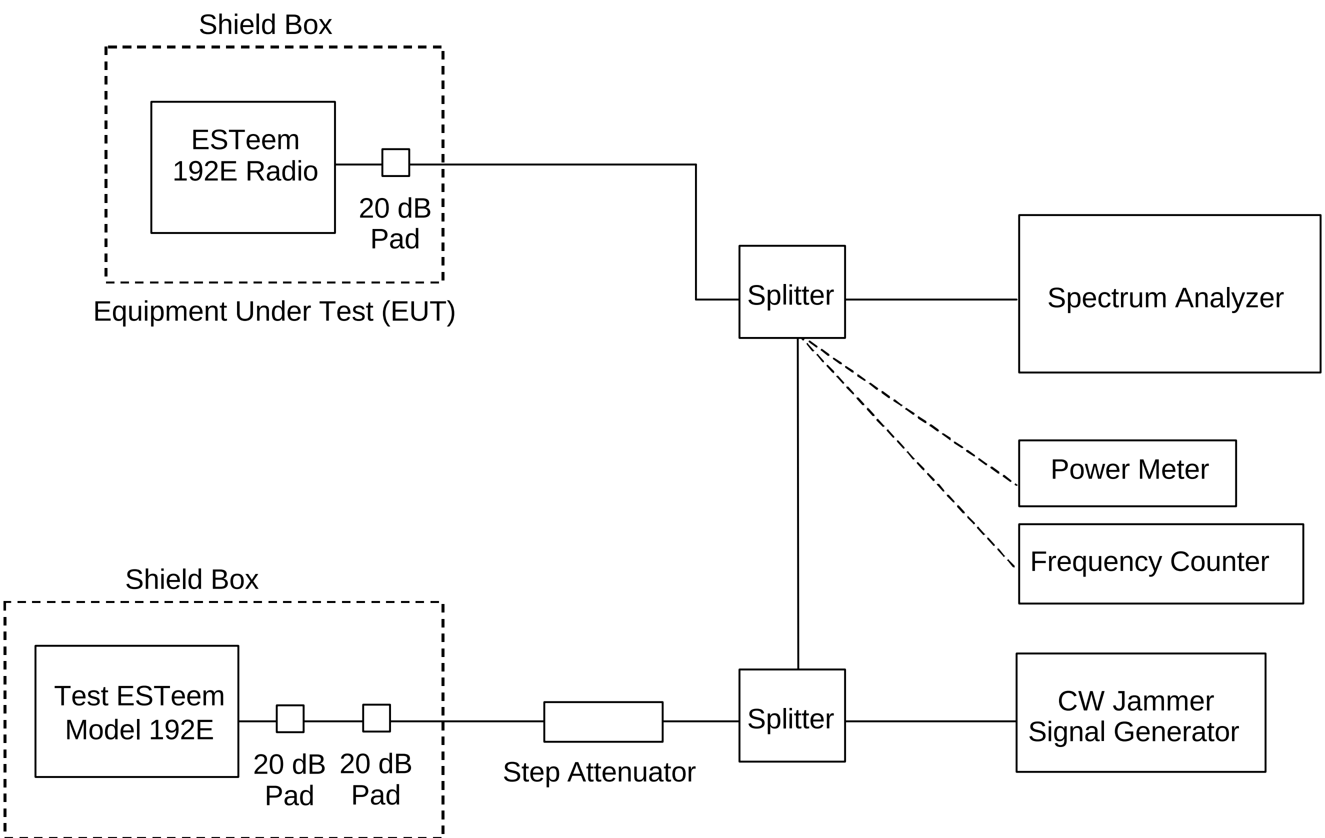

Test Block Diagram

Figure 1

[1] Carl Andren "Testing for Compliance with FCC Rules 15.247e". Intersil Corporation, January 11, 2000.

[2] "HFA3863 Data Sheet". Intersil Corporation, April 2000

[3] Carl Andren "A Comparison of Frequency Hopping and Direct Sequence Spread Spectrum Modulation for IEEE 802.11 Applications at 2.4 GHz." April 11th 1997

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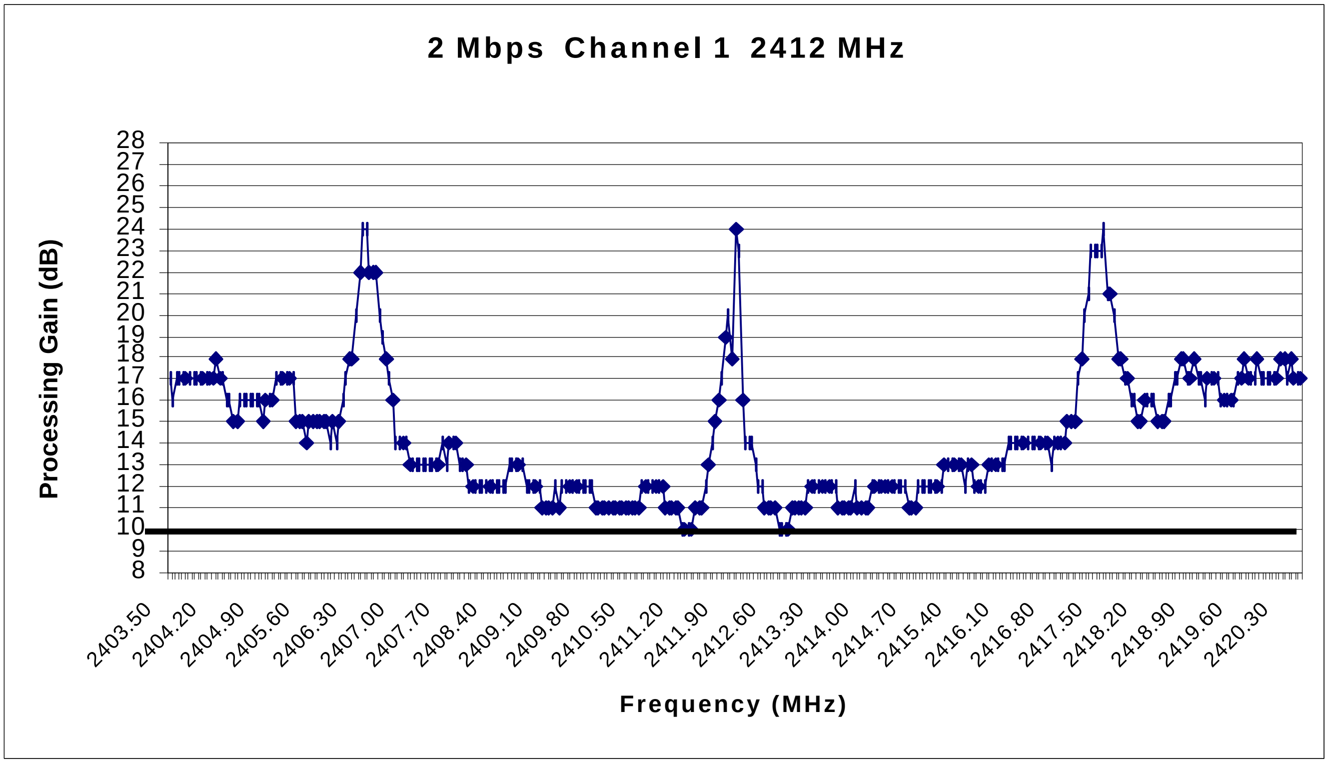

Jamming Margin Numerical Test Data Graph
Channel 1 - 2412 MHz – 2 Mbps
Figure 2

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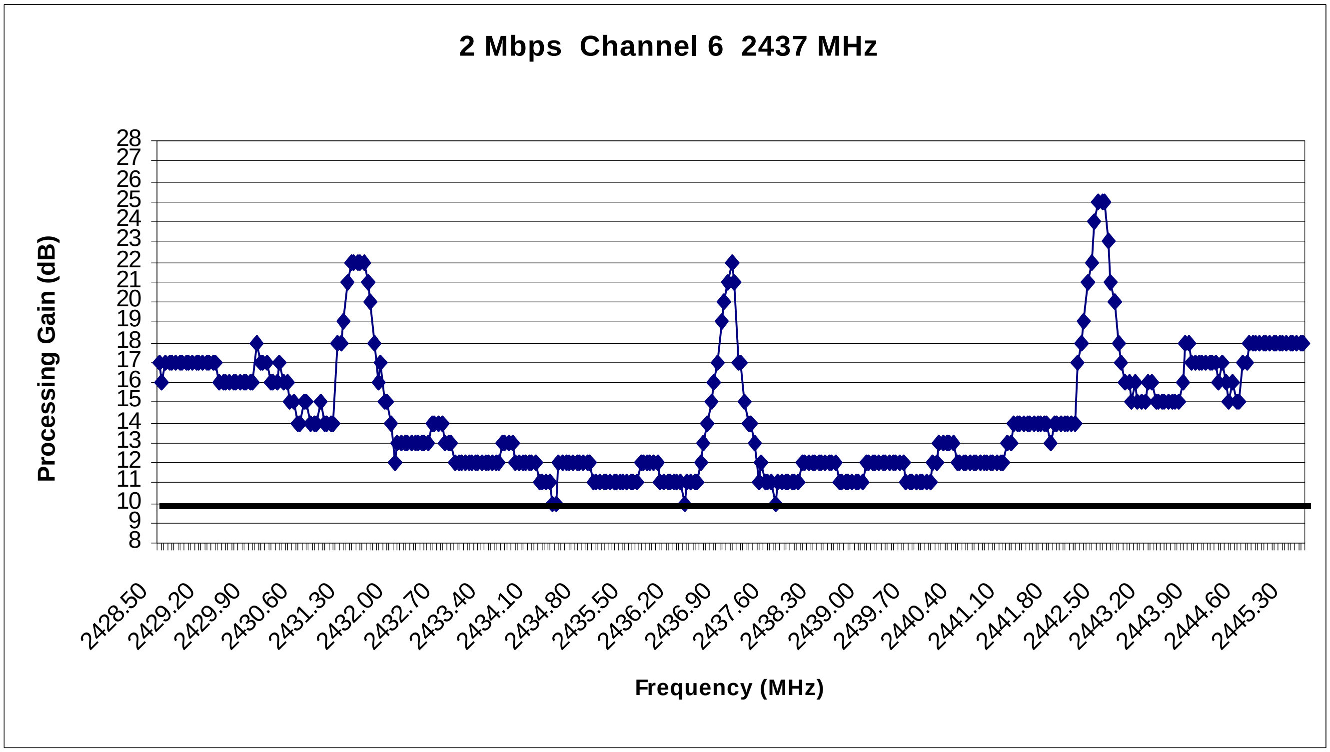

Jamming Margin Numerical Test Data Graph
Channel 6 - 2437 MHz – 2 Mbps
Figure 3

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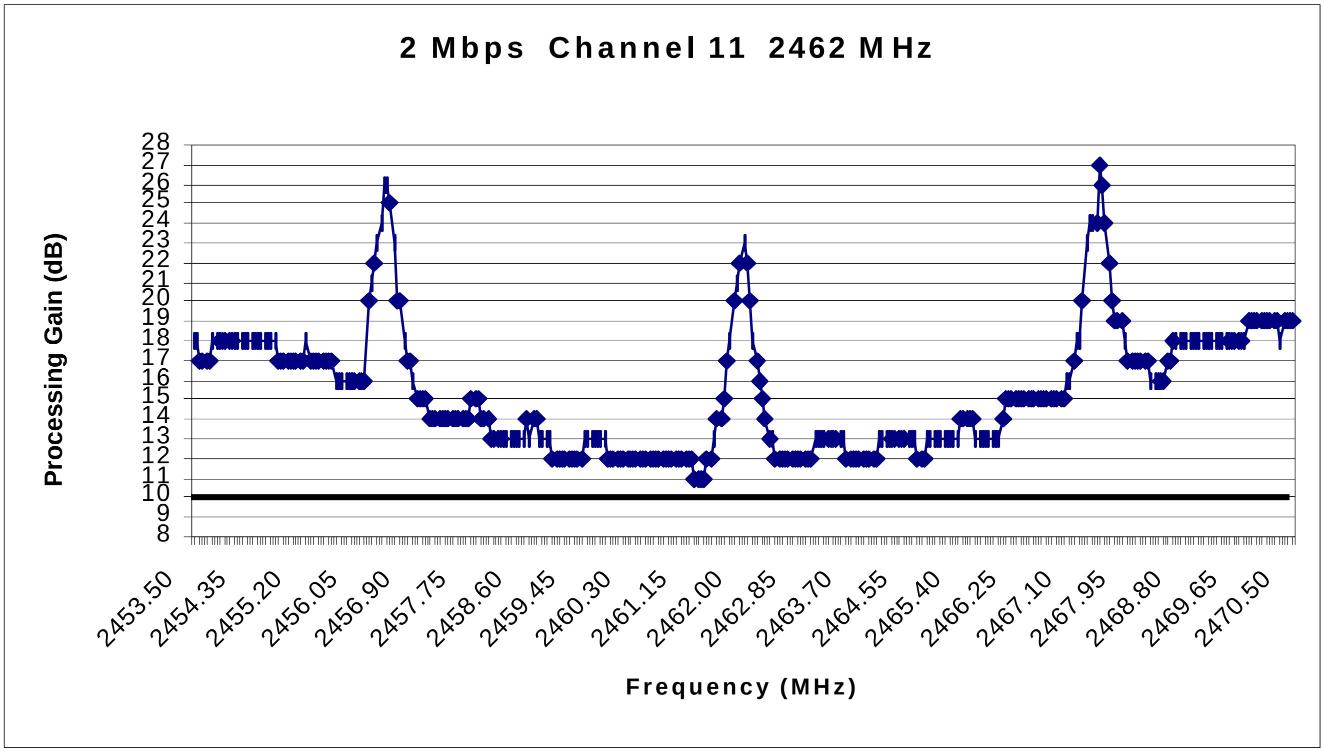

Jamming Margin Numerical Test Data Graph
Channel 11 - 2462 MHz – 2 Mbps
Figure 4

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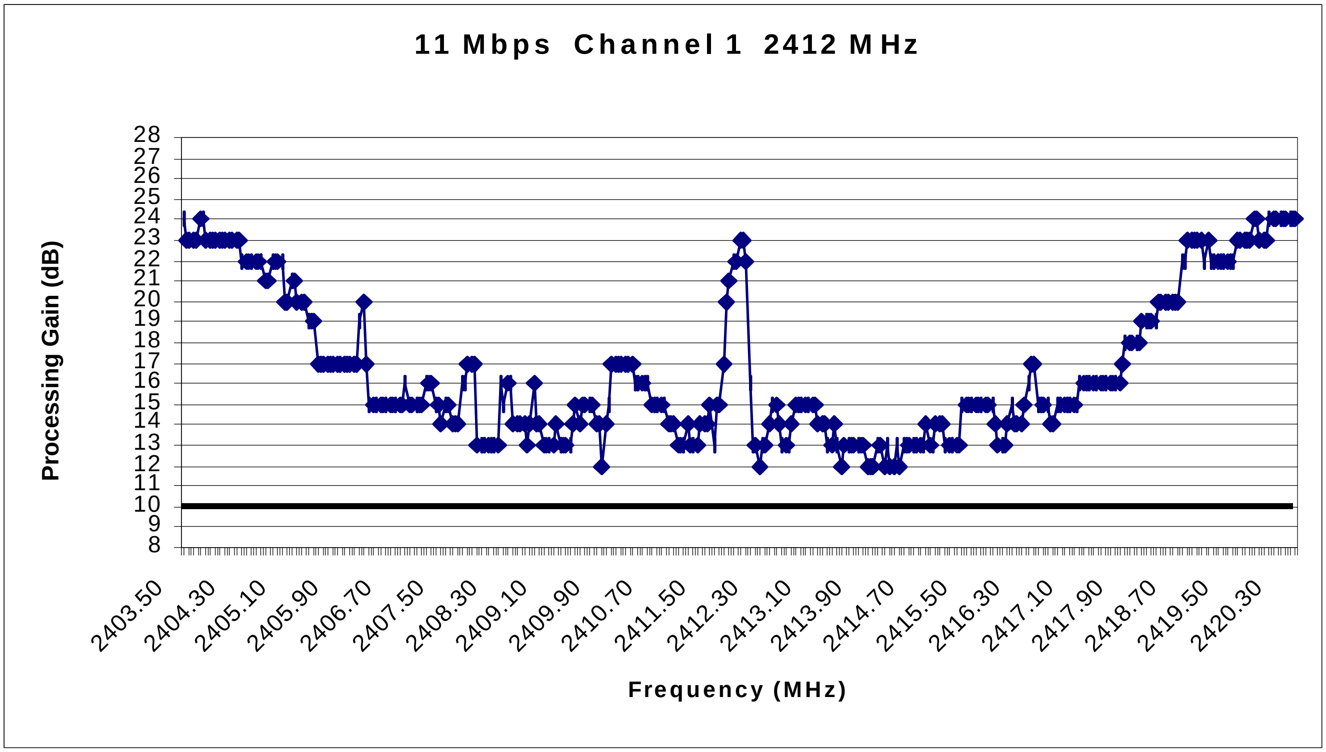

Jamming Margin Numerical Test Data Graph
Channel 1 - 2412 MHz – 11 Mbps
Figure 5

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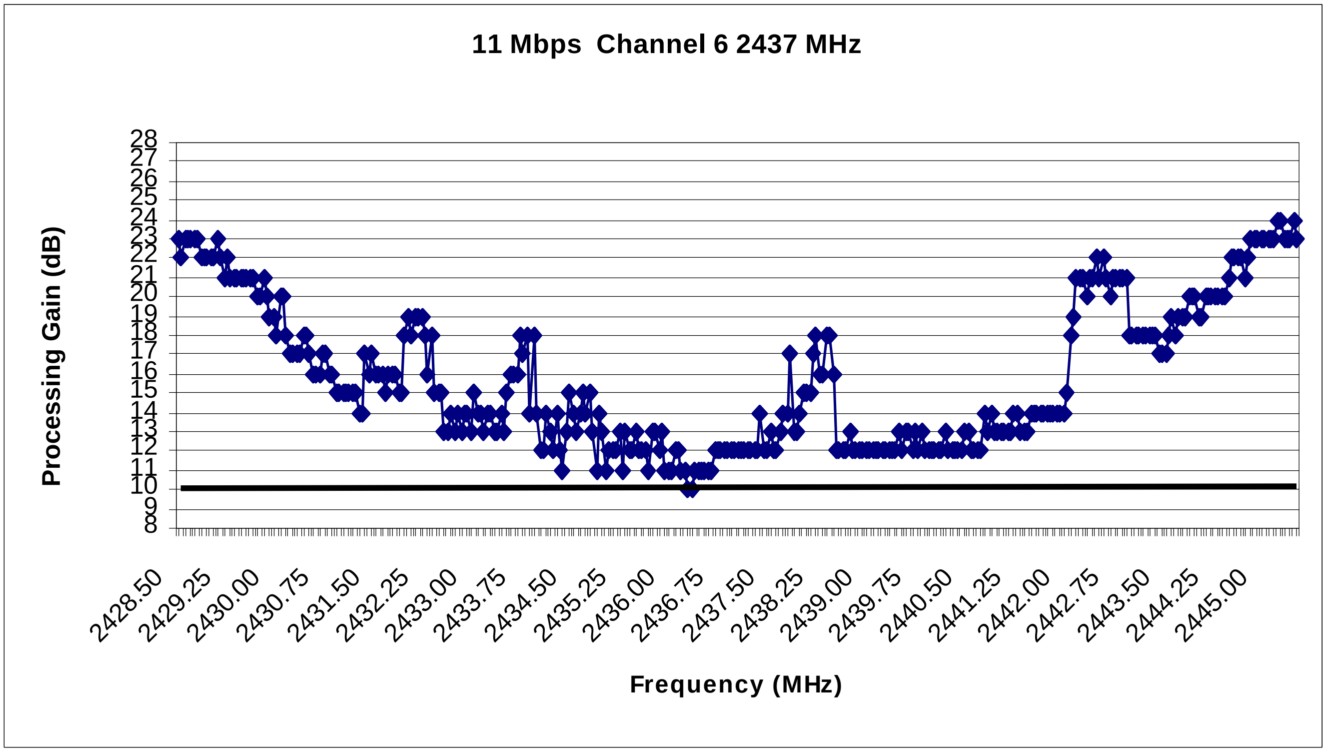

Jamming Margin Numerical Test Data Graph
Channel 6 - 2437 MHz – 11 Mbps
Figure 6

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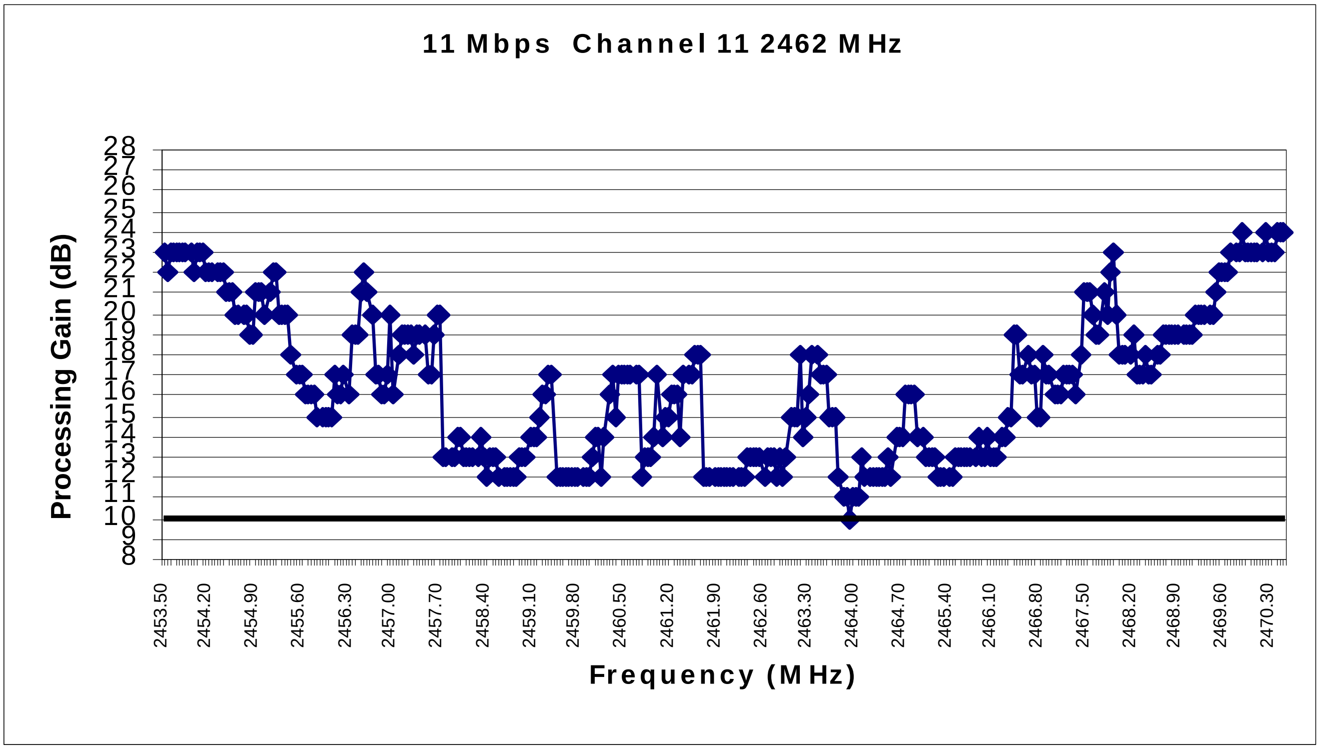

Jamming Margin Numerical Test Data Graph
Channel 11 - 2462 MHz – 11 Mbps
Figure 7