1.2. Operational Description

The EUT is a TRANSCEIVER with built-in 900MHz FHSS transceiver. The number of the channels is 25 in 909 - 919MHz. The device adapts the frequency hopping spread spectrum modulation. The antenna is monopole and solder on PCB and provides diversity function to improve the receiving function.

The system receivers have input bandwidths that match the hopping channel bandwidths of their corresponding transmitters and shift frequencies in synchronization with the transmitted signals

Frequency hopping spread spectrum systems are not required to employ all available hopping channels during each transmission. The transmitter is presented with a continuous data stream. In addition, a system employing short transmission bursts must comply with the definition of a frequency hopping system and must distribute its 25 channels and over the minimum number of hopping channels (25 channels).

The incorporation of intelligence within a frequency hopping spread spectrum system that permits the system to recognize other users within the spectrum band so that it individually and independently chooses and adapts its hop sets to avoid hopping on occupied channels is permitted. The coordination of frequency hopping systems in any other manner for the express purpose of avoiding the simultaneous occupancy of individual hopping frequencies by multiple transmitters is not permitted.

The frequency shift keying (FSK) transceiver intended for use in half-duplex, bidirectional RF links. The multi-channeled FSK transceiver is intended for UHF radio equipment.

The transmitter consists of a PLL frequency synthesizer and power amplifier. The frequency synthesizer consists of a voltage-controlled oscillator (VCO), a crystal oscillator, dual modulus prescaler, programmable frequency dividers, and a phasedetector. The loop-filter is external for flexibility and can be a simple passive circuit. The output power of the power amplifier can be programmed to seven levels. A lock-detect circuit detects when the PLL is in lock. In receive mode, the PLL synthesizer generates the local oscillator (LO) signal. The N, M, and A values that give the LO frequency are stored in the N0, M0, and A0 registers.

Another detail information please refer to spec of chipset.