4.1 Block Diagram Description

The PILA8472 is a printed wire assembly containing circuitry that, when installed inside a standard IBM PC or compatible personal computer, provides data communications in an ethernet environment. It supports additional remote management features when installed in APM or ACPI capable PCs.

Refer to figure 4.0 for the block diagram.

The board contains the following blocks:

Intel 82558 LAN Controller

This device is the core Ethernet controller and provides the following functions:
- CSMA/CD Protocol Engine
- PCI Bus Interface
- DMA engine for movement of commands, status, and network data across PCI.
- Access to EEPROM and flash boot ROM
- Standard MII interface for access to IEEE 802.3u compliant physical layer devices.
- Complete functionality necessary for the 10Base-T and 100Base-TX network connections through a common 10/100Mbps magnetics module.
- Complete set of MII management registers for control and status reporting.
- 802.3u Auto-Negotiation for automatically establishing the best possible operating mode when connected to other 10Base-T or 100Base-TX devices, whether half or full-duplex capable.

EEPROM and Flash

This section includes the optional flash boot ROM and EEPROM which holds the unique Ethernet address and other product configuration data.

Configuration

There are no jumpers or switches. The EtherExpress™ Pro/100+ Dual Port PCI LAN Adapter is totally software configurable.

Digital 21152 PCI to PCI Bridge

This device provides the interface between the two 82558 LAN Controllers and the system PCI bus. Major features include:
- PCI 2.1 Compliant.
- PCI to PCI Bridge V1.1 Spec Compliant.
- Allows 88 bytes of buffering for posted memory write commands.
- Allows 72 bytes of read data buffering in each direction.
- Provides concurrent primary and secondary bus operation.
- Provides arbitration support for four secondary bus devices.

4.1 Block Diagram Description con't

Differences from the PRO/100B with Intel 82555 PHY

- Uses the Intel 82558 LAN controller, which incorporates the Intel 82557 C step and the Intel 82555 10/100 PHY.
- EEPROM address map is specific to PRO/100+ DP with Intel 82558s.

EEPROM Configuration

- The on-board EEPROMS each contain 64x16 bit memory that have a 4 wire serial interface which is used to store the PRO/100+ DP's default configuration. There are multiple ways the EEPROM can be accessed on the PRO/100+ DP. The 82558 automatically reads three words 0xA, 0xB, 0xC and from the EEPRO upon deassertion the PCI RST# signal. These words provide information about the ID PCI Configuration space registers: Device ID, Vendor ID, Subsystem ID, and Subsystem Vendor ID. Software can also access the EEPROMs via the 82558 EEPROM interface.

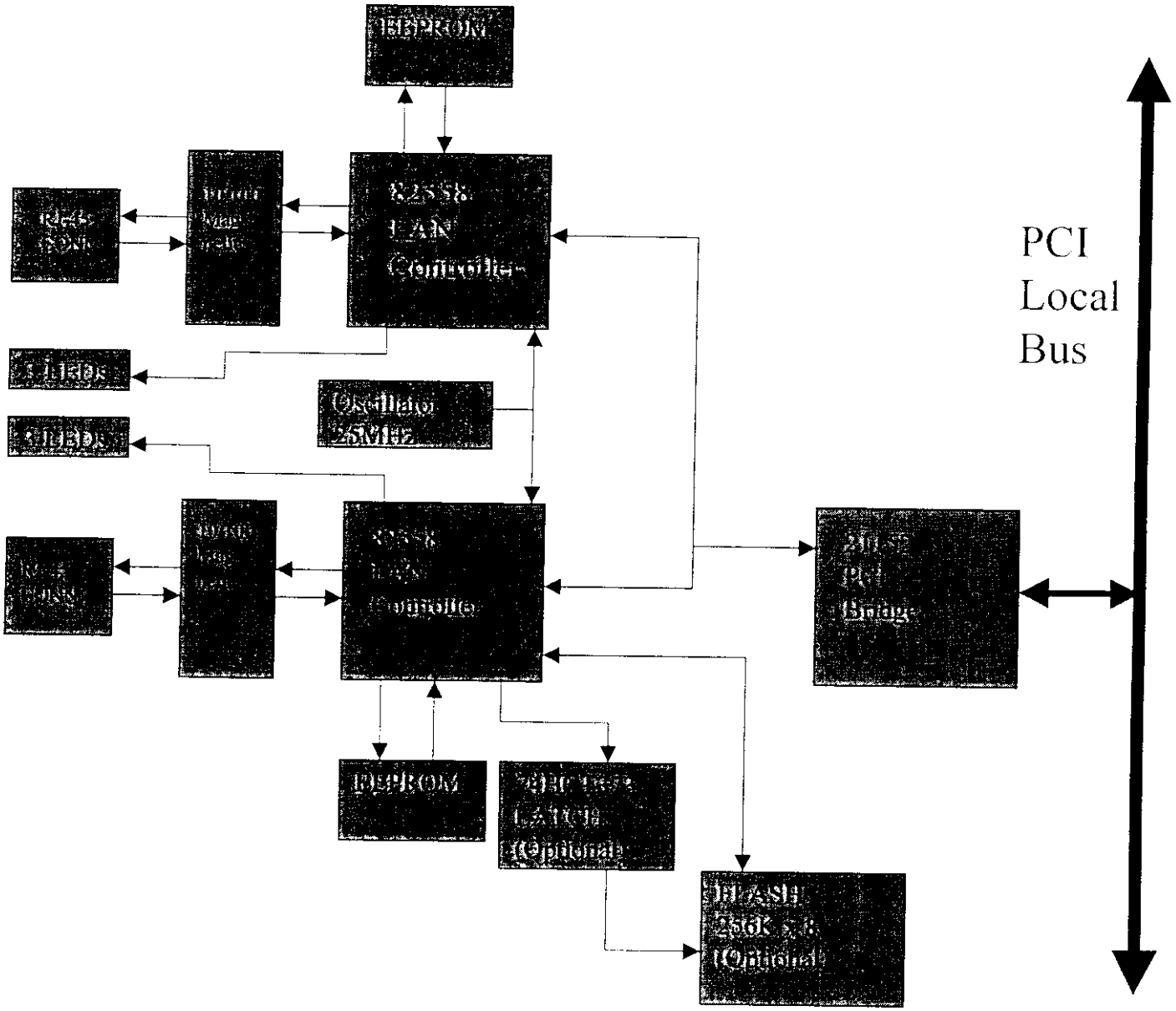
Power Consumption

- The PRO/100+ DP adapter draws power through the PCI interface. It draws from the +5V system and the +12V supply. The +12V supply is used only if the flash memory boot ROM option is installed, and the flash memory is being programmed.

Reliability

- The calculated MTBF (Mean Time Between Failures) for the PILA8472 with Intel 82558s is 1,385,195 hours, or approximately 158 years. The FIT numbers used for this calculation were taken from the MTBF Prediction-Component Default Table of the "Environmental & Reliability Board & System Validation Test Handbook", Intel Document #662394-02.

4.0 Block Diagram of EUT



PRO/100+ DUAL PORT BLOCK DIAGRAM