Multitone TLA 853 - Technical Description

1 CIRCUIT SUMMARY

The TLA 853 message receiver consists of two Printed Circuit Board (PCB) assemblies contained in a plastic case.

The case is constructed in two main parts, the case front and the case back. A cover on the back of the TLA 853 provides access to the battery compartment. The two boards in the case are:

a) The Radio Board which has the Dual Conversion Receiver, the POCSAG Decoder, the 1 Volt regulator and the audio alert output circuit and transducer.

b) The Decoder Board which has the microprocessor, the EPROM, the SRAM, the Liquid Crystal Display Module, the LCD illumination lamp, the vibrate motor and the primary and backup power supplies.

The block diagram of the functional areas of the TLA 853 is shown in Figure 1.

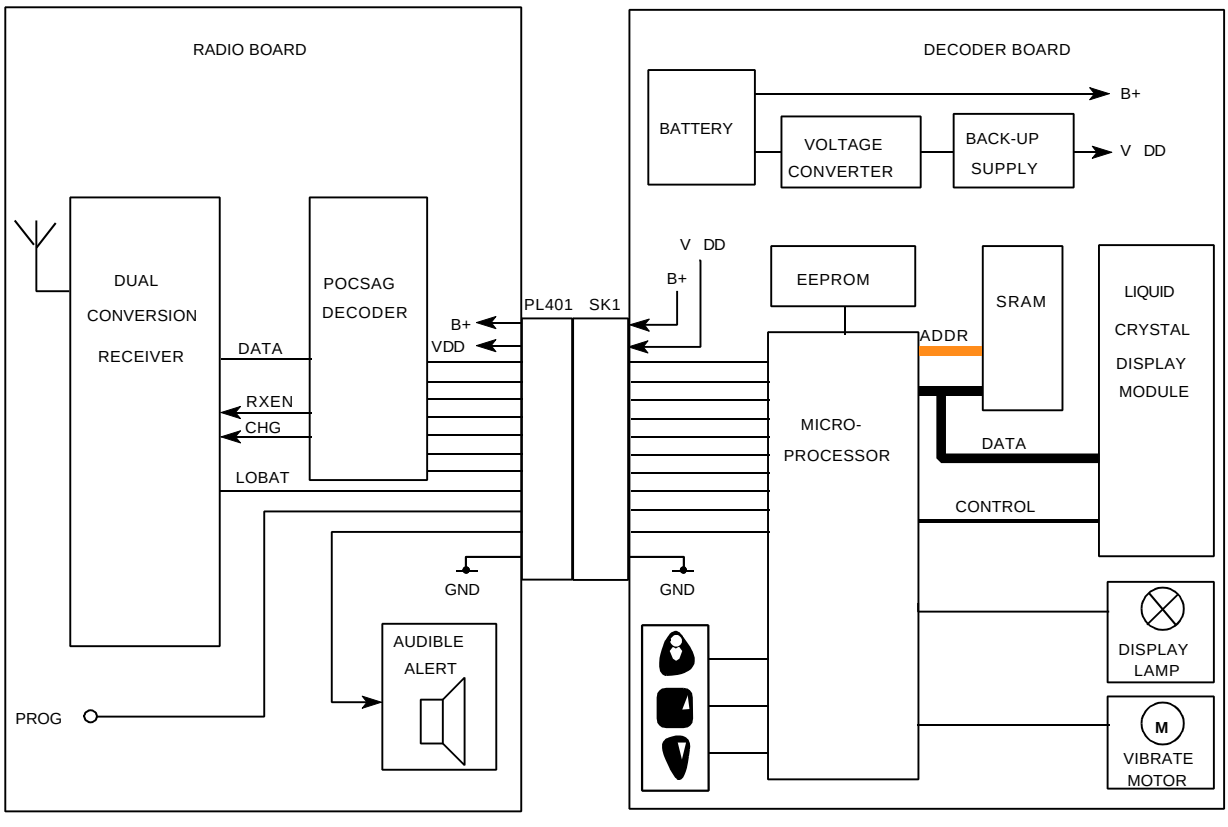

Figure 1: TLA 853 Block Diagram

The RF signal enters the aerial and is fed to the dual conversion superheterodyne receiver. The signal is demodulated from RF to AF, converted to digital format and is then fed to the decoder. This results in the received data activating the memory, display and the selected audible alert or vibrate alert.

To prolong the life of the battery, the receiver operates with battery economy mode. When the unit is in standby mode, the receiver is powered up at regular intervals (equivalent to once per batch) to allow the POCSAG decoder to search for pre-amble. While the unit is receiving preamble on its allocated channel, the receiver remains powered up. This allows the POCSAG decoder to search for a SYNC word. When the SYNC word is found, 'batch lock' is acheived. In batch lock the receiver is only powered up during the allocated frame to allow the POCSAG decoder to search for its address. If the address is found, the receiver stays ON for the duration of the message.

2 DUAL CONVERSION RECEIVER

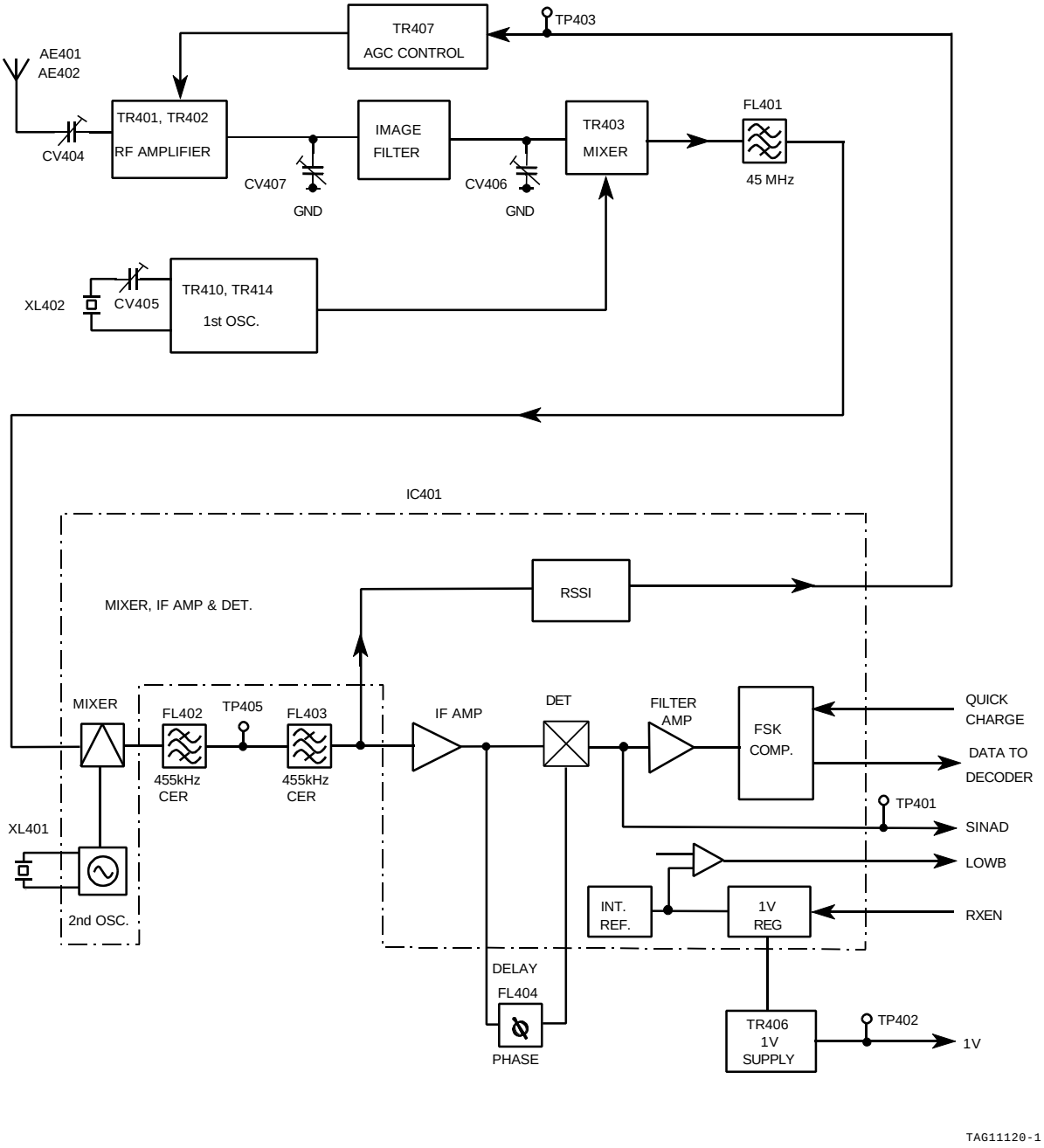

Figure 2: Receiver Block Diagram

The incoming RF signal is received by the aerial AE401/AE402 which is tuned by CV404. Capacitors C401 and C441 provide matching to RF amplifier TR401, TR402. The amplifier, typically, yields a low noise gain of 10dB. R401, R402 and TR407 provide DC negative feedback.

Output from the RF amplifier passes through an image filter which provides these functions:

a) Attenuation of the first image frequency.

b) Attenuation of signals outside the required band.

c) Matches the output impedance of the RF amplifier to the input impedance of the mixer stage.

C406, L401 and CV407 form a parallel tuned circuit with the resonant frequency adjusted for minimum loss at the frequency of operation.

C428, CV406 and L407 also form a parallel tuned circuit adjusted for minimum loss at the frequency of operation. In addition, C428 and L407 form a series resonant circuit with the resonant frequency close to the first image frequency. This gives approximately 40dB of attenuation at the image frequency.

The local oscillator comprises transistor TR410, crystal XL402 and associated components. Frequency adjustment is by CV405. The local oscillator frequency is calculated as follows:

$$fx = \frac{\text{carrier frequency - 45MHz}}{3}$$

where *fx* is the crystal frequency in MHz.

The collector of TR410 is tuned to the third harmonic of XL402 by L411 and C459. The circuit provides the correct Local Oscillator frequency and reduces the level of 2nd, 4th and higher harmonics. The two tuned circuits, L413, C463 and L415, C464 give further filtering of unwanted harmonics.

The mixer circuit, TR403 and associated components, receives the output of the image filter. This is mixed with the local oscillator output to produce a 45MHz product which is selected by the resonant circuit L406, C451. The 45MHz output passes through a monolithic crystal filter, FL401, which has a bandwidth of ±7.5 kHz at the -3 dB points.

The output from FL401 is fed to IC401 pin 24. IC401 is a combined mixer/local oscillator/IF/detector.

The second oscillator runs at 44.545MHz and, with the exception of XL401 and its associated components, is built into the IC. As the second oscillator is not trimmed, small frequency errors are absorbed when tuning the first local oscillator.

The input at pin 24 is applied to the internal second mixer, and is mixed with the second oscillator output to produce a 455 kHz 2nd IF signal at pin 3. The IF signal then passes through two ceramic filters FL402 and FL403 which remove unwanted mixer products and provide further selectivity.

The output from FL403 is split: one output connects through C450 to pin 6 of IC401 and the IF amplifier; the other connects to the Received Signal Strength Indicator (RSSI) circuit in IC401 through C419, R407 and pin 5.

Due to the characteristics of filters FL401, FL402 and FL403, the signal at the input to the IF amplifier has amplitude modulation (AM). The AM must be removed before the signal reaches the detector stage. This is performed by the IF amplifier in IC401 which has very high gain and is designed to limit the amplitude of the signal to remove the AM component and give a 'square' output. C479 and C480 provide de-coupling for the IF amplifier.

The output from the IF amplifier passes to the detector in IC401. This circuit is a Quadrature Demodulator which has two inputs. One input connects directly to the IF amplifier, the other receives the signal from the IF amplifier through a phase delay circuit connected to pins 9 and 10 of the IC. The phase delay depends on the frequency of the IF signal and is 90 degrees at the centre frequency of the unit's allocated channel. The phase shift is provided by ceramic discriminator FL404, capacitor C426 and resistor R416.

The RSSI circuit in IC401 provides an Automatic Gain Control (AGC) signal for the receiver. The circuit detects the received signal strength and gives a DC current out. R407 sets the level at which the circuit starts to operate. The value of 68 kilohms sets it to approximately 16dB above the noise floor. The DC output from pin 22 of the IC connects to the AGC control circuit. When there is no RSSI output, transistor TR407 is biased on and keeps the RF amplifier at full gain. At strong signal levels the output from the RSSI causes TR407 to cut off gradually, thus reducing the gain of the RF amplifier. C437 determines the rise and fall times of the AGC.

The output from the detector stage, pin 11, gives an audio output to TP401. This test point is used in the final stages of production to align the receiver circuits. TP401 is also used to program the decoder section of the unit. Pin 11 of IC401 also connects through R425, R429 and R428 to pin 12. These resistors together with capacitors C448, C483, C484 and the internal filter amplifier of IC401 form the data filter; a unity-gain, low-pass filter which reduces high frequency noise.

The output of the data filter connects internally to the FSK Comparator. The data output of the comparator, from pin 18, connects to the POGSAG decoder, IC402, pin 4. A logic signal from IC402, pin 2 to IC401, pin 16 controls the Fast/Slow charge of the FSK Comparator. When the receiver starts a preamble search, the logic level is high and the circuit is set to Fast Charge to allow the reference voltage for the comparator to be set to the mean dc level of the demodulated signal. After a fixed time the logic level at pin 16 is set low which sets the comparator to normal operation.

3 DECODER

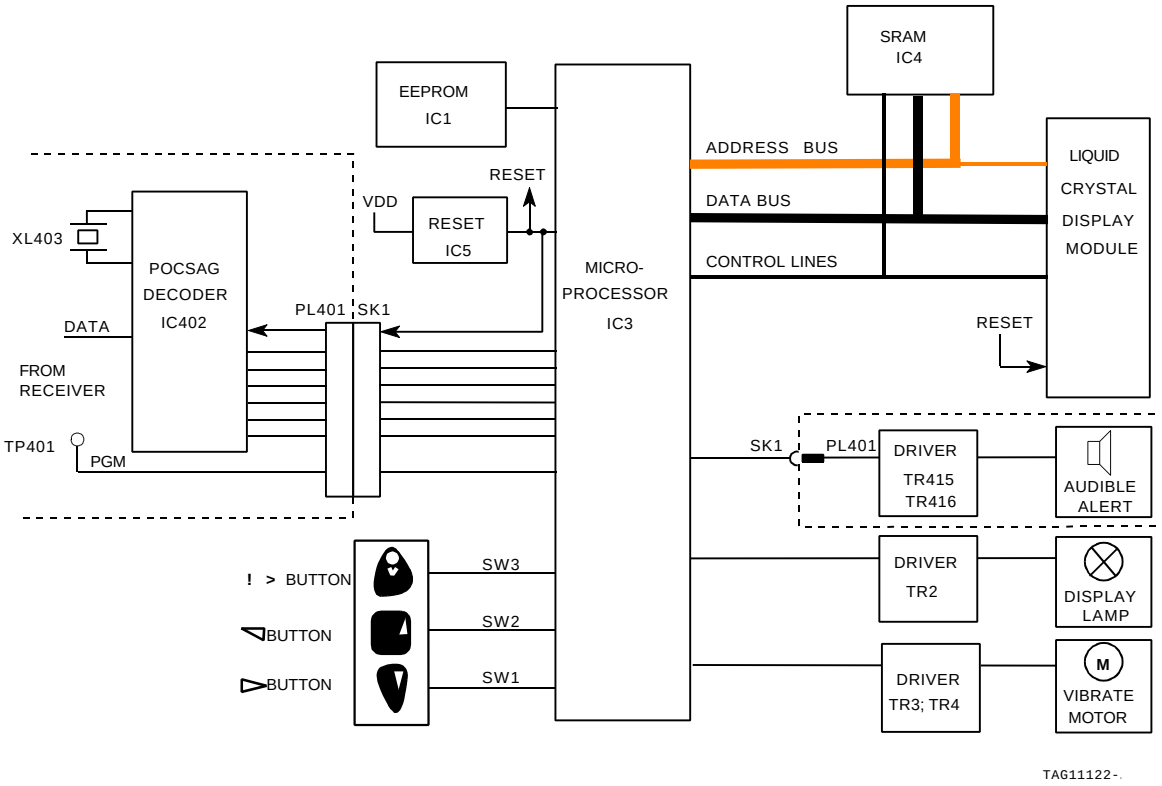

Figure 3: Decoder Block Diagram

General

The Decoder comprises the POCSAG decoder, Microprocessor, EEPROM, SRAM message memory and switches, plus support components and a separate LCD module. The signal from the receiver is processed by IC402, the POCSAG decoder, and the decoded data passed to the microprocessor. The microprocessor stores the information in the SRAM, IC4, before activating the selected alert and sending the message data to the LCD module for display. The EEPROM holds information applicable to the unit.

POCSAG Decoder

The POCSAG decoder, IC402, is installed on the Radio Board of the unit and connects to the microprocessor, IC3, through PL40I / SK1. Pin 4 of IC402 receives the data signal from IC401. IC402 decodes the information and sends it, four bytes at a time, to the microprocessor, IC3. IC402 uses the SCK clock pulses from IC3, pin 59, to transfer the data on the SDO line, IC402, pin 13.

When no signals are received by the unit, the system goes into a standby mode to reduce power consumption. In this mode a pulse from IC402, pin 1 (BS1), sets the receiver circuits ON at regular intervals for a preamble search. If a preamble signal is received, followed by a valid address, a signal is sent from IC402, pin 15 (ATTN) to alert the microprocessor.

Pin 9 (CLK0) provides clock pulses to operate the microprocessor while it is in standby mode.

Pin 11 (AREA) goes high when a valid signal is received.

Pin 14 (SDI) receives program information from the microprocessor.

Pin 2 (BS2) controls the 'fast charge' operation of the FSK comparator in IC401.

Microprocessor

The microprocessor controls the functions of the unit. A 4.19MHz clock controlled by XL1, provides the basic timing for the system.

Data received from IC402 is processed by the microprocessor and stored in the SRAM chip, IC4. The microprocessor then causes the selected Alert to operate and sends the message to the LCD module for display. Outputs from pin 5 (LCD-CS), pin 39 (AD17), pin 38 (AD16) and pin 60 ($\overline{WR}$) control the transfer of data to the LCD module on the databus. Outputs from pins 2 and 7 control the operation of the audio alert and the vibrate motor.

IC3 also controls the internal functions of the system, displaying the symbols and changing the modes when selected by the three buttons on the front of the unit.

EEPROM

The EEPROM (IC1) holds information applicable to the unit, such as: Serial Number; RIC codes; Radio parameters. The information is sent to the microprocessor through the serial data link, pins 62, 63 and 64.

SRAM

The SRAM (IC4) is a 256 k device which can store up to 32 k of 8-bit information. Address lines AD00 through AD14 and control lines RAM-CE and $\overline{WR}$ from the microprocessor, control the flow of data in and out of the device on the databus.

LCD Module

The LCD Module is a single device which contains all the necessary circuits to produce the alpha-numeric characters and the symbols for the integral 2-line display. Address lines AD16 and AD17 and control lines LCD-CS and $\overline{WR}$ from the microprocessor, control the flow of data to the device on the databus.

R14 and R20, connected to pins 33 and 34, are feedback resistors for the module's internal oscillator.

C20 and C21 (pins 38 through 41) are part of the internal DC/DC converter of the module's negative bias supply.

R11, R12, R13, C17 and C22 through C25 are part of the circuit which controls the voltage to the LCD driver.

Display Illumination

A single miniature lamp is used to illuminate the LCD display. The lamp is selected ON or OFF using the buttons on the front panel. The 'Lamp ON/OFF' signal, which comes from pin 8 of the microprocessor, controls transistor TR2 in the lamp circuit.

Alerts

a) **Audible Alert (Beep)**

The transducer, SP401, and the driver circuits TR415 and TR416, are located on the Radio Board. The audible alert signal from IC3, pin 2 connects to TR415 through SK1/PL401 pin14. The alert can be selected ON or OFF using the buttons on the front panel.

b) **Vibrate Alert**

The vibrate motor is operated by transistors TR3 and TR4 on the Decoder Board. The vibrate alert signal from IC3, pin 7 connects to pin 1 of TR3. The alert can be selected ON or OFF using the buttons on the front panel.

3 POWER SUPPLIES

The primary power supply for the unit is a single 1.5 Volt, AAA battery (BAT1). The supply from the battery (B+) connects directly to the lamp and vibrate motor circuits that require relatively high currents. B+ also connects to the Radio Board through SK1/PL401, pin 9 and to the voltage converter, IC6, on the Decoder Board.

IC6 and its associated components supply the +3.1 Volts (VDD) for the unit. In addition, the circuit charges the backup supply (BAT2) through resistor R6. Double diode D2 provides isolation for the two circuits.

IC5 monitors the voltage of V_{DD} and resets the decoder circuits if the voltage drops to a level that would cause data corruption.

Transistor TR1, connected to pins 6 and 15 of IC3, detects the battery voltage. If BAT1 is removed, the drop in B+ causes transistor TR1 to switch OFF which sets the microprocessor to low-current mode. In this mode BAT2 supplies sufficient power to keep the microprocessor and the SRAM operational for up to 60 minutes.

The 1 Volt supply for the receiver circuits is provided by transistor TR406 and its associated components. The circuit is a series regulator and is maintained within specification by a control circuit in IC401.