Chapter 1
Product Description

1.1 Introduction

This manual contains information and procedures for the installation, operation, and maintenance of the EHP19 Integrated Power Transceiver (IPT).

1.2 Scope of Manual

This manual is intended for use by service technicians familiar with similar types of equipment. It contains service information required for the equipment described and is current as of the printing date. Changes which occur after the printing date may be incorporated by a complete manual revision or alternatively as additions.

The manual is organized into the following chapters:

- Chapter 1 - Product Description
- Chapter 2 - Installation
- Chapter 3 - Operation
- Chapter 4 - Maintenance
- Chapter 5 - Specifications and Drawings

1.3 Functional Description

The IPT is a high efficiency RF single channel power amplifier with an internal analog pre-distorter for use with the Radio Base Station (RBS) digital pre-distorter system for RF output linearity. The IPT has an operational bandwidth of 60 MHz from 1930 MHz to 1990 MHz producing a typical output of 60.2 watts (47.8 dBm). The IPT is shown in Figure 1-1. Detailed functional and physical specifications for the IPT are listed in Chapter 5.

1.3.1 RF Interface

The IPT RF interfaces consist of the TX OUT port located on the top of the IPT front panel and the RX0 and RX1 ports located on the bottom of the IPT front panel.

1.3.2 Main Transceiver

The following circuits are part of the main transceiver section.

1.3.2.1 Customer Interface/CPRI Input

The incoming serial data stream from the customer interface (DRIC) front panel connector is applied to a Serialiser-Deserialiser (SerDes), converted into a parallel format and decoded. The customer interface also includes processing of the frame alignment, byte alignment and chip alignment, including delay adjustment. A clock acts as the frequency reference for the entire transmitter. The clock is extracted from the incoming signal using a phase locked loop (PLL). There are two outputs

from this block: control data and signal data. The control data determines parameters such as channel frequencies, signal ramp-up/ramp down and transmit power level. These functions are implemented in a Field Programmable Gate Array (FPGA).

1.3.2.2 Digital Up Converter (DUC)

The DUC modulates individual symbol streams from the signal data stream on to baseband carriers and applies root-raised cosine channel filtering. This function is implemented on an Application-Specific Standard Product (ASSP).

1.3.2.3 Crest Factor Reduction (CFR)

The CFR function is implemented in the FPGA. The CPR varies the DUC signals to reduce the peak-to average power of the transmit signal to allow the P-Mod to operate with higher efficiency ensuring the transmit signals stay in the occupied bandwidth/spectral mask limits.

1.3.2.4 Data Interpolation (INT)

The interpolation function, which is implemented in the FPGA, changes the sampling rate up to 92.16 Msps.

1.3.2.5 Digital Predistortion (DPD)

The DPD function, which uses an ASSP DPD engine, and a Digital Signal Processor (DSP), processes the forward path signal to compensate for the non-linearities in the forward path. The DPD function ensures that the transmitter operates at the correct power level over variations in supply voltage, load impedance, temperature and aging.

The DPD function also provides compensation for imperfections in the AUC such as differential delay, I-Q amplitude and phase balance and DC offset/carrier leakage. the linearisation lock function monitors the operation of the signal and turns off the transmitter if the system is not functioning correctly. The digital output signal from the DPD engine is converted back to an analog signal in a high-speed digital-to-analogue converter (DAC).

1.3.2.6 Analog Up Converter (AUC)

The AUC uses a direct-conversion architecture (I-Q modulator) to transform the I-Q baseband signals from the DPD up to the operating RF frequency.

1.3.2.7 Observation Path (OBS)

The OBS act as a high performance radio receiver tuned to the RF transmit frequency. The OBS converts the sampled RF transmit signal to a VHF intermediate frequency where it is sampled by a high-speed analogue-to-digital converter (ADC). The output of the ADC is fed to the DPD block, compared with the drive signal and then used to update the parameters in the DPD algorithms running on the DSP.

1.3.2.8 Clock Module

The FPGA high-speed serial interface (SerDes) extracts a timing clock from the incoming data stream, the transmit frequency stability depends on the accuracy of the incoming input signal. The recovered clock is used to synchronize a crystal oscillator used as a clean frequency reference for the timing functions on the TRx board (RF LOs, DAC and ADC clocks, Tx, Rx and lineariser signal processing clocks).

The reference is used as a direct reference for the RL local oscillators. Except for the digital clocks, the reference is passed to a PLL VCO, which is then subdivided. All RF PLLs include lock-detect signals to allow the transmitter to be turned off if there is a fault with a PLL.

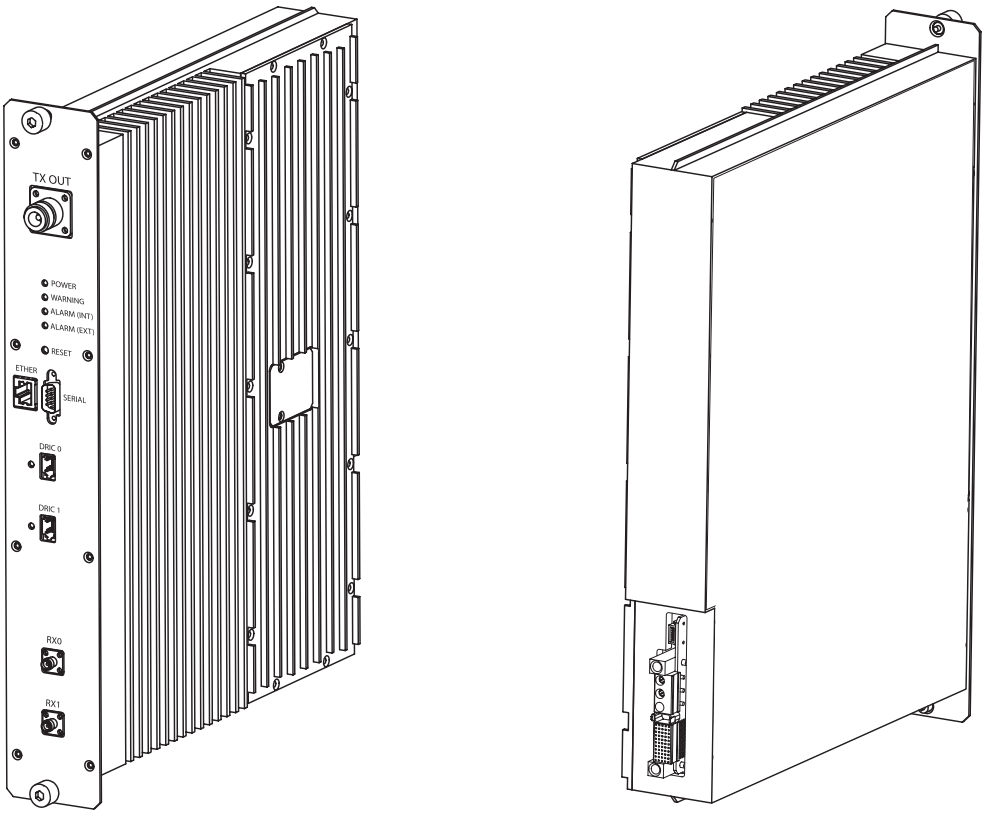

Figure 1-1 Integrated Power Transceiver Front and Rear Isometric View

1.3.3 Power Module

The P-Mod is a multi-stage amplifier, which amplifies the low level signal from the AUC up to the RF output power level of +47.8 dBm (60.25 W). The P-Mod consists of a two-stage pre-driver, a driver amplifier and an output stage. The bias currents are electronically calibrated during factory test and bias setting and temperature compensation are controlled by a master control unit on the P-Mod PCB. The P-Mod also includes a directional coupler, which allows a sample of the transmit signal to be fed to the observation path and an isolator, which protects the P-Mod from damage or potential oscillation under adverse RF load conditions. An RF switch allows either the observation signal or the reflected power from the antenna connector, measured at the third port of the isolator, to be passed to the TRx

1.3.4 Front Panel

The front panel contains a RESET switch and four status and alarm LEDs.

1.3.5 Operational States

The IPT has three operational states: Operational, Disabled and Not Ready.

The IPT remains in the Not Ready state during start-up until all parameters are met for the IPT to become operational.

The IPT is normally in the Operational state: no faults are present, the IPT internal temperature is within limits, appropriate DC power is applied, and the IPT is producing RF output. The green operational (O) LED on the Man Machine Interface is lit.

The Disabled state is ordered from the RBS (if there is a fault in the IPT or in other RBS units) or entered automatically when a critical hardware error is detected by the IPT. The Disabled state causes the IPT to shut down, but it can be enabled by the RBS if the fault is cleared.

1.3.6 State Transitions

The IPT has five state transitions: Reset, Status OK, Alarm, Disable, and Enable.

Reset initiates the Not Ready state. This state is entered when power is initially applied to the IPT or from a dedicated reset signal from the RBS to the IPT.

Status OK is entered from the Not Ready state and initiates the Operational state when commanded by the IPT

Alarm initiates the Disabled state from the Operational state if the IPT detects a hardware or temperature fault. The RBS reads the potential fault cause for fault logging.

Disable is ordered from the RBS to force the IPT to go to the Disabled state and shut down. Power on of the IPT after a Disable can only be ordered by the RBS through a RESET command.

Enable is ordered from the RBS to power on the IPT after it has been disabled. The IPT enters the Operational state after checking status and temperatures and re-perform start-up if required.

1.3.7 DC Power (DC)

DC power (-48 Vdc nominal) is supplied by the RBS to the IPT through the rear mounted connector. Refer to Table 1-1 for a description of the DC connector inputs.

Table 1-1 DC Power Connections

Pins	Signal Name	Description
1,2	GND (-48V_RTN)	DC plus (isolated from amplifier chassis)
3,4	-48V	DC minus (isolated from amplifier chassis)
5,6	GND (NC)	Not connected

1.3.7.1 Power Supply

The power supply assembly contains two subassemblies. The DC/DC converter produces regulated +28 Vdc, +9 Vdc and +6.5 Vdc from the -48 Vdc supply for the IPT internal supply. The low voltage supply uses the +6.5 Vdc from the DC/DC converter to provide regulated 3.3 Vdc, 1.8 Vdc and 1.5 Vdc reference level supplies.