Technical Report

MICROWAVE DATA SYSTEMS
MODEL 9710A
DATA TRANSCEIVER

FCC ID: E5MDS9710-1

Microwave Data Systems
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1.0 General Equipment Information

This device is marketed and manufactured by Microwave Data Systems as the MDS 9710 Data Transceiver and is intended primarily for use in Point-to-Multipoint networks. The MDS 9710 is used as the remote radio in the multiple points in the network which communicate with a master station.

1.1 Summary of RF Parameters

Transmitter

Type:	Synthesized, 12.5 kHz steps
Frequency Range:	806 to 940 MHz.
Power Output:	37 dBm maximum (5 Watts)
Crystal frequency:	16 MHz TCXO

Receiver

Type:	Double conversion superheterodyne
Frequency Range:	806 to 940 MHz.
1st Local Oscillator Range:	723.8 to 857.8 MHz.
First Intermediate Frequency:	82.2 MHz.
Second Intermediate Frequency:	455 kHz.
Crystal Frequencies:	16 MHz, 81.745 MHz.

1.2 Construction Details

The MDS 9710 Data Transceiver consists of a transmitter and receiver constructed on a common printed wiring board assembly, sharing many common circuits. The transceiver board is mounted within a die-cast aluminum housing. A die-cast aluminum top cover completes the enclosure assembly, providing a well-shielded enclosure.

Power, interface and antenna connections are made via connectors on the front face of the transceiver package. DC power may be supplied to the transceiver from any suitable DC source capable of supplying 13.8 VDC nominal at a maximum of 2.5 Amperes. The DC power source should be current limited or have a protective fuse or circuit breaker.

2.0 Description of Device Operation

2.1 General Operation

The MDS 9710 Data Transceiver is a narrow band radio designed to operate on 12.5 kHz. channels, meeting the requirements of FCC Part 2, FCC part 15 and FCC Part 90.

2.2 Description of Circuit Functions

The following is a summary of the operation of the MDS 9710 Transceiver. Refer to Figure 1, the block diagram, and to the schematics, to follow the discussion.

2.2.1 Receiver

Receive Front End

Connector J301 on the main PWB board conducts the RF signal from the front panel antenna connector to the antenna switch network. In the receive mode, one port of the antenna switch conducts the receive signal to the input of helical filter FL300.
The output of FL300 is fed to RF amplifier Q302, whose output goes to helical filter FL302. Each helical front-end filter has a 25 MHz 1 dB bandwidth, and are down approximately 20 dB at ±100 MHz. The output of FL302 output goes to M301, a double-balanced mixer whose local oscillator injection voltage is derived from the VCO U307.

High IF

The 82.2 MHz High IF signal from M301 enters IF amplifier transistor Q301, whose output goes to FL308 and FL303, a dual SAW filter which provides part of the IF selectivity of the receiver. The output of FL303 is connected to U302, which contains the Low IF amplifier and other functions.

Low IF

U302 contains several circuit sections: mixer, oscillator, IF amplifier / limiter, quadrature detector and meter drive. The oscillator section of U302 uses crystal Y301and associated components to set the second oscillator frequency at 81.745 MHz.

The 455 kHz output of the second mixer is fed to a ceramic filter set consisting of FL307 and FL309. This filter set provides the main adjacent channel selectivity of the receiver.

The output of FL309 is fed to the limiter amplifier input pin of U302. The limiter output is fed to a quadrature detector circuit tuned by FL301; audio recovered from the detector appears on Pin 8 of U302.

A secondary output of the IF subsystem at Pin 5 of U302 gives a received signal strength indication (RSSI) voltage.

Digital Signal processing

Audio processing

The unfiltered recovered audio from the IF detector passes through amplifier U201 to an A/D converter U205 and then processed by the DSP U202 to decode the digital information.

RSSI Processing

The unfiltered RSSI from the IF detector passes through a low pass filter to a monolithic internal A/D converter built within the 68HC11 micocontroller U101. A scaled version of the RSSI signal is output though the D/A converter U203 connected to the DSP U202.

2.2.2 Power Supply

The + 14 volt (nominal) DC input appears when an external power source is connected to J103. From J1, the +14V is conducted to the internal transceiver circuits through F1, a 4 ampere board-mounted self-resetting poly fuse. CR112 is a transient voltage suppresser on the + 14 VDC primary power input. It protects against a reverse polarity condition. U105 is a switching regulator that provides + 5.6 volts for transceiver circuits.

- U102 regulates the + 5.6 volts down to + 5 volts which supplies power to the microprocessor and all of the CMOS logic.
- U204 regulates the + 5.6 volts down to + 3.3 volts which supplies power to the DSP and A/D converter
- Regulator U306 provide 10 volts for all of the receiver low noise amplifiers and VCO circuitry.
- The power amp runs directly off the 14 volt supply.
- U310 regulates the 5.6 volts down to 5 volts for the TCXO and synthesizers.

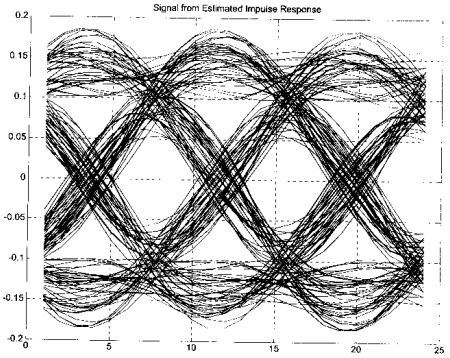
2.2.3 Transmitter

CPFSK Modulation Process

The transmit audio is generated internal to the DSP with an FIR filter. The DSP drives a D/A converter U203 which provides a control voltage to the VCO U307 and the TCXO Y302. This process creates the CPFSK (continuous-phase frequency shift keying) modulation.

Although the data rate is 9600 bits/second, the average signaling rate is less than half this value. Root-duobinary signal coding, ensures a maximum signaling rate of 4800 b/s. However, this would only occur during a run of alternating 1s and 0s. However, the MDS 9710 employs a data scrambler circuit which converts an alternating 1,0 pattern into a pseudo-random bit pattern. Any other bit pattern is likewise scrambled into a pseudo-random bit pattern.

Further insight into the modulation rate can be seen from a consideration of the two possible extremes. The scrambler could, over a limited time, produce a run of all 1s or all 0s, which would be a signaling rate very close to zero (DC). At the other extreme, the scrambler could produce an alternating pattern of 1s and 0s for a limited time. This would be a signaling rate of 4800 b/s. The two extremes are at the tails of the probability distribution, and are very unlikely. The most likely situation is at the mean of 2400 b/s. Since the likeliness relates directly to the time spent in such a condition, the power spectral density is likewise directly related, and behaves as if the signaling rate is 2400 b/s.



In addition to the above considerations, the scrambled signal passes through a digital low-pass filter with a 3 dB point of 4800 Hz. This means that when a brief run of 4800 b/s signal occurs, *it will deviate the radio to only one-half of the peak deviation.* This has a direct effect on reducing the occupied bandwidth of the emissions of the radio.

The accompanying “eye” diagram from a Matlab simulation illustrates the effect. The runs of 2400 b/s or less deviate the transmitter fully, while runs of 4800 b/s deviate to only half full deviation. Arbitrary units are used on the axes.

Exhibit B, the Laboratory Test Report, shows a measured value of occupied bandwidth of 9.28 kHz when operating at 956 MHz with a measured peak deviation of 3.54 kHz. Under these conditions, the transmitted spectrum is contained within the limits of emission mask requirements of FCC Part 101.111(5) as demonstrated by the spectrum plots given in Exhibit B.

It should be evident that the modulation process in the MDS 9710 is complex and statistical in nature, and does not easily translate to the formulas for calculation of necessary bandwidth given in Part 2.202.

Results using FCC Part 2.202(g) III-A (1) with the measured value of peak deviation, and the following substitutions of values, are shown below.

Formula
$B_n = 2M + 2Dk$

If we base the calculation on runs of 2400 b/s with full deviation of 3540 Hz, we get:

M = 2400 b/s = 2400 Hz.
D = 3540 Hz
k = 1
then,

$B_n = 2(2400) + 2(3540) = 4800 + 7080 = 11{,}880$ Hz. = 11.8 kHz.

If we base the calculation on runs of 4800 b/s with one-half the full deviation of 2850 Hz, we get:

M = 4800 b/s = 4800 Hz.
D = 3540/2 = 1770 Hz
k = 1
then,

$B_n = 2(4800) + 2(1770) = 9600 + 3540 = 13{,}140$ Hz. = 13.14 kHz.

As expected, calculation from the simple formula of Part 2.202(g) III-A (1) gives a necessary bandwidth value with considerable error compared with the measured value of 99% occupied bandwidth.

Based on all of the above measurements and considerations, we have requested a necessary bandwidth on the emission designator of 11K2, this value being the maximum authorized bandwidth of 11.25 kHz for 12.5 kHz channel spacing in this operating frequency range.

Transmit Power Amplifier

The power amplifier chain of the transmitter section consists of U312 and U304. U312 is a buffer amplifier biased by the + 5v supply. The output of U312 is input to a five watt power amplifier U304.

The RF output of U304 is fed through a directional coupler and low pass filter to the antenna diode switching network.

Antenna Switch

The antenna switch consists of a quarter wave section constructed with microstrip line on the PCB and pin diodes. During the transmit mode, diodes CR301 and CR302 are biased on by U305. When the diodes are conducting, CR302 provides a low impedance path for the transmit signal to the antenna port and CR301 shorts out to ground. With CR301 and CR302 on, the network acts as the equivalent of a quarter wave transmission line with no RF current flowing through quarter wave microstrip line. With CR302 and CR301 on, RF energy is prevented from appearing at the input of FL300.

2.2.4 Processors

Microprocessor / FLASH Memory

The microprocessor U101, controls many of the on-board functions of the transceiver. It runs a predetermined routine that controls all of its pin functions; this routine is stored in FLASH memory, U104. All programmable functions and values are stored by the microprocessor in EEPROM in the microcontroller. This includes operating parameters such frequency, CTS delay time/mode, as well as model and factory serial numbers. The microcontroller uses the 16 MHz system clock as its clock source.

Digital Signal Processor (DSP)

The DSP controls all of the real time modem functions including FIR filtering, converting/writing to D/A, reading from A/D and running the asynchronous RS-232 interface. It runs a predetermined routine that controls all of its pin functions. The routines are downloaded from the microcontroller's FLASH memory when the radio is powered up. All programmable functions and values are stored by the microprocessor in EEPROM in the microcontroller. These are used when the radio is powered up. These include operating parameters such as receive FIR coefficients and application interface baud rate. The DSP uses the 16 MHz system clock as its clock source.

2.2.5 PLL/Synthesizers

Two independent PLL circuits generate the High IF mixer local oscillator and transmitter local oscillator.

The temperature compensated 16 MHz crystal oscillator X302 (TCXO) sets the reference frequency for the phase-lock loop (PLL) circuits. The TCXO's output is run to U308 the transmitter synthesizer IC and U300 the receiver synthesizer IC.

U300 and U308 are CMOS PLL synthesizers consisting of phase detectors, programmable reference dividers, programmable feedback dividers, and prescalers. Data input is serially loaded from the microcontroller U101; this data consists of binary coded numbers representing the reference and feedback (VCO RF sample) divider ratios required to produce the final transmit and receive frequencies. The reference divider is programmed only on power-up, with a power reset or with a PLL out-of-lock condition. The feedback divider value changes according to the transmit/receive frequencies sent from the microcontroller.

The phase detector output of U300 and U308 are fed to the respective VCO tuning input through an R-C loop filter. U301 and U307 are self-contained voltage-controlled oscillator (VCO) assemblies whose outputs are amplified by buffer amplifiers U312 and Q303 respectively.

2.2.6 RS-232 Data Interface

U106 and U206 are RS232 line driver/receiver integrated circuits. They have internal +5 volts to +10/–10 volt converters that allow them to provide a true RS-232 compatible output. Transient protection for the six RS-232 I/O lines is built into the RS-232 driver.

2.2.7 LED Indicators

LED indicators are provided to visually signal the state of the transceiver. U108 and U109 are inverting buffers which provide drive to the LED indicators.

3.0 Block Diagram

Block Diagram of MDS 9710 Data Transceiver:

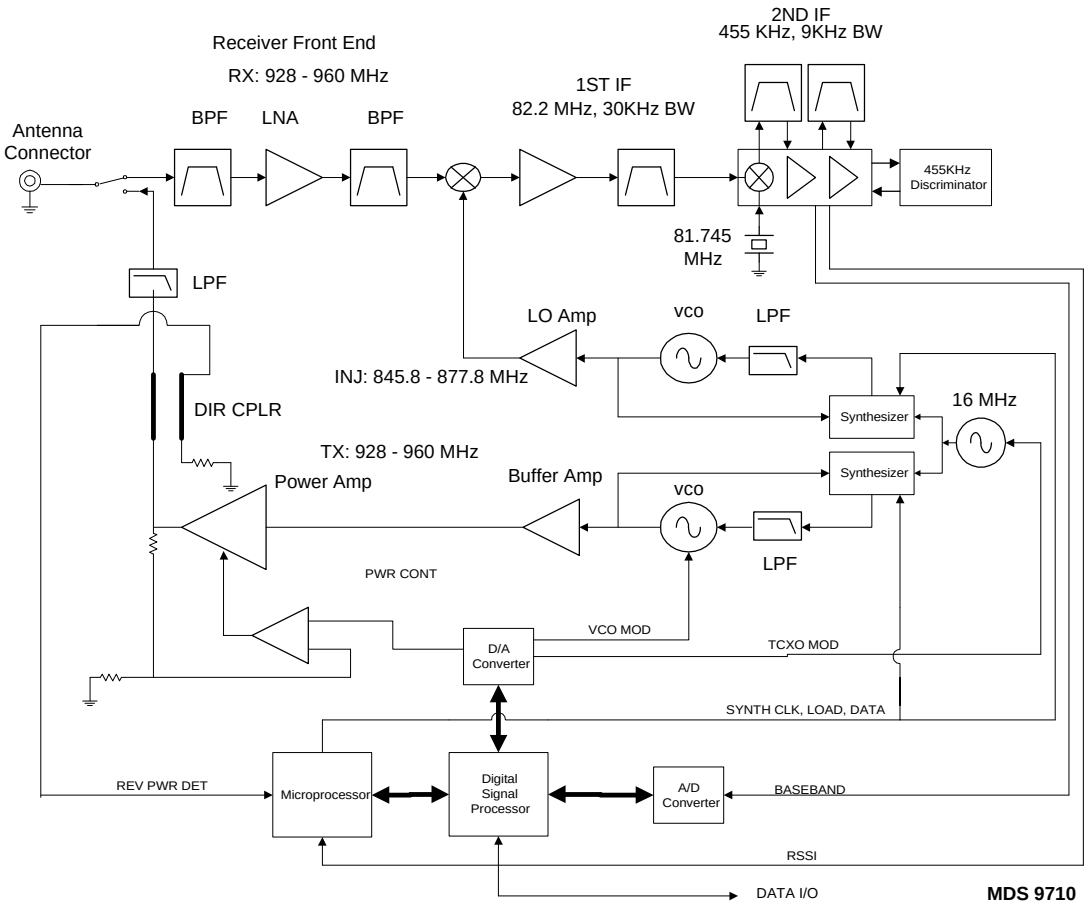


Figure 1

3.5 Schematic Diagrams (3 sheets)

(See the following 3 pages)

4.0 Design Considerations for EMC

The design of the MDS 9710 Data Transceiver incorporates good design practices developed by MDS during our 10+ years of radio design and manufacturing.

The most important design technique to minimizing both unwanted radiation and undesired susceptibility is in the proper design and layout of the printed circuit board. A 6-layer printed circuit board is used, with critical signal and oscillator traces run on internal layers between layers acting as ground planes. This stripline approach ensures minimum radiation from signal traces, and likewise protects them from induced voltages from external field sources during susceptibility testing.

Almost all components are surface mount, using the smallest outline packages available, which minimizes radiation from components, and allows for very short connecting traces. The enclosed area of any current loops is minimized as well, to reduce radiation. All components are mounted on the top surface of the printed circuit board.

Critical oscillator circuits are enclosed in a shield assembly on the top of the printed circuit board. The bottom side of the printed circuit board under the shield is a continuous copper surface connected to the top shield by plated through copper vias ensuring a good shield connection.

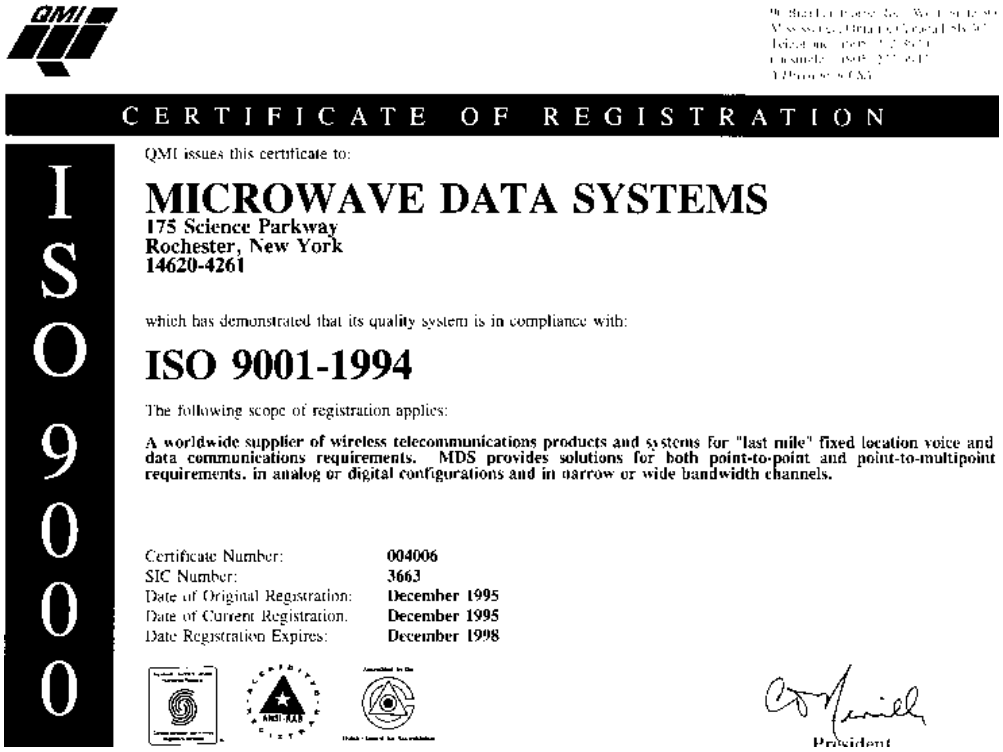
Input and output data and control lines appearing on the DB-25 connector, J101, are individually bypassed with 0.001 uF capacitors. Input and output lines appearing on the RJ-11 connector, J102, are similarly bypassed.

The transceiver enclosure is a two-piece, self-complementary cast aluminum shell. A metal knit RFI gasket is used to ensure an RF-tight seal between the two halves. This all-metal enclosure provides excellent RF shielding.

The MDS 9710 has been tested and shown to comply with all applicable requirements of FCC Parts 2, 15 and 90.

5.0 Quality System at Microwave Data Systems

Microwave Data Systems has been registered to ISO 9001 since December 1995. A copy of our Certificate of Registration is shown below.



CERTIFICATE OF REGISTRATION

ISO 9000

QMI issues this certificate to:

MICROWAVE DATA SYSTEMS
175 Science Parkway
Rochester, New York
14620-4261

which has demonstrated that its quality system is in compliance with:

ISO 9001-1994

The following scope of registration applies:

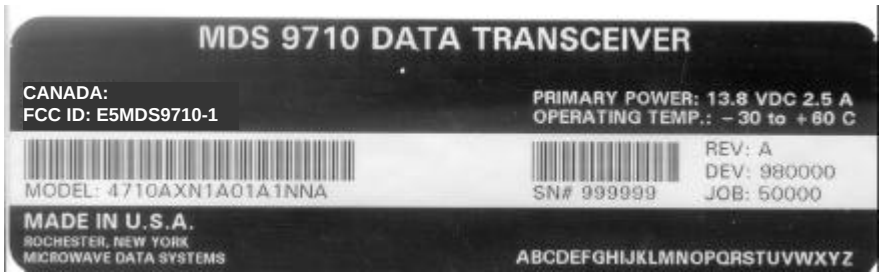
A worldwide supplier of wireless telecommunications products and systems for "last mile" fixed location voice and data communications requirements. MDS provides solutions for both point-to-point and point-to-multipoint requirements, in analog or digital configurations and in narrow or wide bandwidth channels.

Certificate Number:	**004006**
SIC Number:	**3663**
Date of Original Registration:	**December 1995**
Date of Current Registration.	**December 1995**
Date Registration Expires:	**December 1998**

President

6.0 Product Label

The label which will be used on the MDS 9710A Data Transceiver is shown below. This label will be used after Type Acceptance has been granted by the FCC.



Location of identification label:
(Also see Photograph 2)