2.0 Description of Device Operation

2.1 General Operation

The EL-705 Data Transceiver is an OEM narrow band radio designed to operate on 12.5kHz channels, meeting the requirements of FCC Part 90 and FCC Part 15.

2.2 Summary of RF Parameters

Transmitter

Type:	Synthesized, 12.5kHz steps.
Frequency Range:	450 to 470MHz.
Power Output:	+33dBm, nominal.
Master Clock Reference:	16MHz TCXO, +/- 1.5ppm stability.

Receiver

Type:	Double conversion superheterodyne.
Frequency Range:	450 to 470MHz.
1st IF Frequency:	45MHz
1st LO Range:	Low-side injection 405 to 425MHz, 12.5kHz steps.
2nd IF Frequency:	450kHz.
2nd LO Frequency:	Low-side injection 44.550MHz, fixed.

2.3 Description of Circuit Functions

The following is a summary of the operation of the EL-705 Data Transceiver, and is referenced to the block diagram shown in Figure 1.

2.3.1 Receiver

Receiver Front End

RF for both transmit and receive is connected to the OEM transceiver board thru the BCN antenna connector J201. In the receive mode, the received signals first pass thru a 5th order lumped-element harmonic lowpass filter. This filter suppresses all signal energy above the receive band of interest. Following this lowpass filter, the received signals are passed thru an antenna switch which is in the off mode in receive and directs the signal energy to a 3-section helical bandpass filter, FL200. The output of FL200 is then passed thru a low-noise RF preamplifier, Q201, and then thru another 3-section helical bandpass filter, FL201. The combination of both 3-section helical filters has approximately a 20MHz bandwidth, suitable to cover the 450 to 470MHz band and provide sufficient rejection of the undesired out of band signals.

The filtered and amplified received signals are then passed thru to a double-balanced IC mixer, U301 that, in conjunction with the 1st local oscillator signal, downconvert the desired signal to the 1st IF of 45MHz. The 1st conversion process to 45MHz utilizes a low-side injection method. Since the receive range is 450 to 470MHz in 12.5kHz steps, the 1st LO will cover 405 to 425MHz in 12.5kHz steps.

1st Intermediate Frequency

The 1st IF is filtered by a 3-pole monolithic crystal filter, FL302. This filter has a center frequency of 45MHz and has a bandwidth of 15kHz. Since the first mixer has gain, no IF amplifier is needed. Hence the filtered output of the 1st IF is fed directly to the SA-606 FM demodulator IC for further processing.

1st Local Oscillator

The first conversion process mixes the filtered and pre-amplified received signal with a locally generated signal source that is phase locked to a 16MHz master TCXO crystal. This 1st local oscillator is generated from a VCO circuit consisting of Q303 and Q307 and its associated components. The VCO output signal is buffered by U302, and a portion of this signal is fed back to the PLL synthesizer IC, U300, which divides it down using a set of on-chip programmable dividers and compares the result to a divided-down version of the 16MHz master clock in a phase detector. Any static or rotating phase difference between the two signals generates a series of current pulses at a rate of 50 kHz which are converted to a steering voltage in the loop filter. This filtered voltage is then used in concert with a variable-capacitance diode in the VCO circuit to correct this offset to zero. The loop filter also serves to control loop dynamics, suppress the 50kHz phase detector sampling frequency, and noise. The programmable feedback divider string within U300 can also divide the VCO by a fractional part, so smaller than 50kHz increments can be had; thus, 12.5kHz steps can be generated.

The other VCO output is split into two paths. One path is filtered by a single-section elliptic lowpass filter to reduce the harmonic content, and the result serves as the 1st local oscillator signal in the 1st conversion process already described. The second signal path is fed to the disabled transmitter driver and is not used in receive mode. The 1st local oscillator frequency range is 405 to 425MHz in 12.5kHz steps.

2nd Mixer and FSK Data Demodulator

The output of the 1st IF at 45MHz is fed to the FM/FSK demodulator IC, U303. Here, the incoming 45MHz 1st IF is downconverted to a 2nd IF of 450kHz and filtered by two 9kHz ceramic bandpass filters FL300 and FL301. These filters provide the final channel selectivity. This downconversion process is accomplished by an on-chip double balanced mixer in conjunction with the 2nd LO VCO using low-side injection. This VCO runs at 44.550MHz and is designed around an active transistor on U303 in concert with an external VCO tank circuit. Again, as with the 1st LO, a portion of this 2nd LO signal is sent to the PLL synthesizer IC, U300, where it is divided down by 891 to yield 50kHz

and is then phase locked with the 16MHz master clock TCXO divided by 320 (50kHz). The resulting phase difference is filtered by a loop filter, and the resulting loop correction voltage is coupled to the 2nd LO VCO, thus completing the loop. This 2nd LO frequency is fixed at 44.550MHz.

After the ceramic bandpass filters, the filtered 450kHz signal is hard limited by a set of limiting amplifiers, and the result is mixed together with a 90-degree phase shifted version of itself. This quadrature demodulation process, after removal of the 450kHz carrier components, yields the received FSK data. Received signal strength indication (RSSI) is derived from the limiting amplifiers, and provides an indication of the received signal level from the transmitter.

The FM demodulator output is then sent to two active lowpass filters, U110 and U112. One filter provides a DC estimate, and the other is a data-rate filter. The comparison of these two signals provide received data timing information, and the output of just the data-rate filter is the recovered 4-level FSK data. Two bits per symbol are sent, thus 4-level FSK, and the effective maximum payload data bit rate is 9600 bits per second (bps). The resulting 4-level FSK recovered data is sent to the microcontroller, U106, where it is quantized and processed digitally.

16MHz Master TCXO Clock

The entire EL-705 data transceiver clock is derived from an on-board 16MHz TCXO which has a stability of +/- 1.5 ppm over the temperature range of –30 to +75 degrees C. This TCXO provides the clocks needed for the microcontroller and serves as the reference with which all RF signals are phase locked. Thus, all signals generated from this master reference will have a stability of +/-1.5 ppm as well. The TCXO frequency also has the capability of being adjustable via a control voltage of +/-15 ppm.

2.3.2 Transmitter

Transmit VCO and Modulation

In transmit, the carrier is generated directly by VCO circuitry Q303 and Q307 and its associated components. The output of this VCO is buffered by U302 and a portion is sent back to the PLL IC U300, where again it is phase locked to the 16MHz master clock as mentioned before. Here again, the programmable feedback dividers are changed by a three-wire buss from the microcontroller, and are modified to divide down the VCO output to conform to the transmit frequency range of 450 to 470MHz with 12.5kHz steps. A PIN diode switch is used within the VCO circuitry to increase the VCO oscillation frequency to the higher, transmit frequency range.

The data to be transmitted consists of a 4-level FSK, raised-root cosine modulation. The data is encoded as two bits per symbol. Operation of the transmitter is key-on-data. The modulation voltage is generated by the microcontroller as a DC-preserved rate-root cosine shaped data bit PWM waveform, and therefore two-port modulation is used. One

port is sent to the 16MHz TCXO where the data is allowed to modulate the TCXO directly from frequencies from DC up thru to the VCO PLL closed-loop bandwidth. The other is sent to the VCO loop filter where the data modulates the VCO at rates higher than the VCO PLL closed-loop bandwidth. The peak deviation of the data modulated carrier is 3kHz. U111 filters both two-port modulation paths to further reduce out of band energy.

Transmit Driver Amplifier

The modulated transmit buffered VCO output is then split into two paths. One is sent on to the receive mixer where it is not used. The other path is sent to U202 which consists of a voltage-controlled power gain stage. This stage amplifies the modulated VCO output sufficient to drive a power amplifier.

RF Power Amplifier

The amplified transmit waveform from U202 is then coupled into an enhancement mode power MOSFET, Q202, which has enough power gain to amplify the transmit signal level to the two watt level. A resistive divider type DAC circuit controlled by the microcontroller is utilized to set the bias current for the final RF power amplifier.

RF Power Control Loop

The power amplified transmit signal from Q202 is then passed thru a directional coupler where a portion of the forward power component is sampled and envelope detected. This resulting DC voltage, proportional to the forward power coming from the RF power amplifier is filtered and sent to an op-amp, U200, configured as an integrator. This integrator integrates the difference between this DC component of the forward power and a DC voltage sent from a filtered PWM output of the microcontroller, U106. By varying this PWM duty cycle, a DC voltage is developed which can be used to represent the desired forward power level. The integrated difference between these two voltages is sent back to the gain control pin of U202 to complete a power control loop. Thus, by varying the DC voltage obtained from the PWM output, any power output level from Q202 can be realized anywhere between 0 and +33dBm (1mW and 2 watts).

Transmit/Receive (T/R) Switch and Harmonic Lowpass Filter

The RF output from the power control loop directional coupler is then sent to a PIN diode T/R switch. When activated in transmit mode, this switch utilizes a lumped-element quarter wave network which effectively isolates the receive input from the antenna and transmit path. Thus, the power developed in the transmitter stages is send on thru to the harmonic lowpass filter. The lowpass filter consists of a five-pole LC filter and effectively attenuates the harmonics of the transmit carrier to an acceptable level. The RF output of this harmonic lowpass filter is then sent thru J201, where an external antenna is connected.