APPENDIX F: PRODUCT DESCRIPTION

Please see the following pages.

SWL-2200U Radio Description

SWL-2200U USB Stick radio Description

Samsung MagicLAN SWL-2200U USB Stick
Wireless LAN Radio Description

The Samsung SWL-2200U WLAN USB Adapter is a complete wireless high speed Network Interface Card (NIC) utilizing the Intersil PRISM® 2.5 Direct Sequence Spread Spectrum Wireless Transceiver chip set. It provides a complete PRISM 2.5 reference design evaluation platform of hardware and software to system providers or integrators requiring wireless data communications capability and is ideal for integration into computer platforms.

The USB interface implemented in the SWL-2200U complies with the Universal Serial Bus Specification Revision 1.1 dated September 23,1998, which is available from the USB Implementers' forum at http://www.usb.org/.

SWL-2200U supports the IEEE 802.11b network specification for Direct Sequence Spread Spectrum DSSS signaling, providing data rates of 1, 2, 5.5 and 11Mbps. The softwares (Drivers, Utilities, and Manuals) are available on the Install CD or the Samsung MagicLAN Web Site, http://www.magicLAN.com/.

Fiqure 1 shows a block diagram of SWL-2200U. This radio has been designed to conform to the IEEE 802.11b standard.

This application note details the RF and analog design of these cards giving a detailed description of the receive and transmit processes.

General Specification

Targeted Standard	IEEE802.11b
DataRate	1MbpsDBPSK
	2Mbps DQPSK
	5.5Mbps CCK
	11Mbps CCK
Range @ 11Mbps	20m Indoor (typical), 150m Outdoor (typical)
Frequency Range	2412MHz to 2484MHz
Step Size	1MHz
IF Frequency	374MHz
IF Bandwidth @+-3dB	22MHz
RX/TX Switching Speed	2us (Typ)
Operating Voltage	5.0+-0.5Vdc from Host PC
Operating Temperature Range	0°C to 45°C
Storage Temperature Range	-20°C to 70°C
Mechanical	84mm• 25mm• 12mm
Antenna Interface	Chip Antennas on PCB

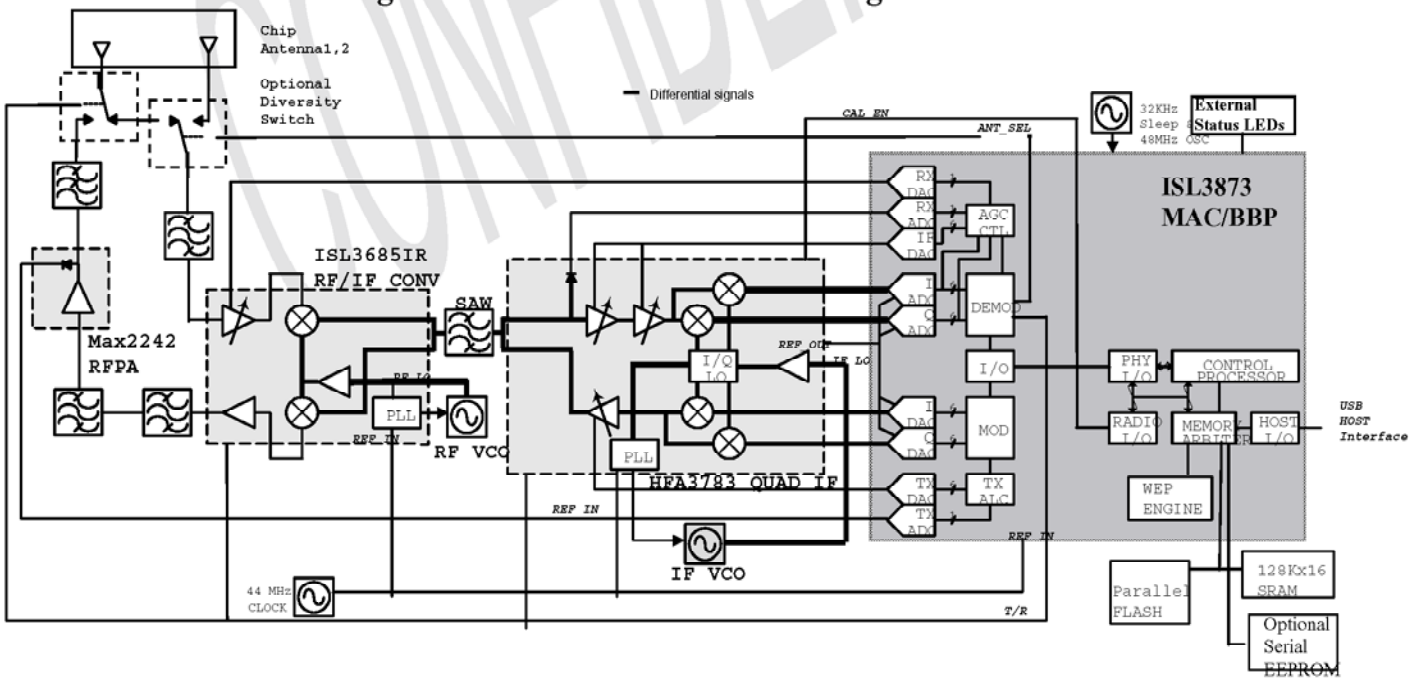
Receive Specifications

Sensitivity	-92dBm(Typ), 1Mbps,8E-2 FER
	-89 dBm (Typ), 2Mbps, 8E-2 FER
	-87 dBm (Typ), 5.5Mbps, 8E-2 FER
	-82 dBm (Typ), 11Mbps, 8E-2 FER
NOTE : FER = Frame Error Rate or Packet Error Rate	
Input Third Order Intercept Point, high gain	-5dBm (Typ)
Image Rejection @8%PER	50dB(Typ)
IF Rejection	>56dB(Typ)
Adjacent Channel Rejection @ 8%PER	35dBc
Consumption Current	220mA(Typ)

Transmit Specifications

Output Power	+16dBm (Typ)
Transmit Spectral Mask IEEE 802.11b	-30dBc sidelobes
Consumption Current	310mA (Typ)

Figure 1. SWL-2200U Block Diagram



Receive Processing

The signal is received through either one of the two chip antennas on the card as shown in the block diagram. These two antennas are controlled by the ISL3873 MAC/Baseband Processor chip (U1) and the diversity switch (U10). Antenna diversity is used to counter the adverse effects of multipath fading and antenna pattern nulls. Such advantages justify the extra space that the second antenna occupies on the card.

The received input from the antenna passes through a bandpass filter (FL5, see Fig 4 below), which provides protection for the RF front-end from out-of-band interfering signals, and image rejection for the first downconverter.

FIGURE 4. INPUT BANDPASS FILTER FREQUENCY RESPONSE & RETURN LOSS

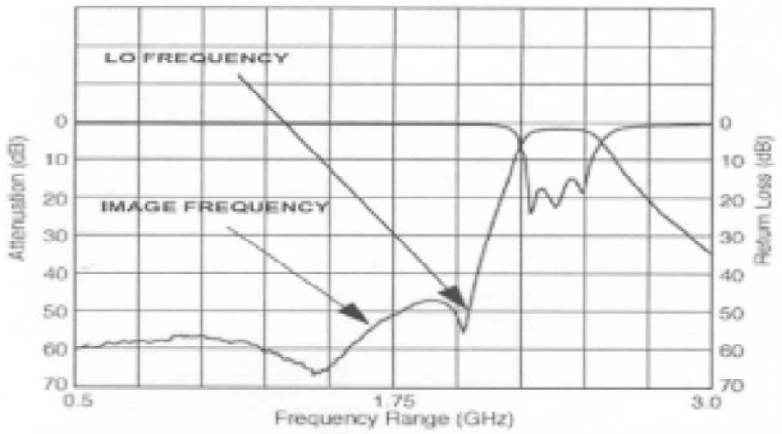


FIGURE 4. INPUT BANDPASS FILTER FREQUENCY RESPONSE & RETURN LOSS

The signal then enters the receive chain of the ISL3685 RF/IF Converter which features a low noise, selectable-gain amplifier (LNA). This amplifier is used to set the receiver noise figure (NF).

The LNA section of the ISL3685 has a selectable gain control H/L pin (pin #5). When the MAC/Baseband processor detects the presence of a strong signal from the IF peak detector output of the HFA3783, it will change the gain settings of the LNA in ISL3685. The peak detector limit is typically -20dBm at the input of the radio. This gain control feature further improves the dynamic range and the Signal Distortion performance of the PRISM 2.5 Chip set.

After the LNA the signal enters the mixer section of the ISL3685, where down-conversion from the RF frequency of 2.4GHz- 2.5GHz band is performed. The IF frequency is 374.25MHz. Low-side injection is used to place the receive image 748.5MHz below the tuned channel. The down converter is driven by an external RF LO with its frequency of operation phase locked by a PLL internal to the ISL3685. This PLL circuit uses an external 44MHz crystal oscillator as a reference frequency input. It should be noted that the ISL3685 RF/IF Converter operates from two separate regulated 2.84V supplies. One regulator, VCCA, supplies the receive and transmit section of the chip, while the other, VCCB, is dedicated to the PLL section and the external RF LO.

The output of the RF/IF Converter is a differential pair of IF signals (RX_MX_OUT+, RX_MX_OUT-). These two signals are open collector high impedance outputs. They are designed to share a common IF matching network and IF SAW filter with the transmit mixer. The PC board layout in this area was designed with special care to avoid interference and noise pickup. Layout symmetry and management of PC board parasites were taken into consideration in order to maximize the bandwidth of the IF matching network while minimizing insertion loss.

A standard LC matching network consisting of R39, R44, L12, L14, C49, and C75 was used at the output of the ISL3685 in order to match the mixer output to 200Ù differential. The differential signals are then fed into an IF SAW filter, FL1, with center frequency of 374MHz, and a 3dB bandwidth of 22MHz.
The SAW frequency response is shown if Figure 5. The group delay variation of this filter is typically 40ns and the insertion loss is typically 8.5dB. The filter's differential inputs are matched to 200 • •using L5, C39 and C44. Another LC matching network to match the output of the SAW filter to 200 • •was designed using L6, C45 and C46.

FIGURE 5. SAW IF FILTER FREQUENCY RESPONSE ADJACENT CHANNEL

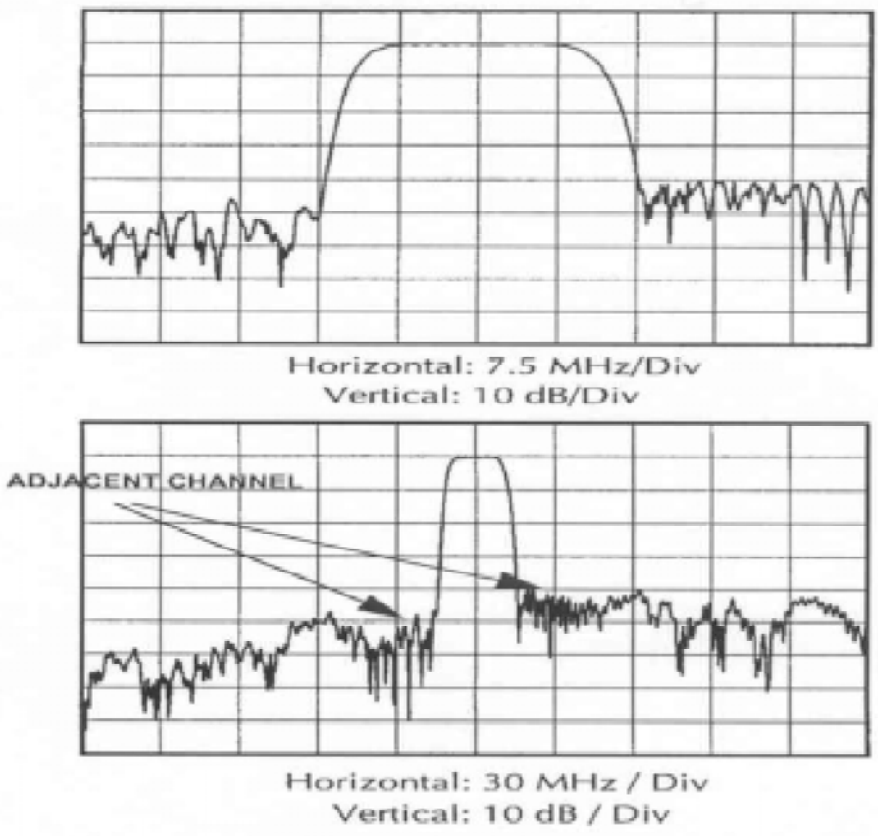


FIGURE 5. SAW IF FILTER FREQUENCY RESPONSE

This SAW filter is used to suppress adjacent channel interference generated from other inband sources. The insertion loss is not critical, since at this point in the receiver, component loss or NF is offset by the preceding gain stages.
It is worth emphasizing the fact that careful design of the ISL3685 RF/IF Converter TX/RX interface as well as design of the HFA3783 IQ Modulator/Demodulator TX/RX interface provided a possibility to share a

single SAW filter in a receive and transmit mode. This approach reduces the cost of the Bill of Materials (BOM) with the PRISM 2.5 radio chip set.

The differential filter outputs are then fed to the I/Q Modulator/Demodulator chip (the HFA3783). In the receive mode, the differential signals travel through two cascaded, low distortion, integrated AGC IF amplifiers. Following the AGC stages, an AC coupled down-conversion pair of quadrature doubly balanced mixers are used for I and Q demodulation. The output of the I and Q mixers are DC coupled to a pair of anti-aliasing baseband filters with DC offset correction. The down converter mentioned above is driven by a broadband quadrature IF LO generator provided by Intersil's integrated external IF VCO the ISL3183 and with frequency of operation phase locked by a PLL. This PLL circuit contains a three-wire interface for serial bus programming. The 44MHz crystal oscillator mentioned above is also used as the reference frequency source for this PLL. The HFA3783 operates from two separate regulated 2.84V supplies. One regulator, VCCA, supplies the receive and transmit section of the chip, while the other, VCCB, is dedicated for the PLL section and the external IF LO. The cascaded front end Noise Figure, IP3 and gain distribution analysis are shown in Table 1.

TABLE 1. PRISM CASCADED FRONTED-END ANALYSIS

STAGE	G	F	IP3O	GC	FC	IP30C	IP3IC
RF connector/Input trace loss	-0.5	0.5	99	-0.5	0.5	99.0	99.5
Antenna select Switch	-0.5	0.5	43	-1.0	1.0	43	44
FL6 Receive Band Filter	-2.0	2.0	99	-3.0	3.0	41	44
Matching Network/ trace loss	-0.5	0.5	99	-3.5	3.5	40.5	44
ISL3685 - max gain	25	3.7	13	21.5	7.2	13	-8.5
FL1 IF Filter	-10.0	10.0	99	11.5	7.25	3.0	-8.5
HFA3783 - max gain	56.0	7.0	2.2	67.5	7.48	2.2	-65.3

Cascaded Gain = 67.5dB Cascaded NF = 7.48dB Cascaded Input IP3 = -65.3dBm

Data for maximum gain (input signal @ -100dBm)

G (individual stage gain, dB), GC (cumulative gain, dB)

F (NF, dB), FC (cumulative NF, dB),

IP3O (individual stage input IP3, dBm), IP3OC(cumulative input IP3, dBm)

F+ (incremental noise figure per device).

The balanced differential analog outputs of the HFA3783 signals (RxI+, RxI-, RxQ+, RxQ-) are then fed into the Baseband Processor section of the combined Medium Access Controller/Baseband Processor chip (ISL3873). The shape of the received I and Q analog baseband signals are shown in Figure 6. In the receive path, these signals enter the two on-board 6-bit Analog to Digital Converters (A/Ds).

An AGC circuit is designed to adjust for signal level variations and to optimize A/D performance of the I and Q inputs by providing proper headroom on the 6-bit converters.

The 44MHz crystal oscillator, previously mentioned, is used to provide the main clock for the ISL3873.

After the A/D converters the Baseband Processor performs the decoding and descrambling of the data to prepare it for the Medium Access Controller (MAC). All packet signals contain a preamble, followed by a header and the payload data. The preamble uses Differential Binary Phase Shift Keying (DBPSK) Modulation that is a scrambled series of all 1's to aid in the acquisition process. In BPSK only 1 bit is encoded into each data symbol. Each data symbol is multiplied by an 11 bit Pseudo Random Noise (PN) sequence or