Certification Report on Compliance with Respect to FCC CFR 47, Para. 15.247(e)
Measurement of Processing Gain of Direct Sequence Spread Spectrum

Product: Intersil HWB3163 Rev B WLAN PCMCIA

Tested by: Intersil Corp.
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ENGINEERING SUMMARY AND CERTIFICATION

This report contains the results of the engineering evaluation performed on an Intersil Wireless LAN PC Card, Model HWB3163 Rev B. The tests were carried out in accordance with FCC CFR 47, Para. 15.247(e).

Robert Rood is a Wireless Applications Staff Engineer at Intersil Corporation. Intersil is a new independent company as of August 13, 1999, previously known as Harris Semiconductor. Robert received a BSEE from the University of Florida in 1979 and his Masters of Science in Engineering Management from Florida Tech in 1988. He joined Harris Semiconductor in 1983 as a Test Engineer after 3 ½ years with Burr Brown Research Corp. He was promoted to Test Staff Engineer in 1989 and moved into Applications in 1991 where he has built on his experience with high speed linear and currently leads the wireless radio development team.

I certify that this data was taken by me or at my direction and to the best of my knowledge and belief, is true and accurate. Based on the test results, it is certified that the product meets the requirements as set forth in the above specification.

Submitted by: Robert Rood _____ Date: _____
Staff Engineer, Wireless Applications, Intersil Corp.

Processing Gain of a Direct Sequence Spread Spectrum, FCC CFR 47, Para. 15.247(e)

Product Name: HWB3163 Rev B

FCC Requirements: The processing gain of a direct sequence system shall be at least 10dB. The processing gain shall be determined from the ratio in dB of the signal-to-noise ratio with the system spreading code turned off to the signal-to-noise ratio with the system spreading code turned on, as measured at the demodulated output of the receiver.

Environmental Conditions: Room Temperature and Humidity: 25^{O}C and 50%.

Power Input: DC Power from a laptop computer.

Test Equipment:
Hewlett Packard Spectrum Analyzer, Model HP8593E 9kHz to 22GHz
Marconi Signal Generator, Model 2031, Freq. Range 10kHz to 2.7GHz
Hewlett Packard Power Meter, Model HP438A
Hewlett Packard Power Sensor, Model HP8481D, -20 to -70dBm
Hewlett Packard Attenuators, Model HP8493A, 6dB and 10dB
Hewlett Packard Step Attenuator, Model HP8494A, 1dB steps
Hewlett Packard Step Attenuator, Model HP8495D, 10dB steps
Hewlett Packard Power Splitter, Model HP11667B
Campaq Laptop Computers (Qty 2), Model Armada 1700

Method of Measurement: Jamming Margin Method. The processing gain may be measured using the CW jamming margin method. Figure 1 shows the test configuration. The test consists of stepping a signal generator in 50kHz increments across the passband of the system. At each point, the generator level required to produce the recommended Bit Error Rate (BER) is recorded. This level is the jammer level. The output power of the transmitting unit is measured at the same point. The Jammer to Signal (J/S) ratio is the calculated. Discard the worst 20% of the J/S data points. The lowest remaining J/S ratio is used when calculating the Process Gain.

Theoretical Calculation: The use of 8% FER frame error rate (or PER packet error rate) as a substitute for the recommended BER bit error rate and the ideal signal to noise ratio per symbol (Es/No) is derived in the attached documents; “Testing for compliance with FCC rules 15-247e”, by Carl Andren and “Theoretical BER curves for the IEEE 1 and 2 Mbps modulations” by Carl Andren.

Engineering Summary: Processing Gain Results Summary

Frequency Channel	Data Rate(Mbps)	Gp (dB)
1	11	11.5
6	11	11.4
11	11	12
6	2	12.5