Theory of Operation

This document is an excerpt from the NGT Transceiver System Technical Service Manual, Chapter 4.

Transmit Path

Handset microphone amplifier transmit path

Drawing 04-03125

The handset has an electret microphone. When PTT (press-to-talk) is not pressed, the microphone audio is clamped by V5.

When PTT is Pressed, V5 is turned off, allowing audio from the microphone to be passed to the amplifier IC9/B. The output of IC9/B is split into two paths, one going to the handset audio bus, the other passing through the inverter IC9/A before going to the handset audio bus. In this way, push-pull balanced audio is provided to the junction box via the handset.

Junction box transmit path

Drawing 04-03201

The junction box has four transmit audio inputs. These four inputs are mixed together at the input of IC7/A as described below.

Tx Audio Input 1. When PTT is pressed on the handset, the handset audio AIN+ and AIN- on P7 is passed to IC11/A. IC11/A converts the balanced audio to single-ended audio that is then passed to IC7/A.

Tx Audio Input 2. When PTT is pressed on the desk console, the desk console audio is mixed via R57 at the input of IC7/A.

Tx Audio Input 3. The audio input of the GPIO port is on pin 5 and 15 of J107. When the GPIO PTT is active, the audio is balanced via T1 before passing to the volume control IC2/C. IC2/C is activated to a preset level, controlled by software. The audio is then mixed via R58 at the input of IC7/A.

Tx Audio Input 4. A tone used for Morse is generated by IC9 on the Microprocessor PCB (drawing 04-03133). The tone is passed to the tone volume control IC2/B before mixing via R56 at the input of IC7/A.

The output of IC7/A goes to IC11/B and then to IC10/A. These two ICs from a three-pole low-pass anti-aliasing filter with a nominal 3kHz cut-off frequency.

The output of IC10/A passes to IC10/B. IC10/B acts as a peak limiter due to H2 and H3 in the feedback path. The normal level for the audio is 1 V P-P. Where the audio level is much higher than this (such as when someone shouts into the microphone), IC10/B limits the output of IC10/A to 4 V P-P. This protects the synchronization pulse generated in the RF unit from becoming corrupted.

The output of IC10/B is split into two paths, one going to the TDM gate IC9/B, the other passing through the inverter IC8/B before going to the TDM gate IC9/A. This produces push-pull balanced audio.

Time division multiplex audio channels

Drawing 04-03201

The system audio uses TDM to produce seven channels of audio and one synchronisation pulse to reference the channel timing.

The audio is sampled at a rate of 12.5 kHz by the TDM gates IC9/A and IC9/B. IC9/A and IC9/B are driven by IC1.

The position of the audio channel will vary depending on the requirements of the system. Its position can be determined by attaching an oscilloscope at test point 2 (TP2).

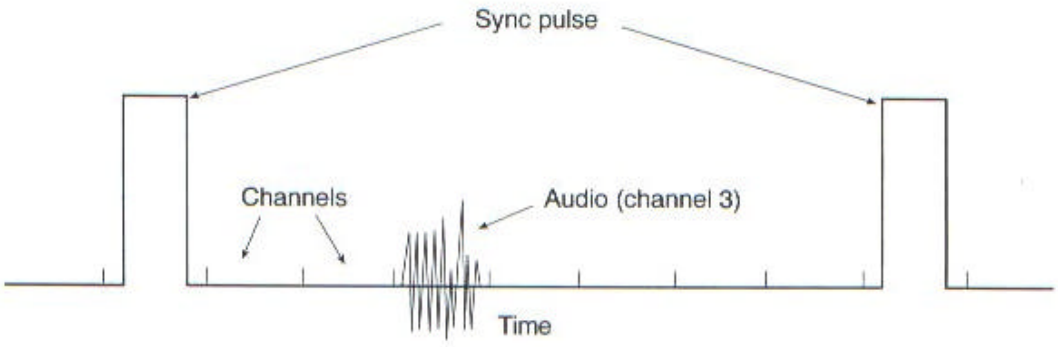

Figure 4 – 1: Representation of the waveform as measured at test point 2 (TP2)

IC11 on the Audio Interface PCB (drawing 04-03109) in the RF unit, drives V3 and IC6/A to generate the synchronization pulse.

The TDM audio from TDM gates IC9/A and IC9/B is passed to the RF unit via SYS AUDIO+- on the CIB.

Codan Interconnect Bus transmit path

The CIB is an 8-wire bus that connects all the units in the system together:

- **SYS AUDIO (+-):** The audio is TDM balanced, as described in the previous section.
- **SYS DATA (+-):** The data uses Control Area Network (CAN) protocol. This protocol has good error detection capabilities and performs well in high noise environments. The data rate on the CIB is 100 kbps.
- **STBY:** Standby power is a 100mA 5 V DC continuous supply. This is used to backlight the ON/OFF button at night.
- **PROTECTED A:** The Protected A rail is an unregulated battery supply that is used to supply power to all the units in the transceiver system. The maximum current that this can supply is 2 A. If very long runs of the CIB cabling are required, an external supply may be connected to the junction box to supply power locally.
- **PWR ON:** The Power On line is used to switch the transceiver on when it is grounded as described in the Power On section at the beginning of this chapter.

- **GND:** Ground is the supply return wire and is connected to the negative terminal of the battery.

RF unit-Audio Interface PCB transmit path

Drawing 04-03109

The Transmit TDM audio from the CIB goes to IC7/B. IC7/B then converts the push-pull audio to single-ended audio so that the correct audio channel is sampled by IC6/D.

C21 is the hold capacitor, and IC7/A, IC8/A and IC8/B form a 5-pole Chebishev re-construction filter with a nominal cutoff frequency of 3 kHz. The filtered audio then goes to the Application Processor PCB via ADC AUX IN.

RF unit-Application Processor PCB transmit path

Drawing 04-03109

The Transmit audio goes to IC5, pin 28. This audio interface device contains an analog to digital converter and a digital to analog converter.

The analog Transmit audio is sampled and converted by IC5 into digital format. A compression function is applied to the digital audio as shown in Figure 4-2 below.

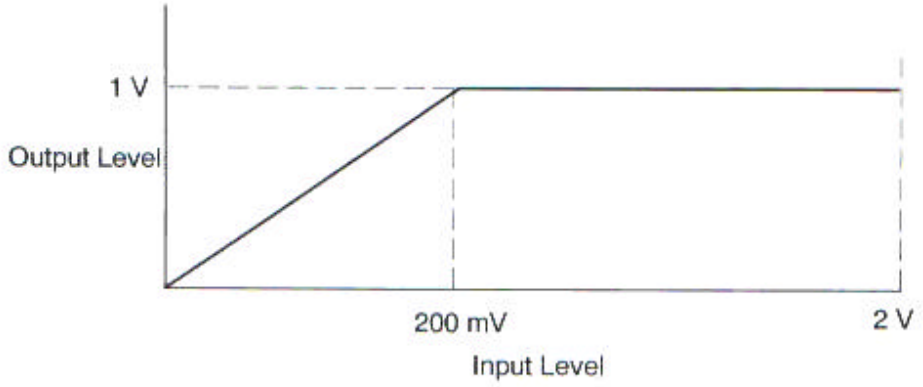

Figure 4-2: Representation of compression function by IC5

The decay time constant is controlled by software and can be varied depending on the type of transmission. For example, for speech, the time constant needs to be short, but for data it needs to be lengthened to improve the bit error rate (BER).

The output level is halved when amplitude modulation (AM) is transmitted or low power is selected, and is controlled by software.

The output of IC5, pins 3 and 4, are summed together in IC7/A to produce an output of 1 V P-P. This output then goes via the Audio Interface PCB to the Rx/Exciter PCB.

RF unit-Rx/Exciter PCB transmitter exciter

Transmit/Receive switching

Drawing 04-03106 sheet 3

The PTT command from the handset via the CIB causes IC405 to drive pins 12 and 13 (Rx Switch and Tx Switch). This switches V419 and V420 off and switches V421 and V422 on, thus causing +10 V Tx to be active. This switches all circuits to the Transmit mode.

Transmit modulator
Drawing 04-03106 sheet 2
The audio goes to the Tx Level potentiometer to set the exciter output level to 600 mV P-P. It then is passed to the input of the balanced modulator IC204 pin 1. The modulator is enabled when DC is applied via R254 to the bias input pin 5.

The audio is mixed with the local oscillator of 456.5 kHz (453.5 kHz for LSB) and is applied to pin 8 and pin 10 of IC 204. This produces a double sideband (DSB) output at pin 6. From there it is passed via D205 to the 455 kHz sideband ceramic filter Z201 pin 1.

455 kHz filter and first mixer

Drawing 04-03106 sheet 2 and 1

(Sheet 2) The 455 kHz sideband ceramic filter Z201, with a bandwidth of 2.5 kHz, filters out the unwanted sideband and leaves only the wanted sideband at pin 3. From there it is passed via the noise limiter gate V204 (disabled in Transmit mode) to a tuned auto transformer T202.

(Sheet 1) The signal is passed from T202 via a resistor-matching attenuator network R144, R145 and R146 to the input of the first balanced amplifier/mixer IC103 pins 12 and 13. IC103 is enabled by applying +10 V Tx. This applies DC via R142 to pin 4, and bias current via R43 to pin 11. The filtered +10 V rail is applied to the mixer output, pins 3 and 14, via the centre tap of the output transformer T108.

The 455 kHz transmit signal is mixed with the output of the REF OSC and applied to IC103 pin 5 to produce a second IF output signal at pins 3 and 14 centred on 45 MHz. The gain of the mixer/amplifier is approximately 20 dB.

45 MHz band-pass filter

Drawing 04-03106 sheet 1

The 45 MHz IF signal is filtered through a 15 kHz band-pass filter (BPF) consisting of T108, Z104, L117, Z103 and T107. This filter removes unwanted signals produced by the first mixer. The filtered output goes to the balanced input of the second mixer IC102 pins 12 and 13. R138 is between T107 and IC102 and is used as a fine balance adjustment for the mixer to remove unwanted spurious signals.

Second mixer and exciter output filter

Drawing 04-03106 sheet 1

The second mixer IC102 is enabled by applying +10 V Tx. This applies DC via R133 to pin 4, and bias current via R134 to pin 11. The filtered +10 V rail is applied via L116 to the transformer T106 and the mixer output from pins 3 and 14.

The 45 MHz transmit signal is mixed with the output of the local oscillator VCO1 then applied to IC102 pins 5 and 7 to produce the selected channel frequency at the mixer output pins 3 and 14. The gain of the mixer/amplifier is approximately 20 dB.

The mixer output goes via a 30 MHz low-pass filter to the transmit exciter output connector J2. From there it is coupled via a coaxial cable to the PA assembly.

Tuning

Drawing 04-03106 sheet 3, 2, and 1

When the Tune command is activated, IC405 pin 7 (sheet 3) goes low. This switches V416 off to allow the 456.5 kHz local oscillator carrier (453.5 kHz for LSB) to be passed to V206 (sheet 2) via CAR INJ. V206 inserts carrier to the input transformer T202 of the first Tx mixer IC103 (sheet 1).

At the same time, IC405 pin 5 (Tx MUTE) goes high and switches V203 (sheet 2) on. Thus, IC202/C and IC202/B open the noise gate V204, which stops the inserted carrier from being loaded by the sideband filter Z201.

The carrier at the output of the second mixer IC102 (sheet 1) will be at the frequency of the selected channel (the suppressed carrier frequency (SCF)). This frequency is used for tunig automatic antennae.

RF unit-Power Amplifier PCB transmit path

Gain control stage

Drawing 04-03169

The RF input is passed to T200, which turns the RF drive into push-pull. This is then applied to the variable gain stage V200 and V201. The FETs V202 and V201 are used as variable resistors depending on the ALC voltage applies to the gates.

If there is no Tx output, 5 V of ALC voltage is applied to the gates, so that the resistance is low and the gain is at maximum. As the output from the PA increases to the power set point (100 W or 125 W), the 5 V ALC voltage drops, thus increasing the resistance in the FETs and so reducing the gain of V200 and V201 and keeping the Tx output power at the set level (100 W or 125 W).

The overall gain of the PA is set to a constant value by R205.

Pre-driver stage

Drawing 04-03169

The leveled RF from the gain control stage is passed via T201 to the Class A push-pull amplifier formed by V204 and V205. L202 and C207 provide a small amount of high frequency gain peaking to ensure the overall output is flat with frequency.

Driver stage

Drawing 04-03169

The signal from the pre-driver stage goes via T203 to the driver stage. The driver is a Class B push-pull amplifier that provides a voltage drive to the output stage.

Each side of the amplifier has three transistors in parallel (V207, V208 and V209, and V210, V211 and V212). These transistors have resistors on theirs emitters to forces them to share the load.

The bias for the driver stage, provide by the emitter follower V206 and set by R222, is applied to the centre tap of T202.

Output stage and bias generator

Drawing 04-03169

The Class B push-pull output stage formed by V215 and V216 is driven from T203 to produce the 100 W or 125 W peak envelope power (PEP).

The bias voltage applied to each gate of V215 and V216 via R250 and R251 varies in level depending on the output level.

The drive waveform from the halfwave rectifier D200 is applied to the squaring (x^2) function circuit comprising IC202/B, V213 and V214. The output of this circuit is then amplified by IC202/A.

The static point of the bias is set by R240 and the amount of waveform bias is set by R244. The bias voltage is then passed to the gates of the output stage. When the match of the output stage is not perfect, the balance potentiometer R253 is used to trim the bias voltage so that equal current is drawn by each output FET.

The balanced to unbalanced impedance matching output transformer T204 couples the power amplifier output to the band filters via J2 and the PTT relay K8.

Output filters

Drawing 04-03169

The transmit frequency range is .6 MHz to 30 MHz. Seven low-pass filters are used to remove the harmonics generated by the PA. The filters are operated from IC2 and IC3 and are selected using relays K1 to K7 as required.

The output of the filter circuit passes through the RF bridge formed by T1 and associated components to the antenna output.

Automatic level control

Drawing 04-03169

The ALC is controlled by

- Forward power
- Reflected power
- Drain voltage swing of output stage
- Battery voltage
- Overtemperature of heatsink
- Failure of transmit/receive and filter relay

All the ALC inputs (except relay detection) are applied to V7 to V10. The 'OR'ed output is connected via R50 and D14 to the positive input pin of the ALC level comparator IC5/A pin 3. The reference voltage to tpin 2 is software controlled by the microprocessor IC2.

The microprocessor IC2 and R19 are used as a 6-bit digital to analog converter with an output range of 5 V to 2.5 V. The output from R19 pin 1 is buffered by IC6/B and then divided and filtered by R55, R56 and C151. The output is then buffered again by IC6/A and used as the reference voltage for IC5/A and IC201/B. This allows the microprocessor IC2 to reduce the PA output at the higher operating frequencies and ensures that the intermodulation distortion remains within specified limits.

The output voltage of the RF bridge formed by T1 and associated components is rectified by D1 for the forward power and by D2 for the reflected power.

The output of the forward rectifier D1 is applied via R37 to the input of V7. The sum of the resistors between the base of V7 and ground form a resistor divider network. This determines the nominal PEP output level when matched to a 50 Ω load.

For high power, the resistors R34 and R35 are shorted out by +5V on the gate of the FET switch V6 and do not contribute to the chain. The nominal high power output, which is measured at low frequency, is set by R32.

For low power, V6 is off, so R34 and R35 are added to the divider. R35 sets the power to <12 W PEP.

The output of the forward detector D1 is also applied to V8 via an averaging detector circuit formed by R40, R43 and C147. When the average of the signal exceeds the peak detector circuit V7, V8 takes control and reduces the output power (this occurs on single tones such as Tune mode, CW (Morse) and in some data transmissions).

When the handset PTT is active, V11 is switched off, which disables the average ALC circuit. This is so the transceiver will produce full PEP on a single tone. This is for measurement reasons only.

The peak output drain swing is rectified by D202 and applied to the transistor V10. V10 conducts and limits the drain peak to 34V to prevent damage to the output FETs

The battery voltage is monitored by V5. When the supply voltage (“A” rail) drops to approximately 12 V, the voltage at the base of V5 falls and causes V5 to conduct. This changes the threshold of the forward power ALC detector. The ALC detector then starts to reduce the output power and since the control is linear, a further reduction in supply voltage continues to lower the output power.

If the heatsink exceeds 80°C, the positive temperature coefficient (PTC) resistor R262 rapidly increases its resistance. This causes V13 to conduct and thus reduces the reference voltage. This lowers the output power and prevents the heatsink from exceeding 100°C.

The relay protection circuit is formed by IC5/b and associated components. It simultaneously monitors the output FET, drain swing and forward detector output of D1. If a relay failure results in no signal at the antenna output, the output of IC5/B will go high. This lowers the gain of the input amplifiers V200 and V201 and thus reduces the drive to the output FETs to a safe level.

The ALCs control the output power from the summing amplifier IC5/A. This output passes to IC201/B, which inverts the direction of the control signal to drive the variable resistor FETs V202 and V203 in the gain stage (see page 4-12, *Gain control stage*).

Receive path

Input low-pass filters

Drawing 04-03169

The receiver input signal goes through one of seven relay-selected low-pass filters (LPF) K1 to K7. The signal then goes via the transmit/receive relay K8 and signal clamping diodes D3 to D9 to connector J1.

Broadcast filter and RF amplifier

Drawing 04-03106, sheet 1

The signal goes through a broadcast filter to reduce any very strong broadcast frequencies below 1.6 MHz, and then goes to the RF amplifier V101. V101 has a nominal gain of 9 dB.

Where there are strong signals and V101 is not required, a 10 dB attenuator pad can be switched by relay K101 to reduce the signal going to mixer 1. The signal then passes through a 30 MHz LPF to remove signals above 30 MHz.

First mixer

Drawing 04-03106, sheet 1

The balanced mixer, formed by V103, V103, V105, and V106, mixes the received signal with the output of VCO1. This is buffer3ed by V107 and V108 to produce an intermediate frequency (IF) of 45 MHz. The mixer has a conversion gain of 4 dB.

45 MHz band-pass filter and amplifier

Drawing 04-03106, sheet 1

The 45 Mhz IF signal is filtered through a 15 kHz band-pass filter (BPF) Z101 and then amplified by V109. it is then filtered again by Z102. This removes the unwanted signals produced by the first mixer.

Second mixer

Drawing 04-03106, sheet 1

Mixer IC101 is a combined amplifier/balanced mixer. The 45 MHz signal is mixed with the output of the reference oscillator, then applied to pin 5. This operates on 44.545 MHz to produce a second IF centred at 455kHz.

DC to the mixer output is provided by the filtered +10 V rail, which is connected to the centre tap of the 455 kHz output transformer T202 (sheet 2). In Receive mode, the +10 VRx rail provided DC via R132 to IC101 pin 4 and bias via R131 to IC101 pin 11.

Noise limiter

Drawing 04-03106, sheet 2

The 455 kHz output of IC101 pins 3 and 14 (sheet 1) is applied to the balanced input of the high gain amplifier IC201 pins 4 and 6. The balanced outputs at pins 1 and 8 and connected to a tuned auto transformer T201 (455 kHz). The output of T201 goes to the base of the active rectifier V201. Noise bursts produce positive-going pulses at the collector of V201, and via V202, trigger the flip-flop IC202/B. The pulse width is determined by C210, R210 and R211 (nominally 250 µs).

The outputs of IC202/B pins 11 and 4 produce complementary pulses that are connected to the FET gates of V204 and V205. These gate out the noise bursts from the 455 kHz signal. With V204 on and V205 off, the IF signal is passed to the sideband filter Z201. When a noise burst is present, V204 is switched off and V205 is switched on, blocking the IF signal for the period of the gate pulse.

The average DC component of the collector current of V201 is used as an automatic gain control to IC201. It is applied via R206 to pin 5. This ensures that only the noise burst signal triggers the flip-flop IC202/B. The AGC decay constant is set by the components C206 and R205.

In Transmit mode, IC202 is disabled (see page 4-12, *Tuning*).

455 kHz filter and IF amplifier

Drawing 04-03106, sheet 2

The IF signal from the noise blanker gate V204 is passed to the 2.5 kHz ceramic filter Z201. The filter removes the unwanted sideband, adjacent channels and other unwanted products generated by the second mixer. The wanted sideband, centred at 455 kHz, is passed by the filter to a 3-stage gain controlled IF amplifier comprising V210, V211, V212 and associated components. The IF amplifier is broadly tuned to 455 kHz by the tuned circuits L201 and C229, L202 and C232, and L203 and C236.

When the optional filter Z202 is installed, relays K201 and K202 are fitted and links LK201 and LK202 are cut. The optional filter is selected when V207 is activated to energise the relays.

Automatic gain control

Drawing 04-03106, sheet 2

An automatic gain control (AGC) is applied to a number of stages in the receiver. This is used to increase the dynamic range of the receiver and to maintain an almost constant audio output level for a large variation of input signals.

When the receiver is at maximum gain, the AGC at the output of IC205/A is nominally 6.5 V. This voltage is set by the voltage reference IC206 and associated components.

The IF signal is rectified by V214 and the resulting DC is amplified by IC205/B. The signal is then passed to various timing circuits.

The signal is passed through D207 to the fast attack circuit (2 ms) comprising V215, R274 and C253. The decay time of this circuit is set by R280.

The signal also goes to the slow attack circuit comprising IC207/D, R279 and C254, and to the slow decay circuit (1 s) R283. The output from these two circuits is summed together at the emitter junction of V216 and IC207/A, and is then passed to the amplifier IC205/A.

If fast AGC is required, the fast/slow control line is held low by the microprocessor. This disables the slow charge capacitor C254.

If the AGC hold function is required, the hold/trigger line is held low. This enables an extra hold circuit comprising V217, V219 and associated components. This circuit holds the AGC voltage constant for a short period after the signal reduces, which can improve the readability of the signal.

The AGC voltage is passed to the IF amplifier. As the signal increases in level, the AGC voltage reduces and hence lowers the gain of the IF amplifier, thus keeping the output level constant.

If the signal level is very large, the anti-log and bias circuit comprising IC203 and associated components operates. When operating, this circuit causes RF AGC voltage to reduce, which in turn causes D104 (Drawing 04-03106, sheet 1) to conduct. This lowers the gain of mixer 1 and helps to keep the level constant at the IF output.

There is an AGC dump input to dump any AGC voltage from a high level signal ton a previously selected channel when the channel is changed. This allows the new channel to have maximum gain. The dump is achieved by pulling the AGC dump and fast/slow control lines low for a short period when a channel is changed.

Demodulator

Drawing 04-03106, sheet 2

The output of the 455 kHz IF amplifier is passed to the input of a double balanced mixer IC208. The IF signal is mixed with the local oscillator that is applied to pins 8 and 10 to produce an audio output at pin 6. The local oscillator operates at 456.5 kHz for USB operation and 453.5 kHz for LSB.

The audio is then filtered by the low-pass filter comprising IC209 and associeated components, before being passed to the Audio Interface PCB.

RF unit-Audio Interface PCB receive path

Voice mute

Drawing 04-03109

The audio from the Rx/Exciter PCB is fed to the input of the mute stage squaring amplifier IC15/A. The squared audio is then fed to a charge pump circuit comprising V10 and associated components. This circuit performs a frequency to voltage function that causes the resultant DC voltage to rise as the frequency increases.

IC16/A and associated components function as an LPF with a cut-off frequency of approximately 10 Hz. The output from IC16/A is a DC voltage, varying at the syllabic rate of the speech received.

IC15/C and IC15/D form a window comparator. The window width is adjusted by the preset MUTE ADJ (mute adjust) R85. The divider network R87, R88 and C64 provides the reference voltage for the window comparator. If the output rises or falls below this reference by the amount set by R85, the open collector outputs of IC15/C and IC 15D will discharge C65, thus applying a low to the input of comparator IC15/B. When the output from this comparator goes high, it indicates to several microprocessors that speech has been detected. The microprocessors then signal the junction box (via the CIB) to switch the audio path on by enabling volume control IC2/E (Drawing 04-03201).

Time division multiplex audio generation

Drawing 04-03109

The raw receive audio passes through a low-pass filter comprising IC3/A and IC3/B. It is then sampled by IC1/A and IC1/D at a rate of 12.5kHz, which produces the TDM audio for the CIB.

The raw receive audio is also passed to the Application Processor PCB where the digital signal processor (DSP) enhances the received audio. This audio enhancement is a proprietary function called “Easitalk”.

The output from the DSP is filtered by IC2/A and IC2/B. It is then sampled by IC1/B and IC1/C and becomes another audio channel on the CIB. The user can select either raw audio or this enhanced audio via the handset. The channel switching is performed in the junction box.

Codan Interconnect Bus receive path

The CIB is an 8-wire bus that connects all the units in the system together:

- **SYS AUDIO (+-):** The audio is TDM balanced (see page 4-19, Time division multiplex audio generation
- **SYS DATA (+-):** The data uses CAN protocol. This protocol has good error detection capabilities and performs well in high noise environments. The data rate on the CIB is 100 kbps.
- **STBY:** Standby power is a 100 mA 5 V DC continuous supply. This is used to backlight the ON/OFF button at night.
- **PROTECTED A:** The Protected A rail is an unregulated battery supply that is used to supply power to all the units in the transceiver system. The maximum current that this can supply is 2 A. If very long runs of the CIB cabling are required, an external supply may be connected to the junction box to supply power locally.
- **PWR ON:** The Power On line is used to switch the transceiver on when it is grounded (see page 4-2, Power on).
- **GND:** Ground is the supply return wire and is connected to the negative terminal of the battery.

Junction box receive path

Time division multiplex audio reconstruction and audio amplifier

Drawing 04-03201

The push-pull system audio is converted to single ended audio by IC8/A. The synchronization pulse is detected by V1 and fed to IC1 to synchronise the audio channels. IC9/B and IC9/C sample the audio channels depending on requirements. Each audio path has a 5-pole Chebyshev reconstruction filter comprising IC4/ IC5 and IC6 , with a nominal cutoff frequency of 3 kHz.

One audio path goes via the volume control IC2/E, which is microprocessor controlled from the speaker volume up/down buttons on the handset. This signal then goes via IC7/B to the audio power amplifier IC3, which drives the loudspeaker.

The other audio path goes to the GPIO port for auxiliary equipment.

Frequency control

Reference oscillator

Drawing 0403106, sheet 3

The reference oscillator is a “Butler” zero phase shift type, and is formed by V412, V413 and associated components. There are two outputs from the reference oscillator, one via V414 to the local oscillator for mixer 2, the other via V415 to the two DDS ICs IC403 and IC404.

Drawing 04-03095

The crystal Z401 is in an oven that runs at approximately 70°C. The negative temperature coefficient (NTC) resistor R4 measures the temperature of the crystal and causes the opamp comparator IC1 to vary the current in the heating element V2 to maintain the temperature within ±1°C.

The peak current of the oven is limited to 400 mA.

Direct digital synthesis

Local oscillator for upper sideband and lower sideband

Drawing 04-03106, sheet 3

IC404 divides the reference oscillator frequency of 44.545 MHz down to the required 456.5 kHz USB and 453.5 kHz for LSB. These frequencies may be varied when different optional filters are used.

The frequency information is programmed serially from the onboard microprocessor IC405.

Phase lock loop reference

Drawing 04-03106, sheet 3

IC403 divides the reference oscillator down to approximately 5 MHz. The signal is buffered by V411 and is then fed as the reference frequency to IC401.

The reference frequency is varied in small step sizes to produce the 10 Hz steps at the output of the phase lock loop.

The frequency information is programmed serially from the microprocessor IC405, based on the channel information.

VCO1 and phase lock loop

Drawing 04-03106, sheet 3

The oscillator VC01 is a “colpitts” type comprising V401 and associated components. The frequency of oscillation is determined by the turned circuit L403, C401 and the capacitance of the varicaps D401 to D404.

The Oscillator output at the tap of the tuned inductor L403 is coupled to the buffer stage made from V402, V403 and associated components. This output is used to drive mixer 1.

Synthesiser IC401 generates a DC control voltage via the phase/frequency detector and control amplifier. This is applied to the varicaps to lock VCO1 to the nominated frequency.

The VCO input frequency at F IN on IC401 is divided down to 100 kHz and compared with the reference frequency that is also divided down to 100 kHz. Ann error between these two signals will produce an output from either pin 14 or pin 15 of IC401.

The microprocessor IC405 loads serial data into IC401 depending on the channel frequency required. This varies the divide ratio on F IN, causing the VCO frequency to change.

The output pulses from pin 14 or 15 of IC401 are applied to the charge pump amplifier comprising V406 to V410. Pin 14 provides a “go up” pulse, while pin 15 provides a “go down” pulse. When locked, these pins go high impedance except for a very narrow pulse that occurs simultaneously at both outputs, thus holding the DC output at a fixed level.

The DC control voltage is filtered by C419, R422 and C418 to remove any reference frequency. The signal is then applied to the varicaps to control the frequency of oscillation.

26 V generator

Drawing 04-03106, sheet 3

The charge pump amplifier runs from the 26 V generator. The 26 V generator is a voltage tripler circuit comprising IC402 and associated components.

Microprocessors and control

Handset microprocessor and control

Standby and power on

Drawing 04-03125

When the transceiver is switched off, the standby indicator LED behind the power on button is illuminated. When the power on button is pressed, V9 is switched on. This causes the main power relay K200 (drawing 04-03169) in the RF unit to be switched on (via the CIB) and power is supplied to the entire system.

Microprocessor

Drawing 04-03125

The handset has an 8-bit microprocessor IC1. This, in conjunction with IC3 (which contains the program memory and an I/O expander with internal "glue" logic), controls all the functions in the handset.

The reset device IC2 resets microprocessor IC1 if the 5 V supply drops below approximately 4.7 V.

Keypad

Drawing 04-03125

The row lines (ROW 0 to ROW 1) are held low. This means when any button on the keypad is pressed, a low is detected by microprocessor IC1. This causes IC1 to scan the keypad to identify which button has been pressed, and then perform the function for that button.

The keypad is backlit by LEDs. The brightness of the LEDs is controlled by switching V1 and V2 as required.

Display

Drawing 04-03125

The liquid crystal display (LCD) H1 consists of a 98 x 32 dot matrix with LED backlighting. Data from the microprocessor IC1 is sent via the 8-bit data lines to the display where the in-built decoder and driver display the information required.

When the user selects to adjust the contrast of the LCD via the appropriate menu in the handset, the microprocessor IC1 varies the output of the electronic voltage divider IC6. IC6 feeds the temperature compensated driver IC7/A. IC7/A has an output of approximately –1 to –3 V, which is used to set the negative (VEE) level to the LCD to achieve the required contrast.

The backlighting of the LCD is achieved by a bank of LEDs mounted at the back of the display. The intensity of the backlighting is switched from bright to medium to off by switching V3, V4 and R36/37.

RS232 programming port

Drawing 04-03125

IC5 is a complete RS232 driver/receiver with in-built negative voltage generator.

Microprocessor IC1 sends and receives data from IC5 and then re-transmits the data onto the CIB.

Handset data bus

Drawing 04-03125

The data bus is a push-pull balanced system and is driven from the CAN driver IC8, which is controlled by the microprocessor. The data bus connects to the junction box. The data rate is approximately 100 kbps.

Junction box microprocessor and control

Handset data

Drawing 04-03133

Data from the handset is fed to IC15. IC15 changes the push-pull balanced data to single ended data that is read by microprocessor IC1.

Microprocessor

Drawing 04-03133

Microprocessor IC1 has a 16-bit bus that connects to SRAM IC8 and flash memory IC4 containing the operating code. The reset device IC2 resets the microprocessor if the 5 V supply drops below approximately 4.7 V.

UART and dual RS232

Drawing 04-03133

UART IC10 is connected to microprocessor IC1 via an 8-bit bus. The output of the UART is used to control the dual RS232 IC12, the outputs of which go to the serial port and the GPIO port.

The UART is also used to drive the diagnostic LEDs H1 to H4, and read the links LK1 to LK4.

E^2PROM

Drawing 04-03133

IC16 and IC17 are serial E^2PROM memories. They contain all the user settings for the system and are read by microprocessor IC1 as required.

Tone generation

Drawing 04-03133

Tone generator IC9 generates tones by dividing the 16 MHz clock by various factors as programmed by the data inputs from the microprocessor. This provides the audible signals required for key beeps and warning signals at the loudspeaker.

CAN driver

Drawing 04-03133

CAN bus controller IC11 decodes the CAN protocol and passes data to and from microprocessor IC1.

IC11 is connected to the push-pull balanced driver for the CIB IC14, which transfers data to the RF unit. The data rate is approximately 100 kbps.

RF unit microprocessors and control

Overview

The RF unit has five microprocessors, two of which are on the Application Processor PCB. The first of these two microprocessors is the DSP processor IC3, which performs speech processing, ALE requirements and high level control. The other processor is a master PIC IC4, which controls three other slave PICs on the other PCBs.

The slave PICs are used for low level control for the PCB on which they are located.

Application Processor PCB

Drawing 04-03108, sheet 1 and 2

CIB data from the junction box is fed via the push-pull balanced driver IC5 (drawing 04-03109) on the Audio Interface PCB to the CAN controller IC 17 (drawing 04-03108, sheet 2) on the Application Processor PCB, where data is decoded for the master PIC IC4 (sheet 1). The master PIC then issues commands to the other microprocessors.

IC3 is a 32-bit DSP processor. IC8, IC9 and IC10 are address bus buffers. IC11 and IC12 (sheet 2) are flash memory devices that hold the main operating code. IC13 and IC14 are SRAM devices.

IC15 is an electrically programmable logic device (EPLD) used for address decoding and controlling the CAN controller IC17.

IC16 is another flash memory device that contains all the channel information as well as the ALE link quality statistics.

The audio interface device IC5 (drawing 04-03108, sheet 1) receives audio on pin 26 or pin 28, depending on the process, then converts this to 14-bit data. The 14-bit data is processed in IC3 and then converted back to audio and output through IC7/A. The audio is then fed to the Audio Interface PCB.

The reset device IC2 resets the microprocessor if the 5 V supply drops below approximately 4.7 V.

Audio Interface PCB

Drawing 04-03109

PIC IC12 is in Sleep mode when no data is present. When data is received from master PIC IC4, the RC oscillator starts to run and ‘wakes up’ PIC IC12.

PIC IC12 then controls the antenna and power off, and drives the diagnostic LED H1. It also controls the EPLD IC11, which samples the ICB audio TDM channels.

Rx/Exciter PCB

Drawing 04-03106, sheet 3

PIC IC405 is in sleep mode when no data is present. When data is received from master PIC IC4, the RC oscillator starts to run and ‘wakes up’ PIC IC405.

PIC IC405 then programs the phase lock loop and the direct digital synthesis ICs depending on the channel frequency required. It also controls the transmit/receive switching functions, filter select, AGC time constraints and other ancillary devices.

PA Filter and Control PCB

Drawing 04-03169

PIC IC2 is in Sleep mode when no data is present. When data is received from master PIC IC4, the RC oscillator starts to run and ‘wakes up’ PIC IC12.

PIC IC12 then selects the correct filter for the channel in use, the PTT switching, high/low power switching, fast/slow ALC time constant, average ALC on/off and fan control. Also, in conjunction with R19, PIC IC2 forms a digital to analog converter that produces the reference ALC voltage. This is used to control the power verses frequency frequency output level.