Theory of Operation

The PAL is a direct sequence spread spectrum transmitter.

ASIC

An Application Specific Integrated Circuit (ASIC) reads the p.n. sequence from an EPROM and sends it to the BPSK Modulator.

BASEBAND FILTER

The sequence is then sent through a lowpass filter to remove the high frequency content of the PN sequence.

Local Oscillator

The local oscillator is synthesized using an integrated phase locked loop(PLL) circuit. A crystal oscillator(28.59375MHz) provides the reference for the PLL, keeping it stable over time and temperature. Differential outputs of the PLL provide the biphase carrier for the BPSK Modulator.

BPSK Modulator

The Bi-Phase Shift Key (BPSK) modulator switches between two phases(0° and 180°) at a 10MHz chipping rate according to a 63 chip pseudo-noise(PN) sequence. This spreads the 159KHz On-Off Shift Keying(OOK) information to a 20MHz Bandwidth.

10MHz Oscillator

The 10MHz Oscillator is used as a clock for the PN sequence.

28.59375MHz Oscillator

The 28.59375MHz oscillator is the reference oscillator for the PLL in the LO.

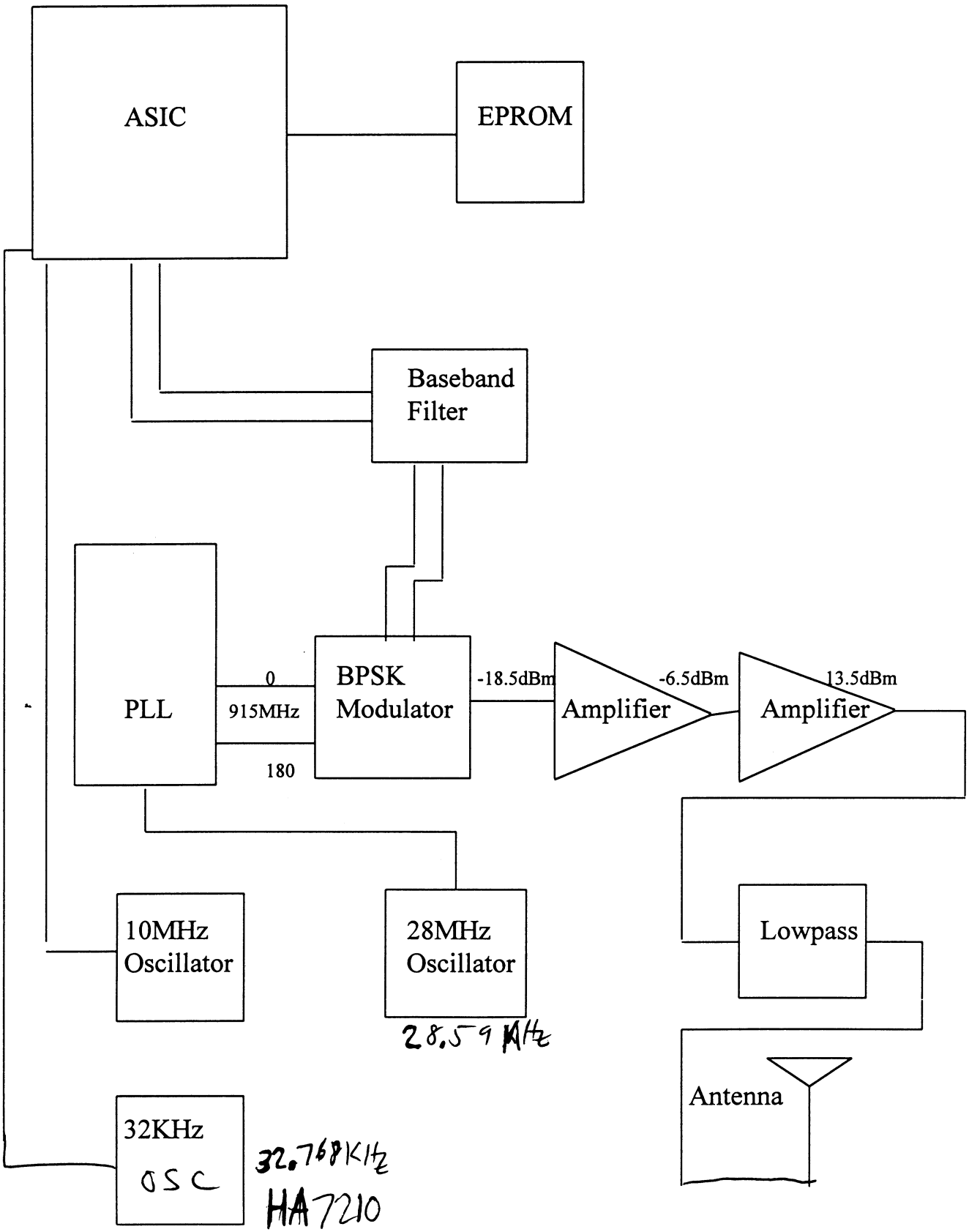
32KHz Oscillator

The 32.768KHz Oscillator is used as the clock to time the transmission of data.

Lowpass Filter

The lowpass filter reduces the harmonics of 915MHz to <-20dBc.

Block Diagram



PROCESS GAIN

Several considerations go into the determination of the process gain when using the jamming margin method of measurement. In particular we must determine how to measure the system sensitivity and the related S/N_o required at the output of the receiver.

SYSTEM DESCRIPTION

The design being submitted for approval is part of a system that has two functions, data telemetry and positional location. The transmitter unit provides telemetry data, and also supplies, via its transmitted signal, positional information. The telemetry data is encoded via on-off keying of the spread spectrum waveform using one complete code cycle per bit. Each message is 27 bits long. The receiver is a single conversion limiting IF design with a SAW correlator and full wave rectifier used to de-spread the incoming waveform.

The initial 3 bits of the message are always "1s", and are used to train the receiver system, and to provide time of arrival information for the message. The receiving system accurately time stamps each message with the arrival time of the 3rd bit of the preamble. By collecting time of arrival data from a number of receivers the position of the transmitter can be accurately calculated.

SENSITIVITY MEASUREMENT, AND S/N_o REQUIRED

For the on-off keyed waveform the signal to noise required for a $1x10^{-5}$ BER would be 12.5 dB in a perfect system. The constraint for the determination of position is more severe. By testing and statistical analysis the accuracy of position determination begins to be severely reduced when the correlation pulse seen at the output of the receiver is down by 3dB (.707 volts) from its maximum voltage. Because of this constraint the system sensitivity and the jamming margin need to be measured using the output pulse compression criteria.

The pulse compression criteria can be shown to occur in a perfect system at a signal to noise ratio of 18dB at the output of the full wave rectifier. (Appendix A)

CALCULATION

The calculated process gain for this system is 18dB. (Appendix A)

MEASUREMENT PROCEDURE

The processing gain of the combined transmitter/receiver system was measured using the suggested technique of FCC Public Notice 54797, dated 12-Jul-95. Since the system sensitivity criteria is based on correlation pulse compression an oscilloscope was substituted for the communications analyzer (fig 1 of the FCC notice). The experimental setup with equipment identified is shown following in figure A.

The following equipment was used:

spectrum analyzer - HP 8594E
Signal generator - HP 8648C
Scope - Tektronics TDS380
Combiners - minicircuits ZSC-2-4
Fixed attenuators - minicircuits SAT-10
Coarse adjust attenuator - HP 8496A (10dB steps)
Fine adjust attenuator - JFW Industries 50DR-046 (1dB steps)
Receiver - serial number 65
Transmitter tested - serial number 53

DETERMINATION OF SYSTEM SENSITIVITY

The system was set up as shown and proper operation was experimentally verified. The 3 bit preamble is shown in figure B. By zooming in on the 3rd bit and running a high level of digital averaging a very stable reading of pulse compression can be made. The peak correlation pulse height is set at modest signal levels as shown in figure C. By adjusting the coarse and fine attenuators the received signal was reduced until the output pulse was reduced by 3dB (.707 x peak voltage). The resulting pulse is shown in figure D.

The resulting minimum signal to the receiver was measured to be -92.1dBm at the system sensitivity limit.

JAMMING MARGIN TEST

After determining the system minimum sensitivity level the coarse attenuator was decreased by 40dB. The CW signal generator was turned on, and for each frequency tested the jamming signal required to drive the output pulse back to 3dB compression was measured. This test was done in 50KHz steps across the passband of the system. Data is shown in appendix B.

FINAL PROCESS GAIN DETERMINATION

The process gain is calculated from the jamming margin test results using the FCC suggested equation Gp=Mj + S/No + Lsys. The required signal to noise at the receiver output (S/No) was shown to be 18dB for this test methodology and system. The maximum allowed system losses of 2dB are assumed. Actual system losses are considerably greater due to significant pass band distortion in the receiver. This distortion occurs due the difficult filter requirements of a receiver that must operate in the vicinity of high powered interference sources (LMS systems) located close to the desired frequency band of the system. The effect of the distortion is reduced with increasing frequency, and can be readily observed by the steady increase in processing gain with frequency.

Measured average processing gain of the system was 13.8 dB (no points discarded)