Circuit Description

Model Number : IHD10100R0WW /GES3081

Model Name : In Home Display

Customer :

Customer Model Number :

Department : CTL

Revision : X1

Date :Jun.30-2010

Number of Pages : 2

Prepared by : _____(Henry Chen)

Approved by : _____(Gordon Qian)

Revision

Rev.	Date.	Prepared by	History
X1	Jun.30	Henry Chen	Initial release

There are three key units in the product:the control unit,the RF module and the LCD display module.

1.Control unit

The key part of the control unit is the MCU (U1). It is a 16-Bit microcontroller with build-in 256KB flash. Its responsibility is to control the whole product:

a. Communicate with the RF module (U2). Exchange data (receive and transmit) via RF module.
b. Send display information to LCD module.
c. Receive the key press information from the key in the front panel.
d. Indicate the status of the product via the LED.
e. Communicate with the EEPROM (U3).

2. RF module

The RF module is a complete ZigBee-ready module with integrated antenna. Its responsibility is to exchange data (receive and transmit) via the 2.4 GHz ISM band RF net. For more details, please read the reference specification of the RF module.

3. LCD display module

The LCD display module(J2) is a FSTN LCD. Its responsibility is to display the information from the MCU.

3. EEPROM

U3 is an EEPROM for storage the status configured by user and other important information.

4. Program port

The J1 is combination program port for program the MCU and the RF module.

5. Power supply

The power input (DC +5V) from J3. U4 is a LDO for voltage regulation. It feeds all the circuits DC +3V.

- End -

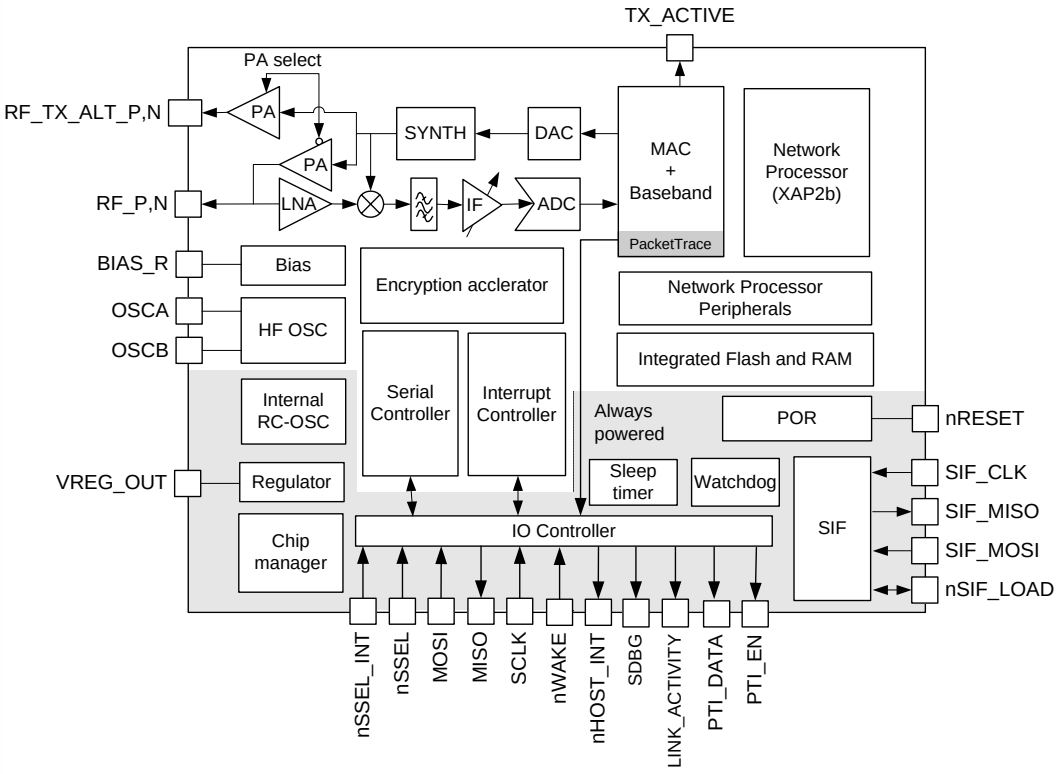
RF module CT-EM2606 CIRCUIT DESCRIPTION

1. **Power Supply**: We can power on the unit though VBRD, because there is a 1.8V regulator in the chip (EM260) and regulate the input power supply to stable 1.8V, so the power supply can range from 2.7 to 3.6V DC.
2. **EM260**: The EM260 integrates a 2.4GHz IEEE 802.15.4-compliant transceiver with a 16-bit net processor (XAP2b core) to run EmberZnet. The transceiver utilizes an efficient architecture that exceeds the dynamic range requirements imposed by the IEEE 802.15.4-2003 standard by over 15dB. The integrated regulator, VCO, loop filter, and power amplifier keep the external component count low.
3. **SKY65337**: SKY65337 is high-efficiency Front-End Module for ZigBee and other 2.4GHz ISM band applications. It contains a 2400-2500MHz high-efficiency transmit path and a low-lose bidirectional path. The transmit path consists of an harmonic filter, an balun and an PA capable of providing +20dbm of power at the antenna port. The bidirectional path consists of a high isolation T/R switch and an balun for low-noise differential port.
4. **TX/RX control**: It is builded of Q1,Q2,R3,R4,R15,R16,R17. The signal of TX is low, U2 set up bidirectional path, U2 can be transmit and receive. The signal of TX is high, U2 set up transmit path.
5. **Antenna**: A PCB's antenna is used to transmit and receive 2.4GHZ carrier signal ,The component of C2,C3,L3 are matched circuit for antenna.

EM260

ZigBee/802.15.4 Network Processor

- *Integrated 2.4GHz, IEEE 802.15.4-compliant transceiver:*
  - Robust RX filtering allows co-existence with IEEE 802.11g and Bluetooth devices
  - - 97.5dBm RX sensitivity (1% PER, 20byte packet)
  - + 3dBm nominal output power
  - Increased radio performance mode (boost mode) gives – 98.5dBm sensitivity and + 5dBm transmit power
  - Integrated VCO and loop filter
  - Secondary TX-only RF port for applications requiring external PA.
- *Integrated IEEE 802.15.4 PHY and MAC*
- *Ember ZigBee-compliant stack running on the dedicated network processor*
- *Controlled by the Host using the EmberZNet Serial Protocol (EZSP)*
  - Standard Serial Interface (allows for connection to a variety of Host microcontrollers)
- *Non-intrusive debug interface (SIF)*
- *Integrated hardware and software support for InSight Development Environment*
- *Dedicated peripherals and integrated memory*
- *Provides integrated RC oscillator for low power operation*
- *Three sleep modes:*
  - Processor idle (automatic)
  - Deep sleep—1.0µA
  - Power down—1.0µA
- *Watchdog timer and power-on-reset circuitry*
- *Integrated AES encryption accelerator*
- *Integrated 1.8V voltage regulator*



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General Description

The EM260 integrates a 2.4GHz, IEEE 802.15.4-compliant transceiver with a 16-bit network processor (XAP2b core) to run EmberZNet, the Ember ZigBee-compliant network stack. The EM260 exposes access to the EmberZNet API across a standard SPI module, allowing application development on a Host processor. This means that the EM260 can be viewed as a ZigBee peripheral connected over a SPI. The XAP2b microprocessor is a power-optimized core integrated in the EM260. It contains integrated Flash and RAM memory along with an optimized peripheral set to enhance the operation of the network stack.

The transceiver utilizes an efficient architecture that exceeds the dynamic range requirements imposed by the IEEE 802.15.4-2003 standard by over 15dB. The integrated receive channel filtering allows for co-existence with other communication standards in the 2.4GHz spectrum such as IEEE 802.11g and Bluetooth. The integrated regulator, VCO, loop filter, and power amplifier keep the external component count low. An optional high-performance radio mode (boost mode) is software selectable to boost dynamic range by a further 3dB.

The EM260 contains embedded Flash and integrated RAM for program and data storage. By employing an effective wear-leveling algorithm, the stack optimizes the lifetime of the embedded Flash, and affords the application the ability to configure stack and application tokens within the EM260.

To maintain the strict timing requirements imposed by ZigBee and the IEEE 802.15.4-2003 standard, the EM260 integrates a number of MAC functions into the hardware. The MAC hardware handles automatic ACK transmission and reception, automatic backoff delay, and clear channel assessment for transmission, as well as automatic filtering of received packets. In addition, the EM260 allows for true MAC level debugging by integrating the Packet Trace Interface.

An integrated voltage regulator, power-on-reset circuitry, sleep timer, and low-power sleep modes are available. The deep sleep and power down modes draws less than 1µA, allowing products to achieve long battery life.

Finally, the EM260 utilizes the non-intrusive SIF module for powerful software debugging and programming of the network processor.

Target applications for the EM260 include:

- *Building automation and control*
- *Home automation and control*
- *Home entertainment control*
- *Asset tracking*

The EM260 can only be purchased with the EmberZNet stack. This technical datasheet details the EM260 features available to customers using it with the EmberZNet stack.

Contents

1 Pin Assignment

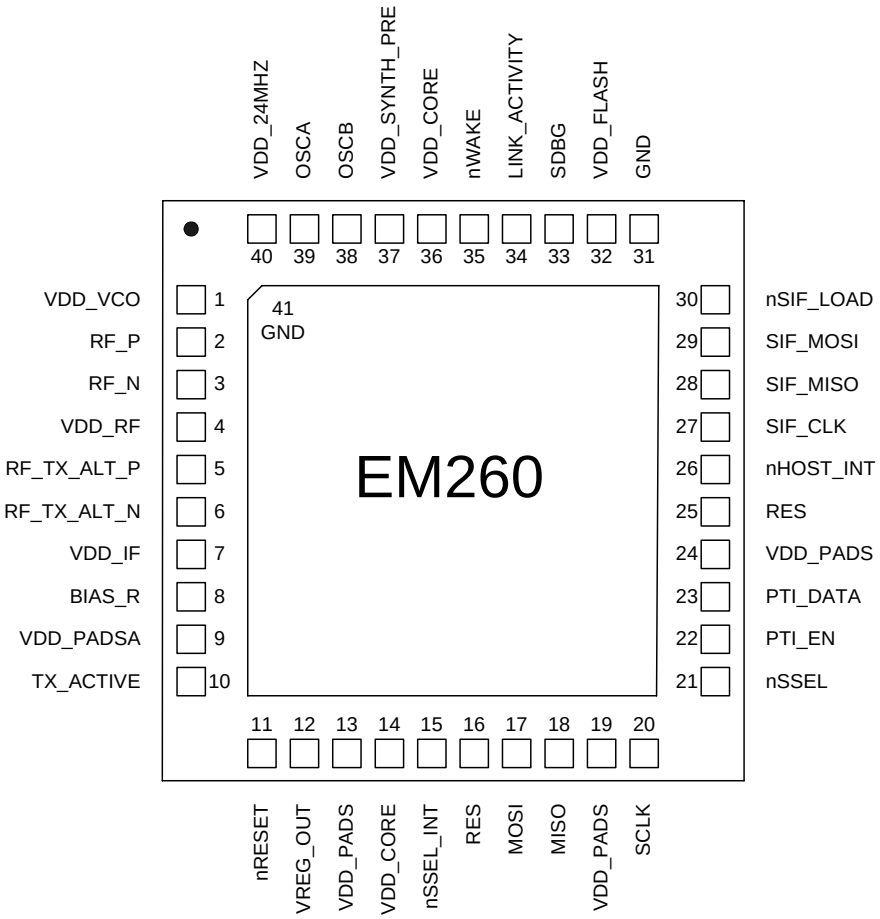

Figure 1. EM260 Pin Assignment

Table 1. Pin Descriptions

Pin #	Signal	Direction	Description
1	VDD_VCO	Power	1.8V VCO supply
2	RF_P	I/O	Differential (with RF_N) receiver input/transmitter output
3	RF_N	I/O	Differential (with RF_P) receiver input/transmitter output
4	VDD_RF	Power	1.8V RF supply (LNA and PA)
5	RF_TX_ALT_P	O	Differential (with RF_TX_ALT_N) transmitter output (optional)
6	RF_TX_ALT_N	O	Differential (with RF_TX_ALT_P) transmitter output (optional)
7	VDD_IF	Power	1.8V IF supply (mixers and filters)
8	BIAS_R	I	Bias setting resistor
9	VDD_PADSA	Power	Analog pad supply (1.8V)
10	TX_ACTIVE	O	Logic-level control for external RX/TX switch The EM260 baseband controls TX_ACTIVE and drives it high (1.8V) when in TX mode. (Refer to Table 6 and section 4.2.2.)

Pin #	Signal	Direction	Description
11	nRESET	I	Active low chip reset (internal pull-up)
12	VREG_OUT	Power	Regulator output (1.8V)
13	VDD_PADS	Power	Pads supply (2.1 – 3.6V)
14	VDD_CORE	Power	1.8V digital core supply
15	nSSEL_INT	I	SPI Slave Select Interrupt (from Host to EM260) This signal must be connected to nSSEL (Pin 21)
16	RES		Reserved for future use, do not connect to any signal.
17	MOSI	I	SPI Data, Master Out / Slave In (from Host to EM260)
18	MISO	O	SPI Data, Master In / Slave Out (from EM260 to Host)
19	VDD_PADS	Power	Pads supply (2.1 – 3.6V)
20	SCLK	I	SPI Clock (from Host to EM260)
21	nSSEL	I	SPI Slave Select (from Host to EM260)
22	PTI_EN	O	Frame signal of Packet Trace Interface (PTI)
23	PTI_DATA	O	Data signal of Packet Trace Interface (PTI)
24	VDD_PADS	Power	Pads supply (2.1 – 3.6V)
25	RES		Reserved for future use, do not connect to any signal.
26	nHOST_INT	O	Host Interrupt signal (from EM260 to Host)
27	SIF_CLK	I	Serial Interface, Clock (internal pull down)
28	SIF_MISO	O	Serial Interface, Master In / Slave Out
29	SIF_MOSI	I	Serial Interface, Master Out / Slave In
30	nSIF_LOAD	I/O	Serial Interface, load strobe (open collector with internal pull up)
31	GND	Power	Ground Supply
32	VDD_FLASH	Power	1.8V Flash memory supply
33	SDBG	O	Spare Debug signal
34	LINK_ACTIVITY	O	Link and Activity signal
35	nWAKE	I	Wake Interrupt signal (from Host to EM260)
36	VDD_CORE	Power	1.8V digital core supply
37	VDD_SYNTH_PRE	Power	1.8V synthesizer and prescalar supply
38	OSCB	I/O	24MHz crystal oscillator or left open for when using an external clock input on OSCA
39	OSCA	I/O	24MHz crystal oscillator or external clock input
40	VDD_24MHZ	Power	1.8V high-frequency oscillator supply
41	GND	Ground	Ground supply pad in the bottom center of the package forms Pin 41 (see the *EM260 Reference Design* for PCB considerations)

2 Top-Level Functional Description

Figure 2 shows a detailed block diagram of the EM260.

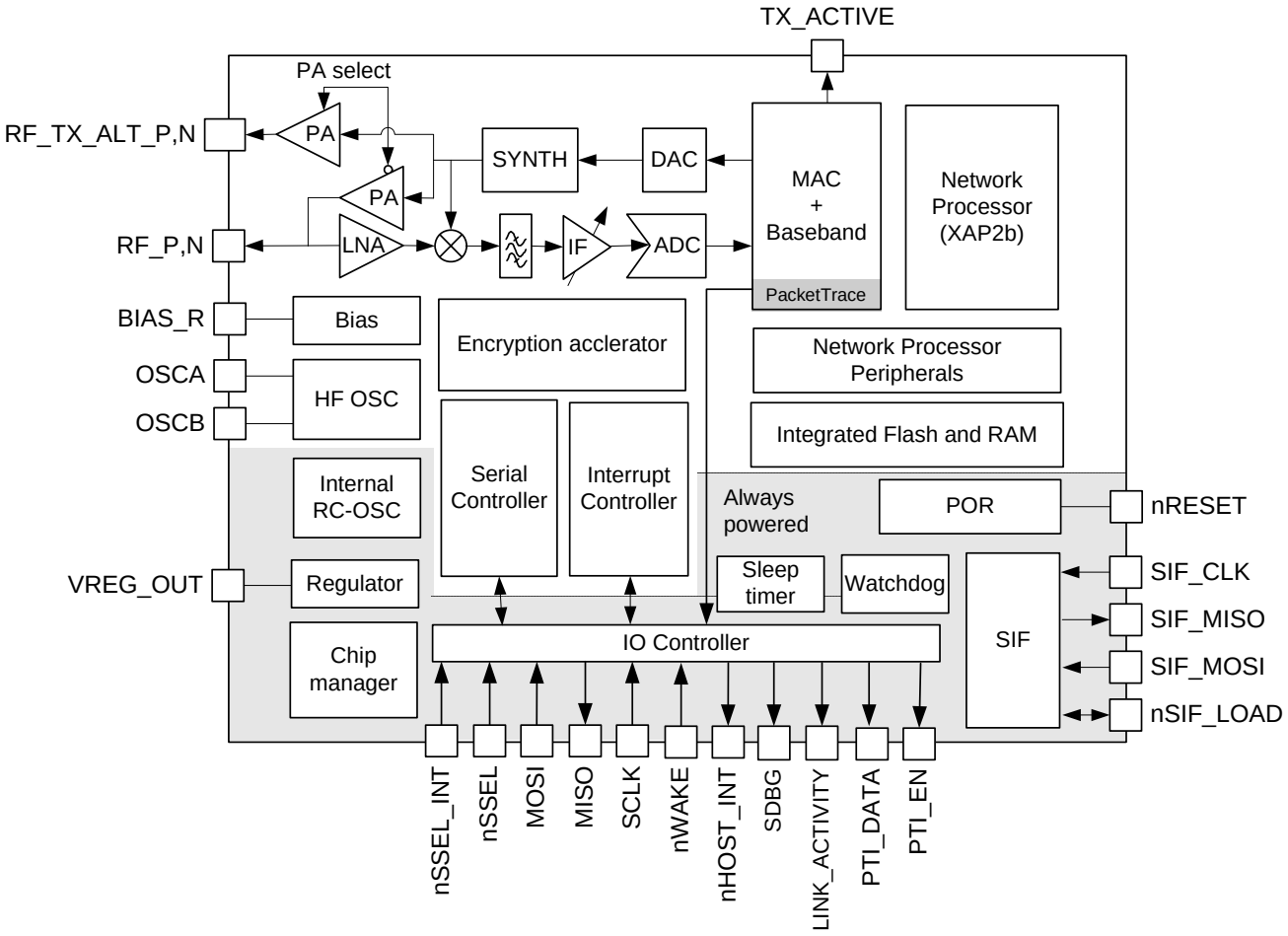

Figure 2. EM260 Block Diagram

The radio receiver is a low-IF, super-heterodyne receiver. It utilizes differential signal paths to minimize noise interference, and its architecture has been chosen to optimize co-existence with other devices within the 2.4GHz band (namely, IEEE 802.11g and Bluetooth). After amplification and mixing, the signal is filtered and combined prior to being sampled by an ADC.

The digital receiver implements a coherent demodulator to generate a chip stream for the hardware-based MAC. In addition, the digital receiver contains the analog radio calibration routines and control of the gain within the receiver path.

The radio transmitter utilizes an efficient architecture in which the data stream directly modulates the VCO. An integrated PA boosts the output power. The calibration of the TX path as well as the output power is controlled by digital logic. If the EM260 is to be used with an external PA, the TX_ACTIVE signal should be used to control the timing of the external switching logic.

The integrated 4.8 GHz VCO and loop filter minimize off-chip circuitry. Only a 24MHz crystal with its loading capacitors is required to properly establish the PLL reference signal.

The MAC interfaces the data memory to the RX and TX baseband modules. The MAC provides hardware-based IEEE 802.15.4 packet-level filtering. It supplies an accurate symbol time base that minimizes the synchroniza-

tion effort of the software stack and meets the protocol timing requirements. In addition, it provides timer and synchronization assistance for the IEEE 802.15.4 CSMA-CA algorithm.

The EM260 integrates hardware support for a Packet Trace module, which allows robust packet-based debug. This element is a critical component of InSight Desktop, the Ember software IDE, providing advanced network debug capability when coupled with the InSight Adapter.

The EM260 integrates a 16-bit XAP2b microprocessor developed by Cambridge Consultants Ltd. This power-efficient, industry-proven core provides the appropriate level of processing power to meet the needs of the Ember ZigBee-compliant stack, EmberZNet. In addition, the SIF module provides a non-intrusive programming and debug interface allowing for real-time application debugging.

The EM260 exposes the Ember Serial API over the SPI, which allows application development to occur on a Host microcontroller of choice. In addition to the four SPI signals, two additional signals, nHOST_INT and nWAKE, provide an easy-to-use handshake mechanism between the Host and the EM260.

The integrated voltage regulator generates a regulated 1.8V reference voltage from an unregulated supply voltage. This voltage is decoupled and routed externally to supply the 1.8V to the core logic. In addition, an integrated POR module allows for the proper cold start of the EM260.

The EM260 contains one high-frequency (24MHz) crystal oscillator and, for low-power operation, a second low-frequency internal 10 kHz oscillator.

The EM260 contains two power domains. The always-powered High Voltage Supply is used for powering the GPIO pads and critical chip functions. The rest of the chip is powered by a regulated Low Voltage Supply which can be disabled during deep sleep to reduce the power consumption.

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 2 lists the absolute maximum ratings for the EM260.

Table 2. Absolute Maximum Ratings

Parameter	Test Conditions	Min.	Max.	Unit
Regulator voltage (VDD_PADS)		- 0.3	3.6	V
Core voltage (VDD_24MHZ, VDD_VCO, VDD_RF, VDD_IF, VDD_PADSA, VDD_FLASH, VDD_SYNTH_PRE, VDD_CORE)		- 0.3	2.0	V
Voltage on RF_P,N; RF_TX_ALT_P,N		- 0.3	3.6	V
Voltage on nSSEL_INT, MOSI, MISO, SCLK, nSSEL, PTI_EN, PTI_DATA, nHOST_INT, SIF_CLK, SIF_MISO, SIF_MOSI, nSIF_LOAD, SDBG, LINK_ACTIVITY, nWAKE, nRESET, VREG_OUT		- 0.3	VDD_PADS+0.3	V
Voltage on TX_ACTIVE, BIAS_R, OSCA, OSCB		- 0.3	VDD_CORE+0.3	V
Storage temperature		- 40	+ 140	°C

3.2 Recommended Operating Conditions

Table 3 lists the rated operating conditions of the EM260.

Table 3. Operating Conditions

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Regulator input voltage (VDD_PADS)		2.1		3.6	V
Core input voltage (VDD_24MHZ, VDD_VCO, VDD_RF, VDD_IF, VDD_PADSA, VDD_FLASH, VDD_SYNTH_PRE, VDD_CORE)		1.7	1.8	1.9	V
Temperature range		- 40		+ 85	°C

3.3 Environmental Characteristics

Table 4 lists the environmental characteristics of the EM260.

Table 4. Environmental Characteristics

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ESD (human body model)	On any Pin	- 2		+ 2	kV
ESD (charged device model)	Non-RF Pins	- 400		+ 400	V
ESD (charged device model)	RF Pins	- 225		+ 225	V
Moisture Sensitivity Level (MSL)			TBD		

3.4 DC Electrical Characteristics

Table 5 lists the DC electrical characteristics of the EM260.

Table 5. DC Characteristics

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Regulator input voltage (VDD_PADS)		2.1		3.6	V
Power supply range (VDD_CORE)	Regulator output or external input	1.7	1.8	1.9	V
Deep Sleep Current					
Quiescent current, including internal RC oscillator	At 25° C			1.0	µA
RX Current					
Radio receiver, MAC, and baseband (boost mode)			29.0		mA
Radio receiver, MAC, and baseband			27.0		mA
CPU, RAM, and Flash memory	At 25° C and 1.8V core		8.5		mA
Total RX current (= $I_{\text{Radio receiver, MAC and baseband, CPU}}$ + $I_{\text{RAM, and Flash memory}}$)	At 25° C, VDD_PADS = 3.0V		35.5		mA
TX Current					
Radio transmitter, MAC, and baseband (boost mode)	At max. TX power (+ 5dBm typical)		33.0		mA
Radio transmitter, MAC, and baseband	At max. TX power (+ 3dBm typical)		27.0		mA
	At 0 dBm typical		24.3		mA
	At min. TX power (- 32dBm typical)		19.5		mA
CPU, RAM, and Flash memory	At 25° C, VDD_PADS = 3.0V		8.5		mA
Total TX current (= $I_{\text{Radio transmitter, MAC and baseband, CPU}}$ + $I_{\text{RAM, and Flash memory}}$)	At 25° C and 1.8V core; max. power out		35.5		mA

3.5 Digital I/O Specifications

Table 6 contains the digital I/O specifications for the EM260. The digital I/O power (named VDD_PADS) comes from three dedicated pins (pins 13, 19, and 24). The voltage applied to these pins sets the I/O voltage.

Table 6. Digital I/O Specifications

Parameter	Name	Min.	Typ.	Max.	Unit
Voltage supply	VDD_PADS	2.1		3.6	V
Input voltage for logic 0	V_{IL}	0		0.2 x VDD_PADS	V
Input voltage for logic 1	V_{IH}	0.8 x VDD_PADS		VDD_PADS	V
Input current for logic 0	I_{IL}			-0.5	µA
Input current for logic 1	I_{IH}			0.5	µA
Input pull-up resistor value	R_{IPU}		30		kΩ
Input pull-down resistor value	R_{IPD}		30		kΩ
Output voltage for logic 0	V_{OL}	0		0.18 x VDD_PADS	V
Output voltage for logic 1	V_{OH}	0.82 x VDD_PADS		VDD_PADS	V
Output source current (standard current pad)	I_{OHS}			4	mA
Output sink current (standard current pad)	I_{OLS}			4	mA
Output source current (high current pad: pins 33, 34, and 35)	I_{OHH}			8	mA
Output sink current (high current pad: pins 33, 34, and 35)	I_{OLH}			8	mA
Total output current (for I/O pads)	$I_{OH} + I_{OL}$			40	mA
Input voltage threshold for OSCA		0.2 x VDD_CORE		0.8 x VDD_PADS	V
Output voltage level (TX_ACTIVE)		0.18 x VDD_CORE		0.82 x VDD_CORE	V
Output source current (TX_ACTIVE)				1	mA

3.6 RF Electrical Characteristics

3.6.1 Receive

Table 7 lists the key parameters of the integrated IEEE 802.15.4 receiver on the EM260.

Note: Receive Measurements were collected with Ember's EM260 Reference Design at 2440MHz. The Typical number indicates one standard deviation above the mean.

Table 7. Receive Characteristics

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Frequency range		2400		2500	MHz
Sensitivity (boost mode)	1% PER, 20byte packet defined by IEEE 802.15.4	- 93	- 98.5		dBm
Sensitivity	1% PER, 20byte packet defined by IEEE 802.15.4	- 92	- 97.5		dBm
High-side adjacent channel rejection	IEEE 802.15.4 signal at -82dBm		35		dB
Low-side adjacent channel rejection	IEEE 802.15.4 signal at - 82dBm		35		dB
2nd high-side adjacent channel rejection	IEEE 802.15.4 signal at - 82dBm		40		dB
2nd low-side adjacent channel rejection	IEEE 802.15.4 signal at - 82dBm		40		dB
Channel rejection for all other channels	IEEE 802.15.4 signal at - 82dBm		40		dB
802.11g rejection centered at + 12MHz or - 13MHz	IEEE 802.15.4 signal at - 82dBm		40		dB
Maximum input signal level for correct operation (low gain)		0			dBm
Image suppression			30		dB
Co-channel rejection	IEEE 802.15.4 signal at - 82dBm		- 6		dBc
Relative frequency error (2 x 40 ppm required by IEEE 802.15.4)		- 120		+ 120	ppm
Relative timing error (2 x 40 ppm required by IEEE 802.15.4)		- 120		+ 120	ppm
Linear RSSI range			40		dB

3.6.2 Transmit

Table 8 lists the key parameters of the integrated IEEE 802.15.4 transmitter on the EM260.

Note: Transmit Measurements were collected with Ember's EM260 Reference Design at 2440MHz. The Typical number indicates one standard deviation below the mean.

Table 8. Transmit Characteristics

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Maximum output power (boost mode)	At highest power setting		5		dBm
Maximum output power	At highest power setting	0	3		dBm
Minimum output power	At lowest power setting		- 32		dBm
Error vector magnitude	As defined by IEEE 802.15.4, which sets a 35% maximum		15	25	%
Carrier frequency error		- 40		+ 40	ppm
Load impedance			200		Ω
PSD mask relative	3.5MHz away	- 20			dB
PSD mask absolute	3.5MHz away	- 30			dBm

3.6.3 Synthesizer

Table 9 lists the key parameters of the integrated synthesizer on the EM260.

Table 9. Synthesizer Characteristics

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Frequency range		2400		2500	MHz
Frequency resolution			11.7		kHz
Lock time	From off, with correct VCO DAC setting			100	µs
Relock time	Channel change or RX/TX turnaround (IEEE 802.15.4 defines 192µs turnaround time)			100	µs
Phase noise at 100kHz			- 71		dBc/Hz
Phase noise at 1MHz			- 91		dBc/Hz
Phase noise at 4MHz			- 103		dBc/Hz
Phase noise at 10MHz			- 111		dBc/Hz

4 Functional Description

The EM260 connects to the Host microcontroller through a standard SPI interface. The EmberZNet Serial Protocol (EZSP) has been defined to allow an application to be written on a host microcontroller of choice. Therefore, the EM260 comes with a license to EmberZNet, the Ember ZigBee-compliant software stack. The following brief description of the hardware modules provides the necessary background on the operation of the EM260. For more information, contact www.ember.com/support.

4.1 Receive (RX) Path

The EM260 RX path spans the analog and digital domains. The RX architecture is based on a low-IF, super-heterodyne receiver. It utilizes differential signal paths to minimize noise interference. The input RF signal is mixed down to the IF frequency of 4MHz by I and Q mixers. The output of the mixers is filtered and combined prior to being sampled by a 12Msps ADC. The RX filtering within the RX path has been designed to optimize the co-existence of the EM260 with other 2.4GHz transceivers, such as the IEEE 802.11g and Bluetooth.

4.1.1 RX Baseband

The EM260 RX baseband (within the digital domain) implements a coherent demodulator for optimal performance. The baseband demodulates the O-QPSK signal at the chip level and synchronizes with the IEEE 802.15.4-2003 preamble. Once a packet preamble is detected, it de-spreads the demodulated data into 4-bit symbols. These symbols are buffered and passed to the hardware-based MAC module for filtering.

In addition, the RX baseband provides the calibration and control interface to the analog RX modules, including the LNA, RX Baseband Filter, and modulation modules. The EmberZNet software includes calibration algorithms which use this interface to reduce the effects of process and temperature variation.

4.1.2 RSSI and CCA

The EM260 calculates the RSSI over an 8-symbol period as well as at the end of a received packet. It utilizes the RX gain settings and the output level of the ADC within its algorithm.

The EM260 RX baseband provides support for the IEEE 802.15.4-2003 required CCA methods summarized in Table 10. Modes 1, 2, and 3 are defined by the 802.15.4-2003 standard; Mode 0 is a proprietary mode.

Table 10. CCA Mode Behavior

CCA Mode	Mode Behavior
0	Clear channel reports busy medium if either carrier sense OR RSSI exceeds their thresholds.
1	Clear channel reports busy medium if RSSI exceeds its threshold.
2	Clear channel reports busy medium if carrier sense exceeds its threshold.
3	Clear channel reports busy medium if both RSSI and carrier sense exceed their thresholds.

4.2 Transmit (TX) Path

The EM260 transmitter utilizes both analog circuitry and digital logic to produce the O-QPSK modulated signal. The area-efficient TX architecture directly modulates the spread symbols prior to transmission. The differential signal paths increase noise immunity and provide a common interface for the external balun.

4.2.1 TX Baseband

The EM260 TX baseband (within the digital domain) performs the spreading of the 4-bit symbol into its IEEE 802.15.4-2003-defined 32-chip I and Q sequence. In addition, it provides the interface for software to perform the calibration of the TX module in order to reduce process, temperature, and voltage variations.

4.2.2 TX_ACTIVE Signal

Even though the EM260 provides an output power suitable for most ZigBee applications, some applications will require an external power amplifier (PA). Due to the timing requirements of IEEE 802.15.4-2003, the EM250 provides a signal, TX_ACTIVE, to be used for external PA power management and RF Switching logic. When in TX, the TX Baseband drives TX_ACTIVE high (as described in Table 6). When in RX, the TX_ACTIVE signal is low. If an external PA is not required, then the TX_ACTIVE signal should be connected to GND through a 100k Ohm resistor, as shown in the application circuit in Figure 12.

4.3 Integrated MAC Module

The EM260 integrates critical portions of the IEEE 802.15.4-2003 MAC requirements in hardware. This allows the EM260 to provide greater bandwidth to application and network operations. In addition, the hardware acts as a first-line filter for non-intended packets. The EM260 MAC utilizes a DMA interface to RAM memory to further reduce the overall microcontroller interaction when transmitting or receiving packets.

When a packet is ready for transmission, the software configures the TX MAC DMA by indicating the packet buffer RAM location. The MAC waits for the backoff period, then transitions the baseband to TX mode and performs channel assessment. When the channel is clear, the MAC reads data from the RAM buffer, calculates the CRC, and provides 4-bit symbols to the baseband. When the final byte has been read and sent to the baseband, the CRC remainder is read and transmitted.

The MAC resides in RX mode most of the time, and different format and address filters keep non-intended packets from using excessive RAM buffers, as well as preventing the EM260 CPU from being interrupted. When the reception of a packet begins, the MAC reads 4-bit symbols from the baseband and calculates the CRC. It assembles the received data for storage in a RAM buffer. A RX MAC DMA provides direct access to the RAM memory. Once the packet has been received, additional data is appended to the end of the packet in the RAM buffer space. The appended data provides statistical information on the packet for the software stack.

The primary features of the MAC are:

- CRC generation, appending, and checking
- Hardware timers and interrupts to achieve the MAC symbol timing
- Automatic preamble, and SFD pre-pended to a TX packet
- Address recognition and packet filtering on received packets
- Automatic acknowledgement transmission
- Automatic transmission of packets from memory
- Automatic transmission after backoff time if channel is clear (CCA)
- Automatic acknowledgement checking
- Time stamping of received and transmitted messages
- Attaching packet information to received packets (LQI, RSSI, gain, time stamp, and packet status)
- IEEE 802.15.4-2003 timing and slotted/unslotted timing

4.4 Packet Trace Interface (PTI)

The EM260 integrates a true PHY-level PTI for effective network-level debugging. This two-signal interface monitors all the PHY TX and RX packets (in a non-intrusive manner) between the MAC and baseband modules. It is an asynchronous 500kbps interface and cannot be used to inject packets into the PHY/MAC interface. The

two signals from the EM260 are the frame signal (PTI_EN) and the data signal (PTI_DATA). The PTI is supported by InSight Desktop.

4.5 XAP2b Microprocessor

The EM260 integrates the XAP2b microprocessor developed by Cambridge Consultants Ltd., making it a true network processor solution. The XAP2b is a 16-bit Harvard architecture processor with separate program and data address spaces. The word width is 16 bits for both the program and data sides.

The standard XAP2 microprocessor and accompanying software tools have been enhanced to create the XAP2b microprocessor used in the EM260. The XAP2b adds data-side byte addressing support to the XAP2 allowing for more productive usage of RAM and optimized code.

The XAP2b clock speed is 12MHz. When used with the EmberZNet stack, firmware is loaded into Flash memory over the air or by a serial link using a built-in bootloader in a reserved area of the Flash. Alternatively, firmware may be loaded via the SIF interface with the assistance of RAM-based utility routines also loaded via SIF.

4.6 Embedded Memory

The EM260 contains embedded Flash and RAM memory for firmware storage and execution. In addition it partitions a portion of the Flash for Simulated EEPROM and token storage.

4.6.1 Simulated EEPROM

The Ember stack reserves a section of Flash memory to provide Simulated EEPROM storage area for stack and customer tokens. The Flash cell has been qualified for a data retention time of >100 years at room temperature and is rated to have a guaranteed 1,000 write/erase cycles. Because the Flash cells are qualified for up to 1,000 write cycles, the Simulated EEPROM implements an effective wear-leveling algorithm which effectively extends the number of write cycles for individual tokens.

The number of set-token operations is finite due to the write cycle limitation of the Flash. It is not possible to guarantee an exact number of set-token operations because the life of the Simulated EEPROM depends on which tokens are written and how often.

The EM260 stores non-volatile information necessary for network operation as well as 8 tokens available to the Host (see section 6.2.6, Tokens). The majority of internal tokens are only written when the EM260 performs a network join or leave operation. As a simple ballpark estimate of possible set-token operations, consider an EM260 in a stable network (no joins or leaves) not sending any messages and the Host is using only one of the 8-byte tokens available to it. Under this scenario, a very rough estimate results in approximately 330,000 possible set-token operations. The number of possible set-token calls, though, depends on which tokens are being set, so the ratios of set-token calls for each token plays a large factor. A very rough estimate for the total number of times an App token can bet set is approximately 320,000.

These estimates would typically increase if the EM260 is kept closer to room temperature, since the 1,000 guaranteed write cycles of the Flash is for across temperature.

4.6.2 Flash Information Area (FIA)

The EM260 also includes a separate 1024-byte FIA that can be used for storage of data during manufacturing, including serial numbers and calibration values. Programming of this special Flash page can only be enabled using the SIF interface to prevent accidental corruption or erasure. The EmberZNet stack reserves a small portion of this space for its own use and in addition makes eight manufacturing tokens available to the application. See section 6.2.6, Tokens, for more information.

4.7 Encryption Accelerator

The EM260 contains a hardware AES encryption engine that is attached to the CPU using a memory-mapped interface. NIST-based CCM, CCM*, CBC-MAC, and CTR modes are implemented in hardware. These modes are described in the IEEE 802.15.4-2003 specification, with the exception of CCM*, which is described in the ZigBee Security Services Specification 1.0. The EmberZNet stack implements a security API for applications that require security at the application level.

4.8 Reset Detection

The EM260 contains multiple reset sources. The reset event is logged into the reset source register, which lets the CPU determine the cause of the last reset. The following reset causes are detected:

- Power-on-Reset
- Watchdog
- PC rollover
- Software reset
- Core Power Dip

4.9 Power-on-Reset (POR)

Each voltage domain (1.8V Digital Core Supply VDD_CORE and Pads Supply VDD_PADS) has a power-on-reset (POR) cell.

The VDD_PADS POR cell holds the always-powered high-voltage domain in reset until the following conditions have been met:

- The high-voltage Pads Supply VDD_PADS voltage rises above a threshold.
- The internal RC clock starts and generates three clock pulses.
- The 1.8V POR cell holds the main digital core in reset until the regulator output voltage rises above a threshold.

Additionally, the digital domain counts 1,024 clock edges on the 24MHz crystal before releasing the reset to the main digital core.

Table 11 lists the features of the EM260 POR circuitry.

Table 11. POR Specifications

Parameter	Min.	Typ.	Max.	Unit
VDD_PADS POR release	1.0	1.2	1.4	V
VDD_PADS POR assert	0.5	0.6	0.7	V
1.8V POR release	1.35	1.5	1.65	V
1.8V POR hysteresis	0.08	0.1	0.12	V

4.10 Clock Sources

The EM260 integrates two oscillators: a high-frequency 24MHz crystal oscillator and a low-frequency internal 10kHz RC oscillator.

4.10.1 High-Frequency Crystal Oscillator

The integrated high-frequency crystal oscillator requires an external 24MHz crystal with an accuracy of ±40ppm. Based upon the application Bill of Materials and current consumption requirements, the external crystal can cover a range of ESR requirements. For a lower ESR, the cost of the crystal increases but the overall current consumption decreases. Likewise, for higher ESR, the cost decreases but the current consumption increases. Therefore, the designer can choose a crystal to fit the needs of the application.

Table 12 lists the specifications for the high-frequency crystal.

Table 12. High-Frequency Crystal Specifications

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Frequency			24		MHz
Duty cycle		40		60	%
Phase noise from 1kHz to 100kHz				- 120	dBc/Hz
Accuracy	Initial, temperature, and aging	- 40		+ 40	ppm
Crystal ESR	Load capacitance of 10pF			100	Ω
Crystal ESR	Load capacitance of 18pF			60	Ω
Start-up time to stable clock (max. bias)				1	ms
Start-up time to stable clock (optimum bias)				2	ms
Current consumption	Good crystal: 20Ω ESR, 10pF load		0.2	0.3	mA
Current consumption	Worst-case crystals (60Ω, 18pF or 100Ω, 10pF)			0.5	mA
Current consumption	At maximum bias			1	mA

4.10.2 Internal RC Oscillator

The EM260 has a low-power, low-frequency RC oscillator that runs all the time. Its nominal frequency is 10kHz. It is divided down to 1kHz using a variable divider to allow software to accurately calibrate it. This calibrated clock is used by the sleep timer.

Timekeeping accuracy depends on temperature fluctuations the chip is exposed to, power supply impedance, and the calibration interval, but in general it will be better than 150ppm (including crystal error of 40ppm).

Table 13 lists the specifications of the RC oscillator.

Table 13. RC Oscillator Specifications

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Frequency			10		kHz
Analog trim steps			1		kHz
Frequency variation with supply	For a voltage drop from 3.6V to 3.1V or 2.6V to 2.1V		0.75	1.5	%

4.11 Random Number Generator

The EM260 allows for the generation of random numbers by exposing a randomly generated bit from the RX ADC. Analog noise current is passed through the RX path, sampled by the receive ADC, and stored in a register. The value contained in this register could be used to seed a software-generated random number. The EmberZNet stack utilizes these random numbers to seed the Random MAC Backoff and Encryption Key Generators.

4.12 Watchdog Timer

The EM260 contains an internal watchdog timer clocked from the internal oscillator. If the timer reaches its time-out value of approximately 2 seconds, it will reset the EM260. This reset signal cannot be routed externally to the Host.

The EM260 firmware will periodically restart the watchdog timer while the firmware is running normally. The Host cannot effect or configure the watchdog timer.

4.13 Sleep Timer

The 16-bit sleep timer is contained in the always-powered digital block. The clock source for the sleep timer is a calibrated 1kHz clock. The frequency is slowed down with a 2^N prescaler to generate a final timer resolution of 1ms. With a 1ms tick and a 16-bit timer, the timer wraps about every 65.5 seconds. The EmberZNet stack appropriately handles timer wraps allowing the Host to order a theoretical maximum sleep delay of 4 million seconds.

4.14 Power Management

The EM260 supports four different power modes: active, idle, deep sleep, and power down.

Active mode is the normal, operating state of the EM260.

While in idle mode, code execution halts until any interrupt occurs. All modules of the EM260 including the radio continue to operate normally. The EmberZNet stack automatically invokes idle as appropriate.

Deep sleep mode and power down mode both power off most of the EM260, including the radio, and leave only the critical chip functions powered. The internal regulator is disabled and VREG_OUT is turned off. All output signals are maintained in a frozen state. Upon waking from deep sleep or power down mode, the internal regulator is reenabled. Deep sleep and power down result in the same sleep current consumption. The two sleep modes differ as follows: the EM260 can wake on both an internal timer and an external signal from deep sleep mode; power down mode can only wake on an external signal.