Intersil Corporation Certification Report

Testing for Compliance with FCC Rules 15-247e

Theoretical BER Curves for the IEEE 1 and 2Mbps Modulations

11Mbps Channel 1 Processing Gain

11Mbps Channel 6 Processing Gain

11Mbps Channel 11 Processing Gain

2Mbps Channel 6 Processing Gain

Certification Report on Compliance with Respect to FCC CFR 47, Para. 15.247(e)
Measurement of Processing Gain of Direct Sequence Spread Spectrum

Product: Intersil HWB3163 Rev B WLAN PCMCIA

Tested by: Intersil Corp.
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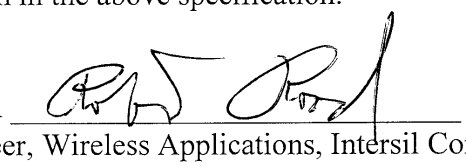
Date: October 14, 1999

ENGINEERING SUMMARY AND CERTIFICATION

This report contains the results of the engineering evaluation performed on an Intersil Wireless LAN PC Card, Model HWB3163 Rev B. The tests were carried out in accordance with FCC CFR 47, Para. 15.247(e).

Robert Rood is a Wireless Applications Staff Engineer at Intersil Corporation. Intersil is a new independent company as of August 13, 1999, previously known as Harris Semiconductor. Robert received a BSEE from the University of Florida in 1979 and his Masters of Science in Engineering Management from Florida Tech in 1988. He joined Harris Semiconductor in 1983 as a Test Engineer after 3 ½ years with Burr Brown Research Corp. He was promoted to Test Staff Engineer in 1989 and moved into Applications in 1991 where he has built on his experience with high speed linear and currently leads the wireless radio development team.

I certify that this data was taken by me or at my direction and to the best of my knowledge and belief, is true and accurate. Based on the test results, it is certified that the product meets the requirements as set forth in the above specification.

Submitted by: Robert Rood  Date: Nov 11, 1999
Staff Engineer, Wireless Applications, Intersil Corp.

Processing Gain of a Direct Sequence Spread Spectrum, FCC CFR 47, Para. 15.247(e)

Product Name: HWB3163 Rev B

FCC Requirements: The processing gain of a direct sequence system shall be at least 10dB. The processing gain shall be determined from the ratio in dB of the signal-to-noise ratio with the system spreading code turned off to the signal-to-noise ratio with the system spreading code turned on, as measured at the demodulated output of the receiver.

Environmental Conditions: Room Temperature and Humidity: 25°C and 50%.

Power Input: DC Power from a laptop computer.

Test Equipment:
Hewlett Packard Spectrum Analyzer, Model HP8593E 9kHz to 22GHz
Marconi Signal Generator, Model 2031, Freq. Range 10kHz to 2.7GHz
Hewlett Packard Power Meter, Model HP438A
Hewlett Packard Power Sensor, Model HP8481D, -20 to -70dBm
Hewlett Packard Attenuators, Model HP8493A, 6dB and 10dB
Hewlett Packard Step Attenuator, Model HP8494A, 1dB steps
Hewlett Packard Step Attenuator, Model HP8495D, 10dB steps
Hewlett Packard Power Splitter, Model HP11667B
Campaq Laptop Computers (Qty 2), Model Armada 1700

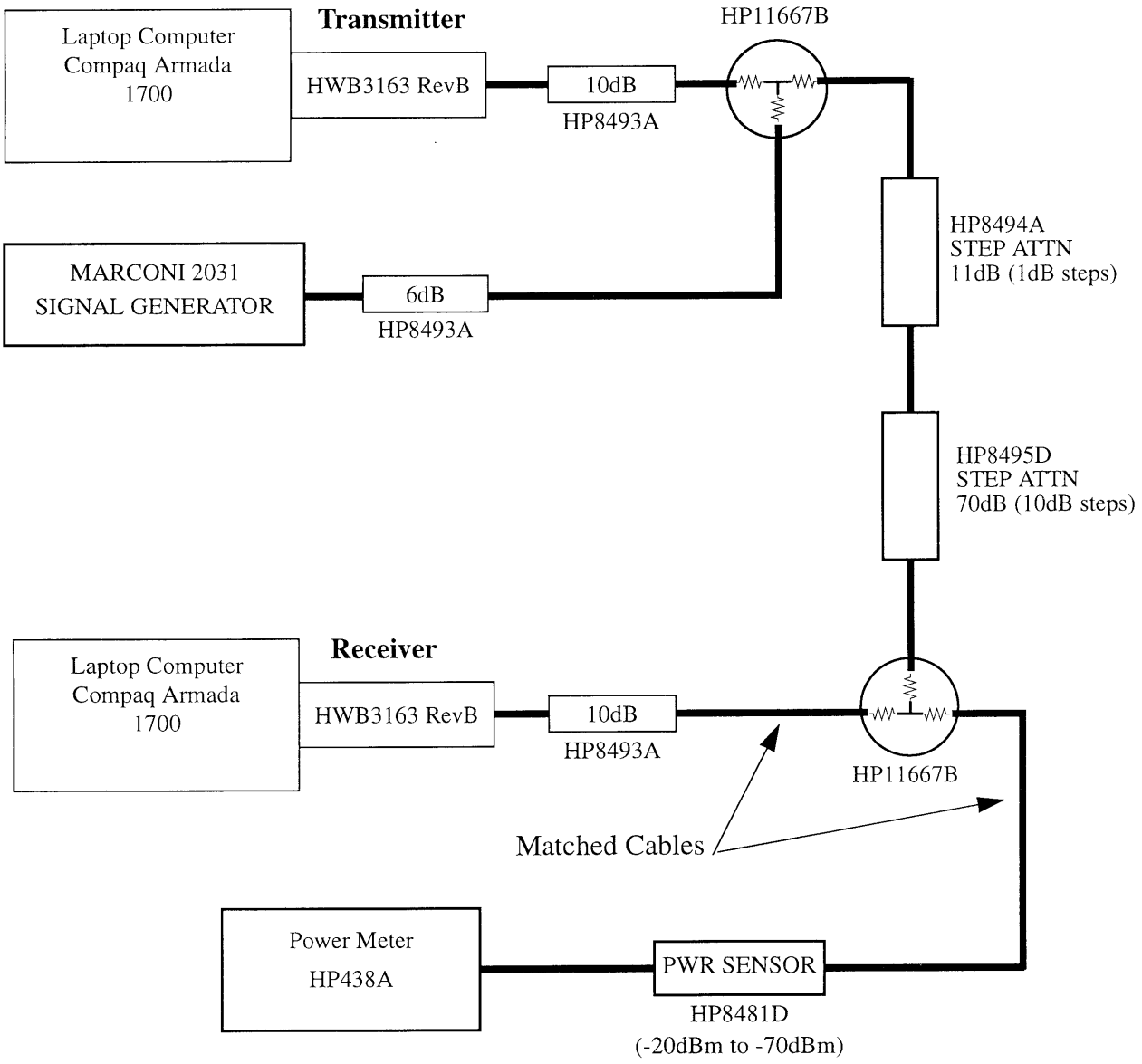
Method of Measurement: Jamming Margin Method. The processing gain may be measured using the CW jamming margin method. Figure 1 shows the test configuration. The test consists of stepping a signal generator in 50kHz increments across the passband of the system. At each point, the generator level required to produce the recommended Bit Error Rate (BER) is recorded. This level is the jammer level. The output power of the transmitting unit is measured at the same point. The Jammer to Signal (J/S) ratio is the calculated. Discard the worst 20% of the J/S data points. The lowest remaining J/S ratio is used when calculating the Process Gain.

Theoretical Calculation: The use of 8% FER frame error rate (or PER packet error rate) as a substitute for the recommended BER bit error rate and the ideal signal to noise ratio per symbol (Es/No) is derived in the attached documents; "Testing for compliance with FCC rules 15-247e", by Carl Andren and "Theoretical BER curves for the IEEE 1 and 2 Mbps modulations" by Carl Andren.

Engineering Summary: Processing Gain Results Summary

Frequency Channel	Data Rate(Mbps)	Gp (dB)
1	11	11.5
6	11	11.4
11	11	12
6	2	12.5

Processing Gain Test Set Up



Testing for compliance with FCC rules 15-247e

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Scope

This report presents the test procedure, test configuration and test data associated with a FCC Part 15.247 (e) Jamming Margin test for the indirect measurement of processing gain.

Applicable Reference Documents.

1. "Operation within the bands 902-928 MHz, 2400-2483.5, and 5725-5850 MHz" ***Title 47 Part 15 section 247 (e) Code of Federal Regulations***. **(47 CFR 15.247).**

2. "Report and Order: Amendment of Parts 2 and 15 of the Commission's Rules Regarding Spread Spectrum Transmitters. Appendix C: 'Guidance on Measurements for Direct Sequence Spread Spectrum Systems" ***FCC 97-114. ET Docket No. 96-8, RM-8435, RM-8608, RM-8609.***

3. "HFA3861A Direct Sequence Spread Spectrum Baseband Processor" ***Harris Corporation Semiconductor Sector Preliminary Data Sheet***, Melbourne FL, July 1999.

4. " M-ary Orthogonal Keying BER Curve",

Test Background and Procedure.

According to FCC regulations [1], a direct sequence spread spectrum system must have a processing gain, G_p of at least 10 dB. Compliance to this requirement can be shown by demonstrating a relative bit-error-ratio (BER) performance improvement (and corresponding signal to noise ratio per symbol improvement of at least 10 dB) between the case where spread spectrum processes (coding, modulation) are engaged relative to

the processes being bypassed. In some practical systems, the spread spectrum processing cannot simply be bypassed. In these cases, the processing gain can be indirectly measured by a jamming margin test [2]. In accordance with the new NPRM 99-231, if the vendor has a system with less than 10 chips per symbol, the CW jamming results must be supported by a theoretical explanation of the system processing gain.

Theoretical calculations

The processing gain is related to the jamming margin as follows [2]:

$$G_p = \left(\frac{S}{N}\right)_{output} + \left(\frac{J}{S}\right) + L_{system}$$

Where $BER_{REFERENCE}$ is the reference bit error ratio with its corresponding, theoretical output signal to noise ratio per symbol, $(S/N)_{output}$, (J/S) is the jamming margin (jamming signal power relative to desired signal power), and L_{system} are the system implementation losses.

The maximum allowed total system implementation loss is 2 dB.

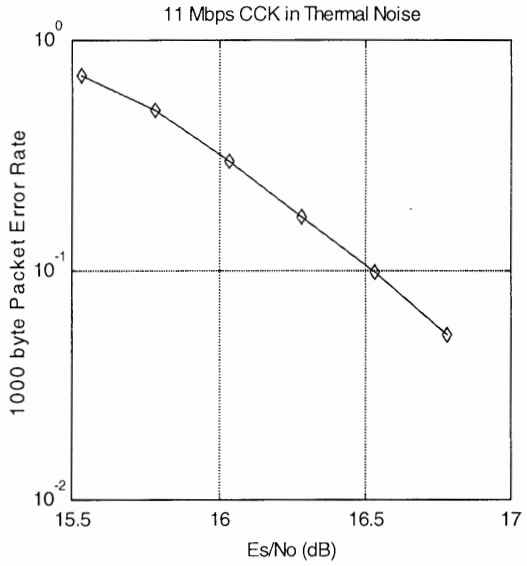
The HFA3861A direct sequence spread spectrum baseband processor uses CCK modulation which is a form of M-ary Orthogonal Keying. The BER performance curve is given by [5]:

" The probability of error for generalized M-ary Orthogonal signaling using coherent demodulation is given by:

$$P_e = 1 - P_{c1} = 1 - \frac{1}{\sqrt{2\pi}} \int_{-\frac{S_{01}}{N_0}}^{\infty} \left[2\left(1 - Q\left\{ z + \sqrt{2\frac{E_b}{\eta}} \right\}\right) \right]^{\frac{M}{2}-1} \exp\left\{ -\frac{z^2}{2} \right\} dz$$

This integral cannot be solved in closed form, and numerical integration must be used. This is done in a MATHCAD environment and is displayed in graphical format.

1.1 1000 byte PER vs. Es/No



The reference PER is specified as 8% . The corresponding Es/No (signal to noise ratio per symbol) is 16.4 dB. The Es/No required to achieve the desired BER with maximum system implementation losses is 18.4 dB. The minimum processing gain is again, 10 dB, therefore:

$$G_p = \left(\frac{E_s}{N_o}\right)_{output} + \left(\frac{J}{S}\right) + L_{system} = 16.4dB + 2.0dB + \left(\frac{J}{S}\right) \geq 10dB$$

$$G_p = 18.4\,dB + \left(\frac{J}{S}\right) \geq 10dB$$

The minimum jammer to signal ratio is as follows:

$$\left(\frac{J}{S}\right) \geq -8.4\,dB$$

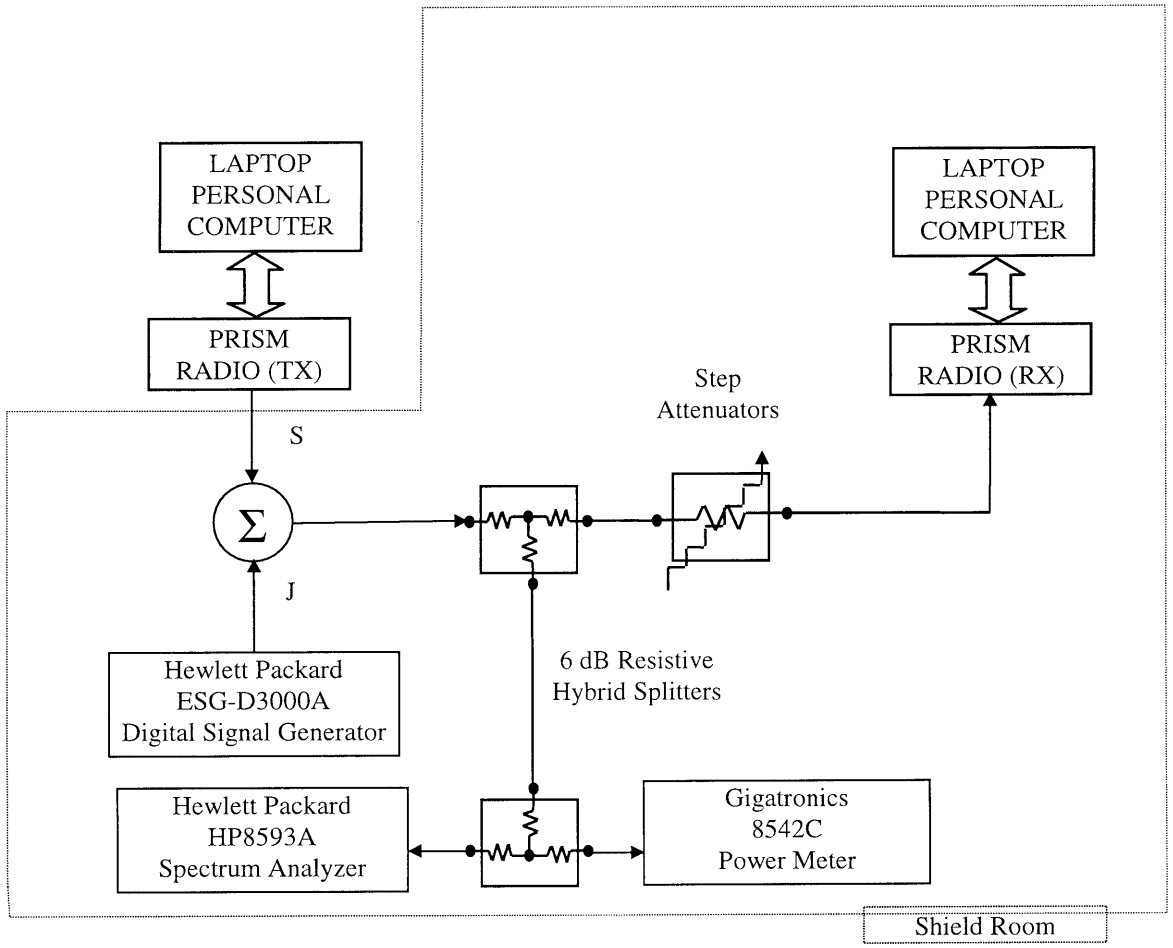
For the case of the HFA3861A, the bit rates are 1, 2, 5.5, and 11 Mbps. The corresponding symbol rates are 1, 1, 1.375, and 1.375 MSps. The chip rate

is always 11 MCps, so the ratio of chip rate to symbol rate is 11:1 for the 1 and 2 Mbps rates and 8:1 for the 5.5 and 11 Mbps rates. Since the symbol rate to bit rate is less than 10 for the higher rates, we supply the theoretical processing gain calculation for these cases where both spread spectrum processing gain and coding gain are utilized. This is reasonable in that they cannot be separated in the demodulation process. If a separable FEC coding scheme were used, we would not be comfortable making this assertion.
As can be seen from the curve of figure 1, the Es/N0 is 16.4 dB at the PER of 8%. This PER can be related to a BER of 1e-5 on 1000 byte packets. With 8 bits per symbol, the Eb/N0 is then 7.4 dB or 9 dB less than the Es/N0. It is well known that the Eb/N0 of BPSK is 9.6 dB for 1e-5 BER, so therefore the coding gain of CCK over BPSK is 2.2 dB. We add this to the processing gain of 9 dB to get 11.2 dB overall processing gain for the CW jammer test.

Taking the calculations above, if the $\left(\frac{J}{S}\right) \geq -8.4\,dB$ then the equipment passes the CW jamming test.

Test Configuration: CW Jamming Margin (15.247) (e)

Basic Test Block Diagram



Test Procedure

Obtain the simplex link shown. Perform all independent instrumentation calibrations prior to this procedure. Set operating power levels using fixed and variable attenuators in system to meet the following objectives:

1. Signal Power at receiver approximately -60 dBm (above thermal sensitivity such that thermal noise does not cause bit errors).

2. Signal Power at power meter between -20 and -30 dBm for optimal linearity.

3. Use spectrum analyzer to monitor test.

4. Ensure that CW Jammer generator RF output is disabled and measure the power at the power meter port using the power meter. This is the relative signal power, S_r.

5. Disable Transmitter, and set CW Jammer generator RF output frequency equal to the carrier frequency and enable generator output. Set reference CW Jammer power level at power meter port 8.4 dB below S_r (minimum J/S, or 10 dB processing gain reference level). Note the power level setting on the generator, this is the reference CW Jammer power setting, J_r.

6. Disable CW Jammer, re-establish link. PER test should be operating essentially error-free.

7. Enable CW Jammer at the reference power level and verify that the PER test indicates a PER of less than 8%.

8. Alternatively, adjust the CW Jammer level to that which causes 8% PER and verify that the S/J is less than 8.4 dB.

9. Repeat step 7 for uniform steps in frequency increments of 50 kHz across the receiver passband with the CW Jammer. In this case the receiver passband is $\pm$8.5 MHz.

The number of points where the PER fails to achieve 8% (is higher than 8%) is determined and if this is above 20% of the total, the test is failed otherwise it is passed.

The margin by which the radio passes the test (for informational purposes) can be determined from the average of the remaining points' PERs scaled on the PER curve above.

The numerical data associated with the following radio channels is tabulated and presented for:

Channel 1: 2412 MHz
Channel 6: 2437 MHz
Channel 11: 2462 MHz

Theoretical BER curves for the IEEE 1 and 2 Mbps modulations

Carl Andren Intersil Corp.

The expected BER versus Eb/N0 curves for these cases may be determined as follows.

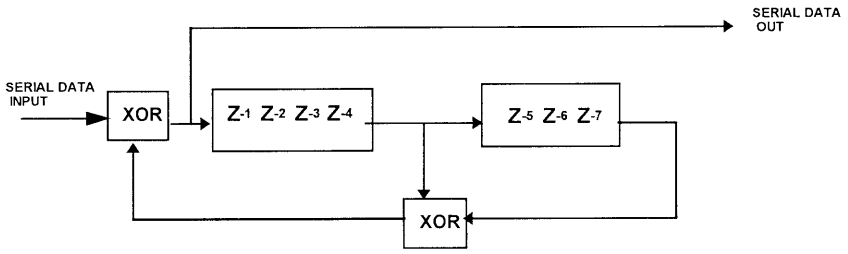
Differential error extension.

The modulation is either DBPSK or DQPSK for 1 and 2 Mbps. With differential coding, there is an error extension factor of 2 which comes from the fact that if one symbol is in error, then the next will be demodulated in error too since it's phase is dependent on the change of phase from symbol to symbol. In DBPSK, this results in a simple factor of two in BER. With QDQPSK, the picture is a little muddied in that a symbol error may cause one or two bit errors since two bits are carried per symbol. The IEEE 802.11 modulations use Grey coding of the phase so that usually only one bit error occurs with a symbol error. Sometimes, two bit errors occur, but this is infrequent at the BER considered. The bit error pattern can be adjacent, separated by one or separated by two for the two error case. This will be shown to be important in descrambling.

De-Scrambling Error Extension

The IEEE 802.11 modulation is scrambled with a self synchronizing scrambler. This scrambler implements a polynomial multiply operation using a feed back shift register configuration as shown in figure 1.

Scrambler Polynomial; $G(z)=Z^{-7}+Z^{-4}+1$



It mixes two taps out of a 7 bit shift register with the data stream. The shift register is fed the received data and any error will propagate through the register for the next 7 clocks. As the error bit passes each of the taps, it will contaminate the output data. Thus each input error can produce several errors on the output. The bit error rate has to be adjusted to account for this effect. For the IEEE 802.11 modulation, taps at registers 4 and 7 are used. In BPSK mode, this produces an error extension of 3. Thus, for an output rate of 10^{-5}, the input rate must be $0.33 * 10^{-6}$ which requires that the Eb/N0 be increased by 0.5 dB. In QPSK mode, the errors can be non adjacent since they are symbol errors and the bit in error can be either the first or second of the dibits. This makes it possible for some errors to cancel in the de-scrambler. Therefore the error extension can be either 2 or 3 in this case.

What we see when running the BER test is that the errors generally occur in groups of 6 with occasional 4s.

The overall effect is to move where we operate on the BER curve. The curve below shows the resulting BER versus Eb/N0 curve. It is well known that a simple BPSK link operates at 9.6 dB for 1e-5 BER. With the error extension effect, we see that at that Eb/N0, the error rate is 6 e-5. Or, conversely, we must operate at 10.3 dB to get 1e-5.

When operating DQPSK at 2 Mbps, the Eb/N0 remains essentially the same, but the Es/N0 goes up by 3 dB. For the purposes of the FCC testing for CW jamming, we add the allowed 2 dB for implementation loss to get a net Es/N0 of 15.3 dB.