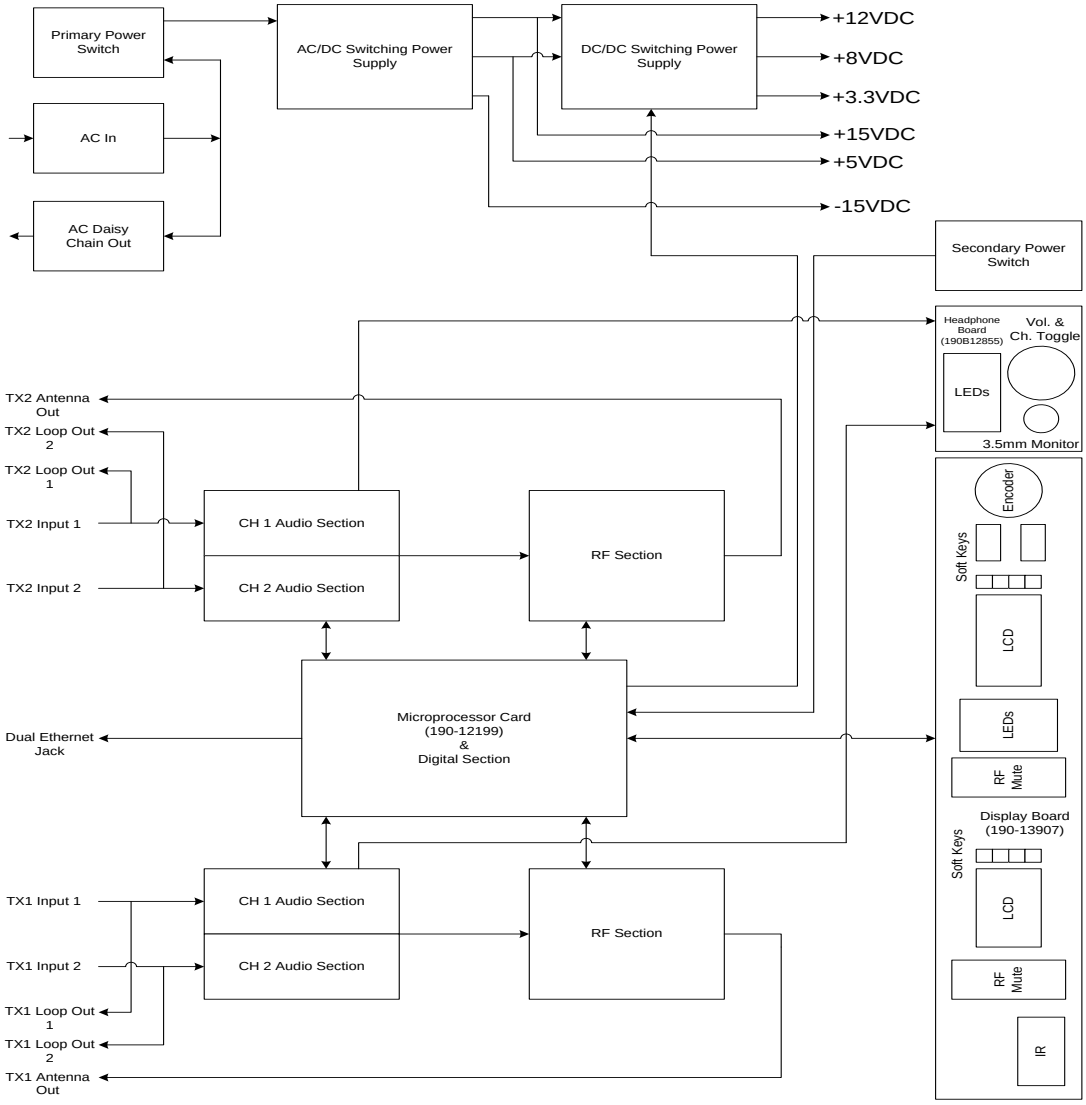
5 Theory of Operation and Design

6.1 Top Level Architecture

P10T System Block Diagram



The P10T incorporates four separate PC boards: the 190-13905 main board, 190-13907 front panel display board, 190-12199 microprocessor board, and 190B12855 headphone board. The P10T is powered from an external AC input. This voltage is then regulated down to +15, -15, and +5 VDC using an internal 3" x 5" AC/DC universal switching power supply. The +15 and +5 VDC voltages are then used to generate +12, +8, +6, +5, and +3.3 VDC for use by the rest of the circuit. Power is distributed to the RF, Audio, and Digital sections of the board. The 2-channel audio section includes gain control, band-pass filtering, and companding. Control of the audio gain is made available to the user through the GUI on the front panel display board. Stereo modulation is achieved through a Walsh encoder and summed with a 19 kHz pilot, which is then fed to the VCO. The signal is then modulated and sent to a power amplifier that can be set to output levels

shown on Table 1.0. Group, channel, and RF power are adjusted via user input or IR transmission. The modulated RF carrier is output via antenna.

6.2 Operating Information

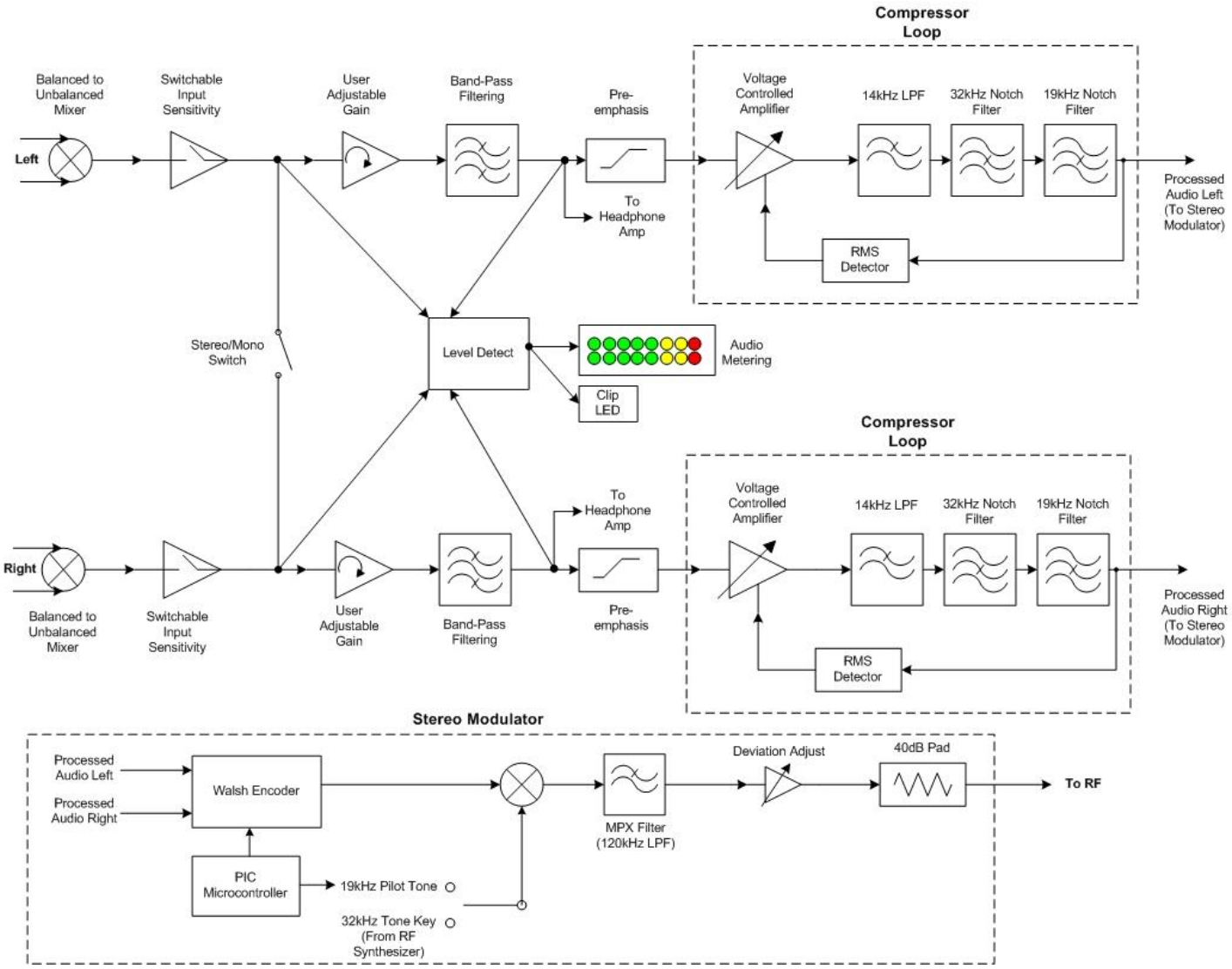
Reference P10T user guide.
http://stellent/stellent/idcplg?IdcService=DOC_INFO_BY_NAME&dDocName=177793&RevisionSelectionMethod=LatestReleased

Note: The P10T is supplied with two half-wave antennas (1 for each channel) as follows:

6.3 Breakdown of Functional Blocks

6.3.1 Audio Section

P10T Audio Section Block Diagram



An audio signal is input to each of the 2 channels through an XLR or ¼" TRS connector (combo jack). Each channel can handle up to +27dBV input signal levels. A loop out is also provided, which feeds the input signals directly out two stacked ¼" TRS connector to allow for daisy chaining of the audio input.

The first stage of the audio front-end converts the balanced L/R input to an unbalanced signal using three 33179 op-amps in an instrumentation amplifier configuration. The second half of the instrumentation amplifier configuration sets the line/aux sensitivity setting (+4dBu/-10dBV) by switching in different feedback impedances around the op-amp to change the overall gain of the stage. This 'sensitivity' adjustment allows the user to alter the gain as appropriate for a

+4dBu line level (higher signal so less gain applied) or a -10dBV aux level (lower signal so more gain applied) signal. This pre-gain audio (i.e. the output of the switchable input sensitivity stage) is sent to input clip-detection circuitry. The detection circuitry is a full-wave rectifier that provides a DC voltage proportional to the audio signal level to an ADC. The microprocessor captures the ADC reading and lights red LEDs on the front-panel if the ADC reading is above a certain threshold, indicating that the input audio signal is clipped and that the user must reduce the audio level they are sending to the transmitter.

The next stage is a user-adjustable gain control, adjustable in 1dB steps, achieved using a standard inverting op-amp stage with a digital potentiometer in the feedback loop. This stage provides an overall gain range of 67dB (-51dB to +16dB). On the LCD, these gain settings are actually shown as ranging from -67dB to 0dB. This stage also acts as a summing amp in 'mono' mode, combining left and right channels. In addition to summing the left and right audio signal, the circuit also pads each channel by 3dB to account for the level increase that would result by summing two relatively equal signals (as typical for stereo programs).

The signal is then sent through a 35 Hz 3rd order Sallen-Key high-pass filter (HPF). Next are three cascaded filters – the first two are 15 kHz 3rd order Sallen-Key low pass filters (LPF) followed by a 19 kHz 1-pole Fliege notch filter. The low- and high-pass filters reduce the amount of out of band noise that reaches the compressor, while the 19kHz notch filter eliminates any of the 19kHz pilot tone that may bleed into the audio or compressor stage. In addition to being sent to the compressor circuitry, this post-gain filtered audio signal is sent directly to an ADC which captures the full audio waveform. The microprocessor uses this data for audio metering on the front panel display board. The audio signal is also routed to the external headphone amplifier board through the headphone amplifier connector located on the main board. This headphone amplifier allows the user to monitor the pre-companded audio signal at the transmitter, allowing them to hear what will be heard at the output of the receiver.

Next is a high-frequency pre-emphasis network, which boosts audio frequencies above 1 kHz to improve noise performance of the overall wireless system. The pre-emphasis network uses a 2% film capacitor to keep variability and distortion at a minimum.

At this point, the signal enters the voltage-controlled amplifier (VCA) section of the THAT 4320 chip. The VCA varies the gain applied to the signal based on the voltage amplitude at its control port. Once the signal exits the VCA, it enters another cascade of filters – first a 14 kHz 2nd order Sallen-Key LPF, then a 32 kHz notch filter and two 19 kHz notch filters to minimize interference with out-of-band noise, pilot tone, and tone key. The compressor section is based on the design first used in ULX wireless, except that this design uses a single THAT 4320 IC for each channel to perform all compressing functionality. The input to the RMS detector is trimmed using a digital potentiometer to set the appropriate threshold such that the knee of the compressor aligns with the knee of the P10R expander. This threshold is set at the IC's internal reference voltage to minimize the effects of the 4320's temperature coefficient. The stage following the RMS detector sets the expansion ratio and provides a "soft-knee" for the compressor. The compressor uses a feedback topology where the compression ratio is defined as dBout = (1+G)dBin. In this case, G = 4 so the compression ratio is 1:(1+4) = 1:5. A soft-knee is created using a diode-connected BJT following the feedback gain stage. The exponential turn-on characteristic of the diode provides a slower change at the control pin of the VCA which translates to a soft transition between no compression and full compression. The Vbe temperature drift of the soft-knee diode is compensated for by using a dual BJT package, with the second transistor in the package being used to subtract the Vbe drop from the output. Since these transistors are within the same package, they are at the same temperature and have a similar temperature coefficient, which provides accurate compensation.

The required amount of fixed gain is derived, and trimmed, from the 4320's internal PTAT (Proportional To Absolute Temperature) reference voltage. The PTAT voltage is nominally VREF–72mV DC at room temperature and has the same temperature coefficient as the RMS

detector and VCA; this provides temperature compensation for fixed gain. +20dB of fixed gain is derived directly from the PTAT voltage source by summing in a scaled version of this voltage to the VCA gain control pin. An additional variable amount of fixed gain (0dB to +24dB) is created by scaling the PTAT voltage source using a digital potentiometer set up as a voltage divider. This variable gain is used for tuning the fixed gain of the compressor to account for part tolerances in the fixed gain circuitry. The scaled voltage is buffered and then also summed in to the VCA gain control pin. The fixed gain controls the VCA unless it is attenuated by the compressor or limiter.

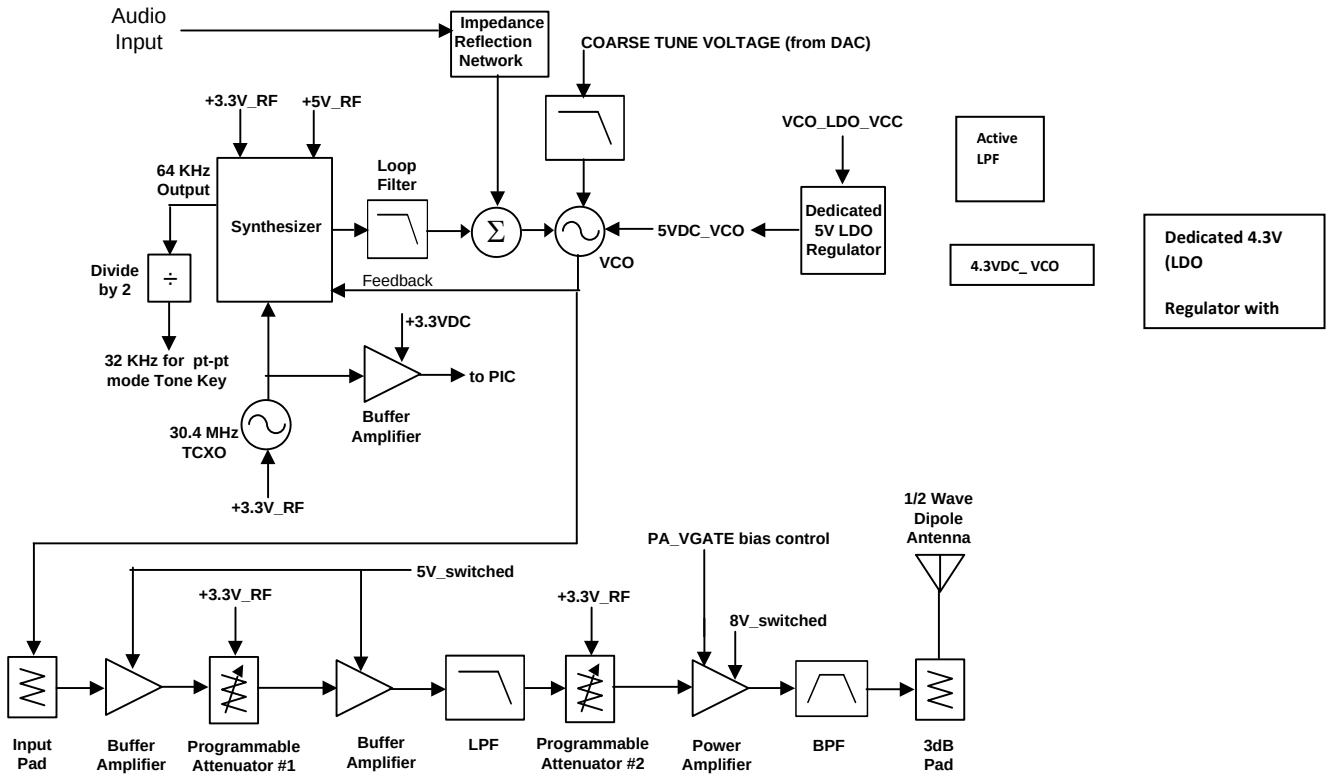
A PIC microcontroller is used to perform Walsh stereo encoding in order to combine the left and right audio signals for transmission. The microcontroller also uses Walsh functions to generate the 19kHz pilot tone required for stereo transmission. The pilot tone (or optional 32kHz tonekey) are summed with the encoded audio to form the composite MPX signal. The 32kHz tonekey is generated from the RF synthesizer. One output of the synthesizer divides down its reference clock to generate pulses at a frequency of 64kHz. These pulses are then sent to a D flip-flop to generate a square wave at half the frequency. This 32kHz square wave is then sent through a band-pass filter to create a 32kHz sine wave. When the transmitter is set to "point-to-point" mode, this 32kHz tonekey is summed with the audio, allowing the P10T to communicate to a UHF-R or Axient receiver. Finally, an additional mode of operation was included in place of an existing developmental mode. This mode, "tone generator", uses Walsh functions to generate both a 19kHz pilot square wave, and a tone of about 397Hz, while muting any input audio which may be present. At launch, this feature is not enabled, but it has been incorporated to all productions PICs in case we want to add this feature through a software update. There is extensive commentary on the PIC source code, which can be found in Subversion. For more information on Walsh stereo encoding theory, see the white paper entitled "Hybrid Stereo Encoding Methods", written by Ryan Perkofski of Shure Incorporated. It can be found here: http://stellent/stellent/idcplg?IdcService=DOC_INFO_BY_NAME&dDocName=040400&RevisionSelectionMethod=LatestReleased.

Finally, the audio signal is sent through a 120kHz 2nd order Sallen-Key LPF and a digitally controlled gain adjustment, which sets the audio deviation for particular RF channel settings. The gain stage is another inverting op-amp stage with a digital potentiometer in the feedback loop. Note that the LM837 op-amp was chosen for this stage and the previous filtering stage due to its high gain bandwidth product, since we are now dealing with a stereo multiplexed signal which has higher bandwidth (20Hz – 53kHz). The digital pot of the gain stage adjusts the audio gain of the output buffer slightly when the transmitter is tuned to different radio frequencies, in order to compensate for gain variations in the VCO across its bandwidth. Consistent deviation tuning throughout all RF frequencies is therefore maintained.

At this point, the signal enters the RF section of the circuitry.

For more detail, including AC and DC levels throughout the audio path, please see sheets 1-4 and 6-9 of the schematic as well as the layout of the P10T. Note that the two transmitters within the P10T are identical and that all the information discussed above is applicable to both transmitters.

6.4 RF Section



RF Section Block Diagram

SYNTHESIZER and VCO

A TCXO (30.4 MHz) is used to provide the reference frequency to both the synthesizer and the PIC. An external TCXO was used because the 2nd channel of the synthesizer is not rated to start up above 16 MHz with its internal oscillator. Running the reference oscillator at 30.4 MHz moves the oscillator spurs out of our operating band. Using the TCXO to also drives the PIC for tone key generation (& point-to-point operation) eliminates manual adjustment of a tuning (trimer capacitor) and is more temperature stable than on previous crystal oscillator designs employed on older PSM transmitters. The TCXO frequency tolerance (& thus RF carrier frequency tolerance) is +/- 2.5ppm. In order to interface with the PIC correctly, a buffer amplifier is employed and D.C. offsets are applied to both the input and output of the buffer amplifier. Additionally, the PIC can run fine using a sine wave as a clock signal (according to the PIC manufacturer), so the output of the buffer amplifier is heavily filtered. This provides a nice sine wave signal to the PIC, and also reduces the harmonic of content to reduce/eliminate troublesome radiated emissions problems.

The new discrete VCO design, based on the PSM900 VCO design, offers improved phase noise performance over the Maruwa VCO modules used on previous PSM transmitters. The control voltage (from the synthesizer) and the audio modulation voltage are combined first, as in previous designs, and then drive a bank of varactor diodes. The circuit also employs lower noise varactor diodes than used previously, and designing to ensure that the peak in the loaded Q response aligns

with the transmission phase zero degree crossing (i.e. at resonance). All this assures the best phase noise performance possible. The charge pump current for the synthesizer IC is programmed to 1.25mA. The VCO gets its DC power from a dedicated, low-noise LDO regulator. The output of this LDO regulator is applied to a “capacitor multiplier” circuit to further filter the DC power before being applied to the VCO. Note that the DC voltage applied to the VCO from the capacitor multiplier circuit is 4.3V nominal. Additionally, there is a separate coarse tune voltage signal (with additional varactors) employed. This helps achieve a tuning bandwidth that is up to 80 MHz, compared to the PSM900 which uses around 36 MHz, while still keeping a low VCO Kv and thus low phase noise performance. The frequency range is divided in to 6 equal bandwidth bins, each of which use a fixed coarse tune voltage over that bins tuning range.

AMPLIFIER BLOCK

The amplifier “strip” is comprised of 3 gain stages to provide gain flexibility to cover band-band gain and VCO output power level variations. In addition, the strip provides superior reverse isolation compared to earlier PSM transmitter designs, to minimize further any audio artifacts that may be generated by variation of the output load impedance (i.e. Antenna VSWR variations from handling).

The output power amplifier device was selected with a higher output level and higher intercept point than in previous designs. Previous transmitter designs (ref. PSM700) have had their amplifiers running in compression. This eliminated the need for tuning (or minimizing tuning) of the output power level, because the power level was relatively consistent from unit to unit. Sometimes the required output level of +20 dBm was difficult to achieve at the antenna connector because of output filter losses (P7T-X1 case in point with ~+19 dBm output). Also, running above the compression point means that the amplifiers are not running in their linear region. This translates to poor IMD performance, including TX-TX IMD generation. In this new design, there is more power (extra design margin) to overcome the output circuit losses, such that the transmitter will be able to easily put out +20 dBm with power to spare. Although we will not need the full 2 Watts of output power that the chosen device will provide, the higher output intercept point that comes with higher output power parts will provide improved IMD performance. Improved IMD performance will also be achieved by the fact that this amplifier strip will be running below the 1dB output power level compression point by 5 to 6 dB or more. Furthermore, TX-TX IMD performance will be noticeably improved because of the increased isolation between transmitters that the output 3dB pad will provide (effectively totaling 6dB of additional isolation). Note that for each dB of pad added, the 3rd order TX-TX IMD products will be reduced by 6 dB. This means an 18dB reduction in IMD levels will be achieved when a 3 dB pad is used on the output of each transmitter. No competitive PSM products employ this technique yet to my knowledge. The down side of this design is that the power amplifier will be running at higher temperatures, and extra precautions are required to provide adequate protection from heat through a generous via hole pattern design, and heat sinking directly to the transmitter chassis which gives an operating temperature margin of around 30 degrees.

The programmable gate bias circuit is designed to cause the PA to be in pinch off mode when power is first applied. This is a function of the programming code; if the code is incorrect, the PA will draw excess current and be destroyed. A DAC on the main PCB is then programmed in the test fixture, to set the idle current of the PA between 250 to 260 mA.

The excess gain and output power margin provided by using 3 amplifiers, along with the digitally programmable attenuators will ensure that +20dBm (+/- ~ 0.5 dB) can be met across the entire frequency band, for ALL frequency bands while allowing for variations in VCO output power over frequency and operating bands, as well as different VCO design options. Additionally, these attenuators can be set to provide the optimum gain for each stage that optimizes the output intercept point for each stage, thus achieving the best output intercept point for the entire transmitter for best IMD performance while still keeping the output power level below the 1dB compression point. There is also a 6 dB pad on the output of the VCO to help minimize reverse isolation from the antenna. This pad can be reduced in value, if necessary, to provide more margin in achievable RF output power at the antenna.

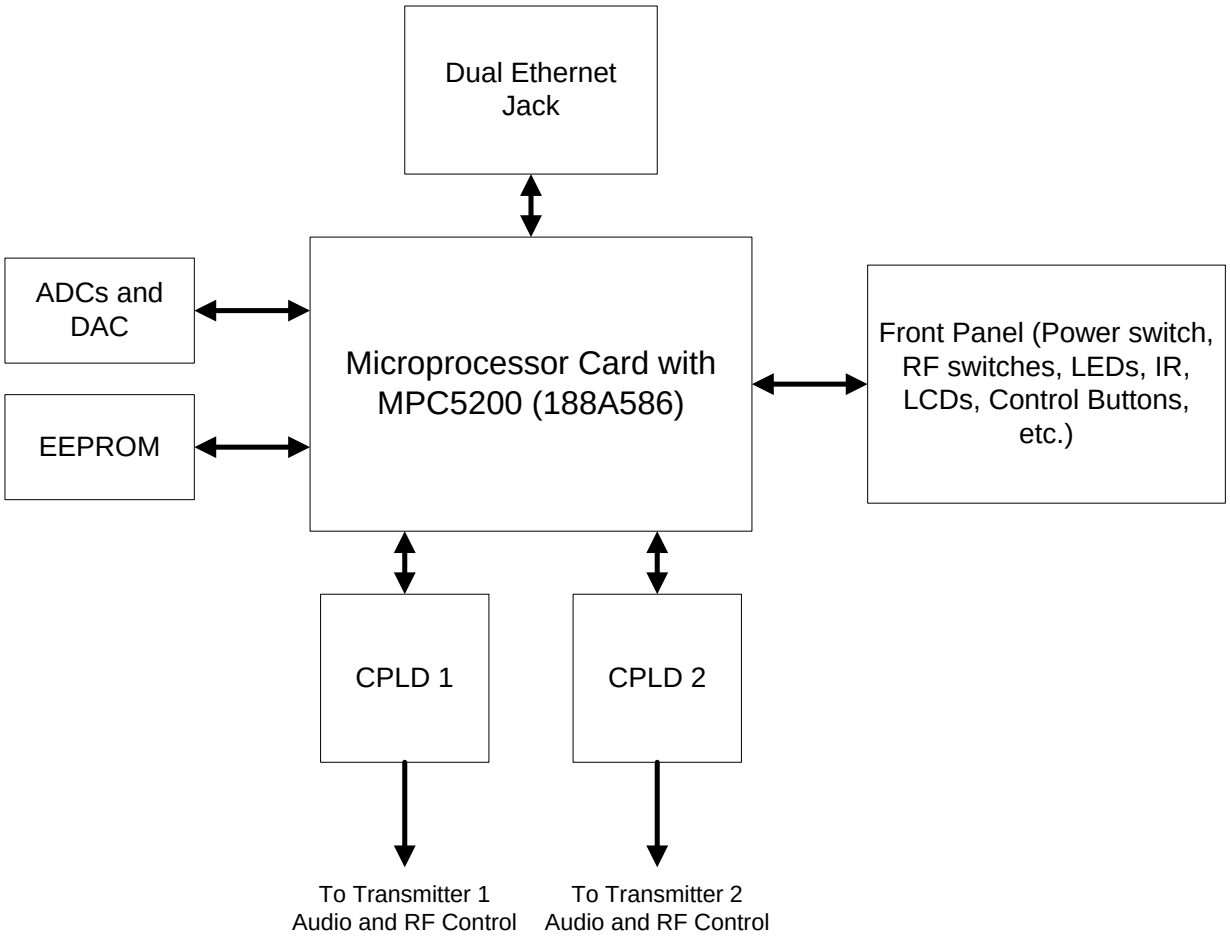
In addition, the programmable attenuators will provide the capability to set the output power to the required levels, as shown in Table 1.0. Each frequency band is divided in to 12 sub bands (bins), and ATE calibration is performed at the center frequency of each bin via Programmable Attenuator #1. The variation in power output across each bin's frequency range, and thus across the entire frequency range, is typically less than 0.5 dB. Programmable Attenuator #2 is used to set the nominal RF output power of 100mW, 50mW, etc. When the transmitter board is first powered up in the ATE fixture, the transmitter will be set to 100mW output power. Since it will take several minutes for the transmitter board to be checked out prior to the RF output power being calibrated, this will allow for the PA to warm up and the power output to stabilize prior to calibration. The actual calibration will occur with the RF output power set to 100mW, and power output will then be verified over frequency and at the higher power levels after calibration is complete. Note that the two buffer amplifiers roll off with increasing frequency. The gain structure was set up to allow for the minimum gain needed at the highest frequency with some margin, as well as to provide enough attenuation to keep the power amplifier well below its 1 dB compression point at the lowest frequency.

A band pass filter was chosen for the output filter instead of a low pass filter to help with ESD protection. The majority of energy present in an ESD event is around 300 MHz or lower, and this will offer additional protection to the PA. Transient Surge Protector Devices will also be installed at the antenna connector, and directly at the output of the PA stage. The band pass filter will also reduce the output harmonic level as required for emissions. The low pass filter earlier in the transmitter strip helps with harmonic rejection as well, and also helps keep the overall broadband noise power going into the PA minimized. The transmitter output impedance is 50 ohms nominal, intended to drive load (antenna) impedances of 50 ohms. The dipole antennas used/supplied with this transmitter have a 50 ohm load impedance.

The mute control powers down the 2 buffer amplifiers and PA stage (switched 5V & 8V DC) during TX power up and also during changes in frequency. The transmitter modulation type is F6E for analog Stereo FM. The Power Amplifier FET is manufactured by Watkins Johnson; WJ part number is FP31QF-F. The worst case current drawn for the PA is 260mA at room temperature.

6.5 Digital Section

P10T Digital Section Block Diagram



The heart of the P10T digital section is the microprocessor card (190-12199) which was originally developed for the Axient project. This card contains an MPC5200 as the main processor that runs off a 67MHz clock, and the entire card is powered off 3.3VDC provided by the P10T main board. The microprocessor card itself contains all the circuitry necessary for Ethernet connectivity. The only Ethernet circuitry on the P10T main board contains TVS diodes for ESD protection and a transformer.

The majority of the microprocessor communication to the P10T main board is done through two CPLDs that are located on the main board. The microprocessor sees the two CPLDs as memory locations and uses a memory bus to communicate information to and from the main board. To send data to the main board, the microprocessor card will write data to the “memory” locations that correspond to the CPLDs. The CPLDs receive this data and trigger the appropriate GPIO and other control signals. Similarly, to receive data from the main board, the microprocessor card will read data from the “memory” locations that correspond to the CPLDs while the CPLDs present information about the status of GPIOs and other signals onto the memory data bus.

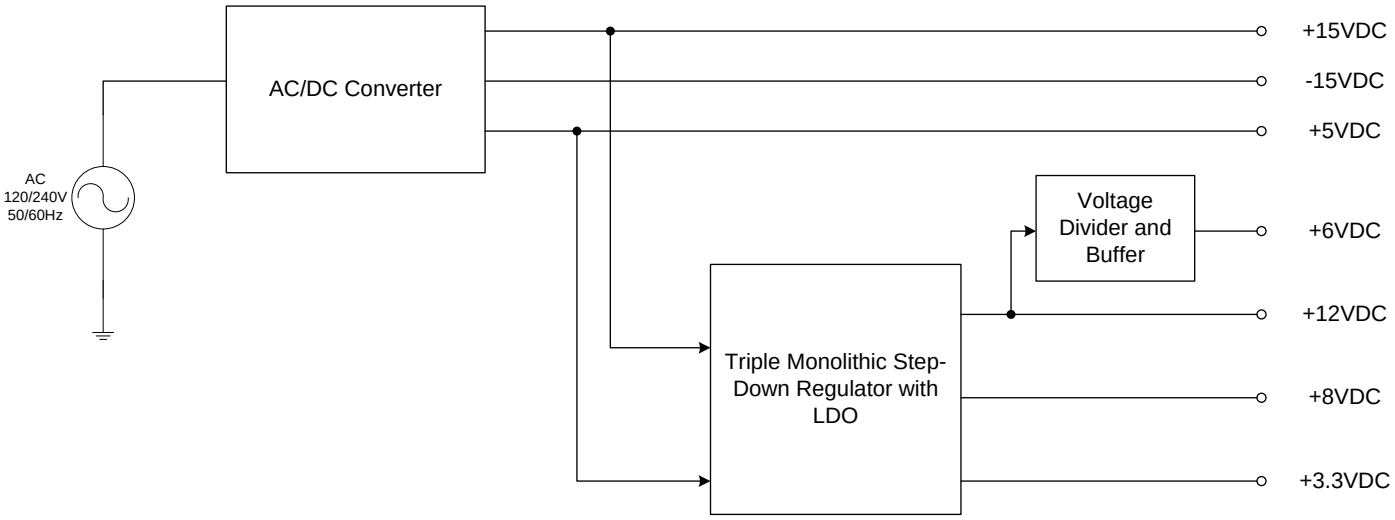
An external EEPROM located on the P10T main board is used as non-volatile memory to store the tuning values of the P10T. It communicates to the microprocessor card through a standard SPI interface which is buffered using the CPLDs.

Three ADCs and one DAC are also located on the P10T main board. Two of the ADCs are used to capture a full bandwidth audio signal from both audio channels of each transmitter. This information is then used for audio metering on the front panel display board. These two ADCs communicate configuration data with the microprocessor card through a standard SPI interface which is buffered using the CPLDs. The ADCs also communicate with the microprocessor card through I^2S. This communication line is used to transfer the actual digital audio data from the ADCs to the microprocessor card. These ADCs are powered off of a local +5VDC LDO to reduce noise on the power supply lines that could translate into noise in the digital audio signal. The other ADC is used to capture the audio clip data, which is a DC voltage corresponding to the audio signal level created by a full-wave rectifier in the audio circuitry. This ADC also captures information about the temperature at different locations on the main board. This is done using thermistors set up as voltage dividers that provide a DC voltage to the ADC that will vary with temperature, allowing us to determine the temperature at the locations on the board near the thermistors. This ADC communicates to the microprocessor card using a standard SPI interface which is buffered using the CPLDs. Finally, the DAC is used for RF tuning purposes. Two of the DAC outputs are used to provide a DC voltage to the RF VCOs for course tuning. Two of the other outputs are used to provide a DC voltage to the RF PA FET, setting up the correct bias voltage on the gate of the FET in order to tune the current through the drain. The DAC communicates to the microprocessor card using a standard SPI interface which is buffered using the CPLDs.

The front panel is a separate PCB (190-13907) that has its own local microprocessor IC: the ATXMEGA128A, which runs off of an external 7.37MHz crystal oscillator. This local processor communicates to the main processor through a two-wire UART interface. Through this communication interface, the main processor provides the local processor with all the information necessary to light LEDs, display information on the LCDs, and other various functions. The local processor can also use this interface to communicate back to the main processor information about the status of the buttons, rotary encoder, and other user interface features.

6.7 Power Supply Section

P10T Power Supply Section Block Diagram



The P10T contains a completely internal power supply, allowing it to be powered directly from an external AC 120/240V, 50/60Hz source. The AC signal is sent to the internal power supply, which is 95B8995. This supply generates a +15V, -15V, and +5V DC voltage from the AC signal. The +15VDC and +5VDC voltages are then sent to a triple step-down regulator. The +15VDC supply is used to generate +12VDC and +8VDC supplies. The +5V supply is used to generate a +3.3VDC supply. The +12VDC supply is also divided and buffered to generate a +6VDC bias voltage.

The +15VDC and -15VDC supplies are used to power the input stages of the audio section to allow for a greater signal swing at the input before distortion occurs. They are also used to power the external headphone amplifier board. The +5VDC supply powers most of the RF circuitry, as well as the DAC and some circuitry on the front panel. The +12VDC supply is used to power all of the audio circuitry with the +6VDC bias voltage being used as a half-supply bias for the audio. The +8VDC supply is used to power more of the RF circuitry. The +3.3VDC supply is used to power the microprocessor card as well as all the digital circuitry on the main board. It is also used to power some additional RF circuitry.