BLX2 Circuit Description:

Audio

BLX2 has a fixed head design, so the mic cartridge is not user-removable. The cartridge wires are soldered into holes (CON1 & CON2) on the PCB. It is important to solder these wires in the proper polarity, as follows:

Cartridge	CON1 (+)	CON2 (-)
PG58	wire with NO red paint	wire with red paint
SM58	yellow	green
Beta58	yellow	green

The front-end gain stage (IC150-4) permits two user gain settings (standard & -10dB) via Q160, Q161, Q162, and associated components. Capacitor C140 couples the signal into a pre-emphasis network formed by R140, R141, and C141.

After the audio preamp, the audio signal is ready for processing by the audio level-dependent processing section, using Shure's patented ARC™ technique. The main elements in this section are the VCA (IC100-1) and the RMS Detector (IC100-2). The VCA, or Voltage Controlled Amplifier, is a DC-controlled amplifier. Following the VCA, the signal enters a 2-pole 17 kHz low-pass filter stage (IC150-1) that protects the RMS detector from energy above the audio band. Next, the signal is coupled to the RMS detector, which converts the decibel-level of the RMS value to a proportional DC voltage. A 1dB increase at the input to the detector produces a 6mV increase at its output. The detector output is fed to the compression threshold stage (IC120-4). This stage provides the transition from uncompressed to compressed signal. At low levels, the audio is uncompressed because diode D190 is turned off. As the AC level increases, the output of IC120-4 decreases enough to turn the diode on. As D190 conducts, the compression ratio changes from 1:1 to approximately 5:1. Once D190 is turned fully on, the audio compression ratio remains fixed at 5:1. An additional diode in the bias network (D162) provides temperature compensation for changes in the V_γ, or "cut-in" voltage of D190. After the compression threshold stage, the DC control signal is then sent to the VCA control voltage input (EC-) through buffer amp IC120-2. The VCA uses the difference between EC- & EC+ (connected to VREF) to determine the gain. Fixed gain, applied below the compression threshold, is set by the DC gain of IC120-2.

The audio muting function was disabled for UI simplicity, and it was later discovered that this circuitry (C205, Q205, etc.) adds additional distortion, so the components were DNP'ed. After this section, audio is then combined with tone key in the summing amp (IC150-2), which uses trim pot TR200 for tuning of audio deviation. The combined audio & tone key signal is then passed to the RF section for transmission. The tone key signal is used in the receiver to provide audio output only when the tone key signal is present with the transmitted signal; therefore, if the tone key or the transmitter is turned off, the receiver will be muted. Tone key squelch helps eliminate receiver noise associated with loss of the carrier, which usually sounds like a "pop". A local crystal oscillator made up of crystal Y347, transistors Q186-1, Q186-2, Q185-1, Q185-2 and surrounding passive biasing components generates the tone key signal. Q185-2 serves as a tone key mute controlled by the microcontroller. During low battery condition, tone key level is increased (TK_LO_BAT signal to R192) for indication on the ½-rack receiver (BLX4R).

The complete signal is then coupled into the RF section through R504 and a minimum pulse distortion attenuation pad made up of R510, R511, R513, R514, C514, C515, C516, C531, C532, C533.

Power Section

Two AA batteries supply power to the transmitter through FET Q410, which provides electrical reverse battery protection. Next, power enters switching regulator IC400, which supplies regulated 5V power. To turn on the transmitter, SW313 shorts the base of Q480 to ground, enabling the regulator and powering up the unit. The microcontroller keeps Q480 disabled until shutdown.

Power is controlled by SW313 and a "shutdown" signal from the microcontroller, which can be initiated manually by the user (by holding down SW313) or automatically by the system (after MCU shut-down procedure, or when the battery is too weak for proper operation). At this time, the MCU enables Q480 and shuts down the converter. When SW313 is in the off position, Q480 and its bias circuitry draw less than 30 µA, so the effect on battery life is negligible. In this condition, the regulator and MCU are disabled.

RF Section

The BLX2 uses a phased locked loop (PLL) system with direct carrier frequency modulation. Processed audio enters the voltage-controlled oscillator (VCO) through a passive "reflection" network before being applied to the varactor diode (D500) through RF choke L503. The VCO and PLL circuitry is shielded to prevent external RF fields from affecting its operation, and to help control radiated emissions of its harmonic frequencies. Power for the VCO and PLL circuitry is supplied by the main 5 volt boost converter and 3.3V regulator. The power and signal lines in the VCO area are heavily decoupled and bypassed to remove noise.

The VCO has a maximum tuning bandwidth of 24 MHz (band dependent), with a tuning voltage range of approximately 1 to 4 volts. The VCO employs separate stages for the oscillator (Q502) and buffer (Q501) to minimize phase noise and load pulling. The VCO output is isolated by capacitive and resistive dividers, before being applied to the frequency control pin of the PLL synthesizer (IC501) through C538. The synthesizer's internal circuitry divides the RF signal down as necessary to achieve tuning resolution steps of 25 kHz. The synthesizer circuit contains a quartz-controlled reference oscillator operating from a 16 MHz reference crystal (Y500) that is adjusted by a variable capacitor CV501. New board group 190-23744 uses a 30.4MHz TCXO as the reference to the new PLL synthesizer, and does not have a variable capacitor. The TCXO does not need adjusting. The transmitter output frequency is user selectable in groups of up to 12 compatible channels (band dependent) within each of the 18 available bands. Frequency selection is made via MCU (microcontroller) IC300. The output of the synthesizer is a series of pulses that are integrated by a passive loop filter consisting of C532, R514, C533, R513, and C531 to produce the control voltage signal.

The VCO output is coupled to the RF buffer stage (Q600) by a resistive isolation network consisting of R503, R505, R520, and R602 through a pi network resistive pad. The isolation network provides additional isolation between the RF buffer stage, the VCO and the PLL feedback loop to lessen the effect of VCO impedance pulling. R600 and R603 provide base bias for Q600, while R605 sets its operating current. RF choke L600 provides power and decoupling for the stage, in conjunction with C600, C601, C606, and C652. The collector of Q600 feeds the power amplifier stage via an impedance matching network consisting of L602, C611, and C618 through a second pi network resistive pad.

The bias voltage for the RF power amplifier (Q601) is supplied by R601 and R604. Its operating current is controlled via emitter resistor R606. RF choke L601 provides power and decoupling for the stage, in conjunction with C603, C607, C608, and C651. L603, C612, and L604 provide the output impedance matching into the low pass filter, which consists of L605, L606, C615, C616, and C617. The low pass filter output couples to the antenna (batteries) via L607 or R607 (band dependent).

The transmitter is capable of delivering up to +12.0 dBm to the antenna. During transmitter power-up and frequency selection, the RF output is muted by bringing the base of Q631 low, which removes bias from Q630 and shuts down power to the RF stages. The RF output is also muted during the transmitter power-down sequence. This is done so that the carrier signal will not interfere with other transmissions when the VCO becomes unlocked.

Digital Section

The heart of the digital section is the MC9S08GT16A 8-bit microcontroller (IC300) from Freescale. This MCU has 16KB of internal Flash memory for program storage, up to 39 general purpose I/O pins, and integrated ADCs for measuring voltage levels.