Lectrosonics Standard Test & Alignment Procedure

Part number(s): M4T **Hardware version(s):** 17427x (Baseband board) & 17396b (Radio board) **Firmware version(s):** 0.0
Common name(s): 4 channel, digital transmitter **Author(s):** Derek Jasnoch, Rodney Wildhagen, & Cruz Garcia **Test procedure version:** 01.00
Date: 29 Sept 2010

Initial setup:

- Radio board & LCD display connected to baseband board
- All audio signal measurements made with a 22Hz HPF and a 22kHz LPF to keep 60kHz pollution out of the measurements.
- All voltage measurements referenced to circuit common
- All DUT (transmitter) audio signal inputs and test receiver audio signal outputs are differential
- Logic Probe equipped with Pulse Memory (Meterman LP25A or equivalent) used in Bit error test
- All Reciever audio signal measurements taken with 300Ω load resistors from XLR pin 2 to XLR pin 1 and from XLR pin 3 to XLR pin 1.
- "Factory" mode contains an expanded menu for product testing. To enter factory mode, push and hold front panel MENU/SEL button while powering up DUT
- This test requires a test receiver wired for access to the bit error signal (baseband board TP24)
- It is noteworthy that the USB port is useful only for upgrading firmware.
- Firmware is updated using the LecNet2 D4 update Utility
- AES Input measured thu a AJA Video Systems, ADA4 4-Channel Bi-directional Audio A/D and D/A Converter, Dip switch Setting are 1,0,3,0.

Step	***Measurement name*** **& description**		**Measurement result**	**(Typ)**
Test segment #10 of 40				
10	*Current draw measurement & Program FPGA IC*			
Note	This need only be performed at the factory the first time it is powered up, when FPGA IC is replaced, or when a firmware update is desired and confirmed to be appropriate.			
	15VDC, 1A current limit, at baseband board VCC (VCC — is circuit common)			
10.10	Measure current draw		30 to 800 mA	
Note	Expected current draw values are:	FPGA not programmed		(?)
		FPGA programmed		(410)
Note	Driver is required. It is packaged in with the LecNet2 software disc *du jour*			
Note	Command line utility is located at S:/DTBACK/UTIL/D4UP			
10.20	**Connect PC to baseband board J3 (rear panel mini USB port)**			
10.30	Use prescribed GUI tool to program FPGA S:\DTBACK\UTIL\D4UP			
10.40	**Remove USB, PC to DUT connection**			
20	*Current draw measurement post programming*			
Note	This need only be performed if the FPGA programing status has changed since test step #20			
Prerequisite(s)	15VDC, 1A current limit, in at baseband board VCC (VCC — is circuit common)			
	FPGA IC programmed			
20.10	Verify LCD display backlight appears to be appropriate		back light on	
20.20	Measure current draw		30 to 800 mA	(410)
Note	The goal here is only to be sure the DUT is on and is not burning up with fever, a tighter tolerance current measurement will be made later.			
Test segment #20 of 40				
30	*Supply rail, reference voltage, and reference oscillator (infrastructure) measurements*			
Prerequisite(s)	15VDC, 1A current limit in at baseband board VCC (VCC — is circuit common)			
	FPGA IC programmed			
30.10.10	Measure DC voltage at baseband board:	TP21	+15.25 to +16.75 VDC	(+16.0)
30.10.20		TP26	-15.75 to -14.25 VDC	(-15.0)
30.10.30		TP20	+3.135 to +3.465 VDC	(+3.0)

30.10.40		TP7 (+1.2V)	+1.14 to +1.26 VDC	(+1.2)
30.10.50		TP23 (+5V)	+4.75 to +5.25 VDC	(+5.0)
	LCD contrast (no adustment for this)	TP 19	+3.75 to +4.25 VDC	(4.0)
30.20.10	Measure DC voltage at radio board:	TP11 (+5V)	+4.75 to +5.25 VDC	(+5.0)
30.20.20		TP12 (VCC_RF)	+2.755 to +3.045 VDC	(+2.9)
30.20.30		TP13 (VCC_OSC)	+3.135 to +3.465 VDC	(+3.3)
30.30.10	Measure reference oscillator signal (36.864MHZ_TO_FPGA) at radio board J1-11 with 10:1 oscilloscope probe BW ≥ 100MHz using RF spectrum analyzer with 50Ω input Z. TP14	Frequency (MHz)	36.859 to 36.871	(36.864)
30.30.20		Amplitude	-18 to +2 dBm	(-15)
30.30.30	Verify first 5 harmonics are at least 3dB below the fundamental	Spectral purity		(-11)

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40 *Transmitter Set up*

40.10 **Transmitter set up: Lock Setup = Unlocked, 2/4 Chans. = 4 Channels, AES3 modes = 1 & 2 Analog, 3 & 4 Analog, Audio Trim = +00 (all 4 channels)**

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50 *Carrier signal measurements*

Prerequisite(s) FPGA IC programmed

Note There is a function called "Mod.Level" in the expanded "Factory Mode" menu that permits carrier signal level (power) to be adjustment as necessary.

50.10 **Press front pannel Menu/Sel button while applying 15VDC, 1A current limit, in at baseband board VCC to enter into factory mode. (VCC — is circuit common)**

50.20.10	Measure carrier signal power for RF channels 1 thu 4 at antenna port	RF channel 1 to 4	21 to 23 dBm	(+22)
50.30	**Transmitter set up: Test Mode "Null"**			
50.40.10	Measure carrier signal frequency at antenna port	RF channel 4	923.899 to 923.909 MHz	(923.904)
50.40.20		RF channel 3	916.987 to 916.997 MHz	(916.992)
50.40.30		RF channel 2	912.379 to 912.389 MHz	(912.384)
50.40.40		RF channel 1	907.771 to 907.781 MHz	(907.776)

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60 *Baseband signal measurements*

Prerequisite(s) 15VDC, 1A current limit, in at baseband board VCC (VCC — is circuit common)

FPGA IC programmed

Transmitter set up: Test Mode "audio"

60.10.10	Measure and note signal amplitude at radio board:	TP10 (I+)	480 to 740 Vp-p	(575)
60.10.20		TP7 (I-)	480 to 740 Vp-p	(575)
60.10.30		TP4 (Q+)	480 to 740 Vp-p	(575)
60.10.40		TP6 (Q-)	480 to 740 Vp-p	(575)

60.20 Verify that baseband signals measured in test sub-step #60.10 are within 20mV of each other

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Test segment #30 of 40

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70 *Bit error test*

Prerequisite(s) 15VDC, 1A current limit, in at baseband board VCC (VCC — is circuit common)

FPGA IC programmed

70.10 **Receiver set up: Lock Setup = Unlocked, 2/4 Chans. = 4 Channels, AES3 modes = 1 & 2 Analog, 3 & 4 Analog, Audio Lev. = +8 (all 4 channels)**

70.20.10 Connect two Antenna to the Receiver antenna ports. Lecto part # 21422

70.20.30	Connect the output of the transmitter to the test equipment testing RF Signal Power and Frequency, keeping cable connection at least 1' away from receiver antennas.			
70.30	**Transmitter set up: Test mode "All 0"**			
70.40	Measure for bit errors at receiver baseband board TP24 over a 15 second period using a Meterman LP25A Logic Probe or equivalent with a Pulse memory track activated		0 errors	(0)
80	*Analog Audio performance measurements*			
Note	Audio channel 1 tested using carrier channel 1, 2 with 2, etc.			
Prerequisite(s)	15VDC, 1A current limit, in at baseband board VCC (VCC — is circuit common)			
	FPGA IC programmed			
80.10	**Transmitter set up: Test mode "Audio"**			
80.20	**-3 dBu, 1kHz, low distortion, differential sinusoid in at Channel 1 test transmitter inputs**			
80.30.10	Measure audio signal amplitude at test receiver outputs Ch 1 (differential) with DUT input level (menu) set to:	+00	+0.5 to +2.5 dBu	(+1.5)
80.40	Measure audio signal distortion at receiver outputs		≤ 1.0 % THD+N	(0.8)
80.50	Measure audio signal phase lag at test receiver outputs relative to DUT (transmitter) input signal		-318 to -282° or +42 to +78°	(-250, +100)
Note	Audio signal phase lag may alternatively be measured as a time lag		? to ? µS	(-?)
80.60.10	Measure audio signal frequency response at receiver output referenced to 1kHz	20 Hz	-6.6 to -4.6 dB(r)	(-5.6)
		50 Hz	-1 to +1 dB(r)	(0)
80.60.20		20 kHz	-1.8 to -1.6 dB(r)	(-1.7)
80.60.30		25 kHz	-20.9 to -16.9 dB(r)	(-18.9)
80.70	Measure audio signal microphonics at test receiver output (activate vibrator motor) We'll need to find a convenient and uniform spot to mount the vibrator motor		≤ -89 dBu	(-91)
80.80	Repeatedly tap edge of baseband and radio boards and watch for any signs of excessive microphonic behavior at test receiver outputs		≤ -89 dBu	(-91)
80.90.10	Measure audio signal amplitude at test receiver outputs Ch 1 (differential) with DUT input level (menu) set to:	-20	-19.3 to -17.3 dBu	(-18.3)
80.90.20	Measure audio signal amplitude at test receiver outputs Ch 1 (differential) with DUT input level (menu) set to:	-10	-9.3 to -7.3 dBu	(-8.3)
Note	A frequency domain analysis of the audio signal offers the best opportunity to observe microphonic behavior with the "tap test".			
80.100	Repeat test step #100 for all DUT audio channels			
90	*Headphone output performance measurement*			
Prerequisite(s)	15VDC, 1A current limit, in at baseband board VCC (VCC — is circuit common)			
	FPGA IC programmed			
	DUT audio level set to -10 all input channels, analog (all 4 inputs), display all 4 channels			
	Transmitter set up: Test Mode "Audio"			
90.10	**Receiver set up for Div. mode " Demod Auto" (Cycle power to DUT)**			
Note	Headphone output measured at Tip and Ring with a 32Ω load.			
90.20	**-3 dBu, 1kHz, low distortion, differential sinusoid in at at DUT Chan. 1 input**			
90.30	Press front panel 1 to select Audio channel 4. The headphone Icon should be present next to the channel 1 input audio level indicator.			
90.40	Rotate R125 CCW to minimum, measure and note audio signal Amplitude Tip to ground at baseband Headphone output J5.			
90.50	Rotate R125 CW to Mid, measure audio signal Amplitude Tip to ground reference to aplitude level in step#####.		+72.0 to +78.0 dBu	(+75.0)
90.60	Rotate R125 CW to Maximum, measure audio signal Amplitude Tip to ground reference to aplitude level in step#####.		+79.6 to +83.6 dBu	(+81.6)
90.70	Measure audio signal Amplitude Tip to ground at baseband Headphone output J5.		-0.3 to +1.7 dBu	(+0.7)
90.80	Measure audio signal Distortion Tip to ground at baseband Headphone output J5.		≤ 0.5% THD+N	(0.1)
90.90.10	Measure audio signal frequency response at receiver headphone output Tip to ground referenced to 1kHz	20Hz	-5.25 to -3.25 dB(r)	(-3.1)
90.90.20		50 Hz	-1 to +1 dB(r)	(0.0)
90.90.30		20kHz	-3.2 to -1.2 dB(r)	(-2.3)
90.90.40		25kHz	-19.5 to -17.5 dB(r)	(-18.5)
90.100	Measure audio signal Noise Tip to ground at baseband Headphone output J5.		≤ -82 dBu	(-86)
90.110	Repeat sub-steps #120.70 through #120.100.40 measuring Ring instead of Tip			

Test segment #40 of 40

100	*AES Input performance measurement*			
Prerequisite(s)	15VDC, 1A current limit, in at baseband board VCC (VCC — is circuit common)			
	FPGA IC programmed			
	Transmitter set up: Test Mode "Audio"			
100.10	**Receiver set up for Div. mode " Demod Auto" (Cycle power to DUT)**			
100.20	**-3 dBu, 1kHz, low distortion, differential sinusoid in at ADA4 A/D converter Input C and D.**			
100.30	**ADA4 A/D converter Output C connected to DUT AES Input CH1/CH2**			
100.40.10	Measure audio signal amplitude at test receiver outputs (differential)	CH 1	-17.0 to -15.0dBu	(-16.0)
100.40.20	Measure audio signal distortion at receiver outputs	CH 1	≤ 0.1 % THD+N	(.05)
100.50.30	Measure audio signal amplitude at test receiver outputs (differential)	CH 2	-17.0 to -15.0dBu	(-16.0)
100.50.40	Measure audio signal distortion at receiver outputs	CH 2	≤ 0.1 % THD+N	(.05)
100.60	**ADA4 A/D converter Output C connected to DUT AES Input CH3/CH4**			
100.70	Repeat steps 105.40.10 to 105.50.40 for test receiver ouput CH3 and CH4.			

110	*Current draw measurement & power down test*		
Prerequisite(s)	Baseband board S7 (transmitter power switch) to ON (outboard) position		
	15VDC, 1A current limit, in at baseband board VCC (VCC — is circuit common)		
	FPGA IC programmed		
110.10	Measure current draw	380 to 440 mA	(410)
110.20	**Place baseband board S7 (receiver power switch) to OFF (inboard) position**		
110.30	Remove 15VDC supply	0 to 5 mA	(0)

120	*Install shield cap*
120.10	Place 26014 RF shield cap on top side PCB assembly. Tack solder two opposite corners.

Lectrosonics, Inc.