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SM 100 Operational Description:

Weldon Sanders

Garrett Metal Detectors

Attachments: SM 100 Operational Description

SM 100

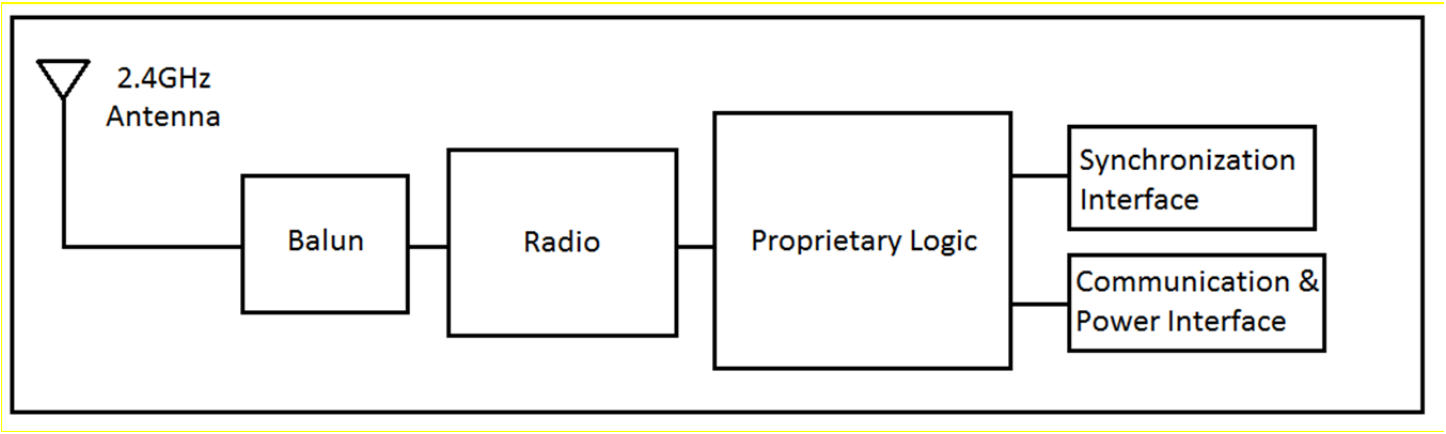

Figure 1: SM 100 Block Diagram

The figure above shows the block diagram for the SM 100. The SM 100 is configured as a MASTER (primary transmitter) or SLAVE (primary receiver) by the host walkthrough metal detector via menu selection. Each radio is capable of service as a transmitter or receiver. A microprocessor runs the proprietary control logic and walkthrough interface (UART). On the transmitter, data is packetized by the processor and sent to the radio to transmit. On the receiver module, received packets are sent from the radio to the processor.

A balun – Anaren BD2425N50200AHF - is used to convert the differential antenna output of the radio to single ended output. The balun also provides matching of the impedances between the radio and the antenna. A 2.4/5 GHz patch antenna – Molex 479501001 - is used.

All of these blocks are common to the transmitter and receiver. The direction of signal flow is from the walkthrough synchronization interface to the antenna on the transmitter and from the antenna to the walkthrough synchronization interface on the receiver.

Block Diagram of Radio

The radio communication of the device uses a Texas Instruments CC2420 chip which is capable of being configured as a transmitter and/or receiver. The receiver features low-IF technology. The received RF signal is amplified by the low noise amplifier (LNA) and down-converted in quadrature (I and Q) to the intermediate frequency (IF). At IF (2 MHz), the complex I/Q signal is filtered and amplified, and then digitized by the ADCs.

The transmitter is based on direct up-conversion. The data is buffered in a 128 byte transmit FIFO (separate from the receive FIFO). The preamble and start of frame delimiter are generated by hardware. Each symbol (4 bits) is spread using the IEEE 802.15.4 spreading sequence to 32 chips and output to the digital-to-analog converters (DACs).

An analog low pass filter passes the signal to the quadrature (I and Q) up-conversion mixers. The RF signal is amplified in the power amplifier (PA) and fed to the antenna.

The frequency synthesizer includes a completely on-chip LC VCO and a 90 degrees phase splitter for generating the I and Q LO signals to the down-conversion mixers in receive mode and up-conversion mixers in transmit mode. The VCO is completely integrated and operates in the frequency range 4800 – 4966MHz. The VCO frequency is divided by two when split in I and Q to generate frequencies in the desired band (2400-2483.5 MHz).

A 16MHz (±20ppm) crystal – e.g. Abracon Corp. ABMM-16.000MHz-B2-T2 - is connected to XOSC16_Q1 and XOSC16_Q2 and provides the reference frequency for the synthesizer.

The CC2420 has an effective RF bit rate of 250kbps. The SM 100 module sends packets of data. Packet transmission rates may range from 200Hz to 265Hz.

The output power for the transmitter is programmable. In this application the output power is fixed at the highest power level of 0dBm.

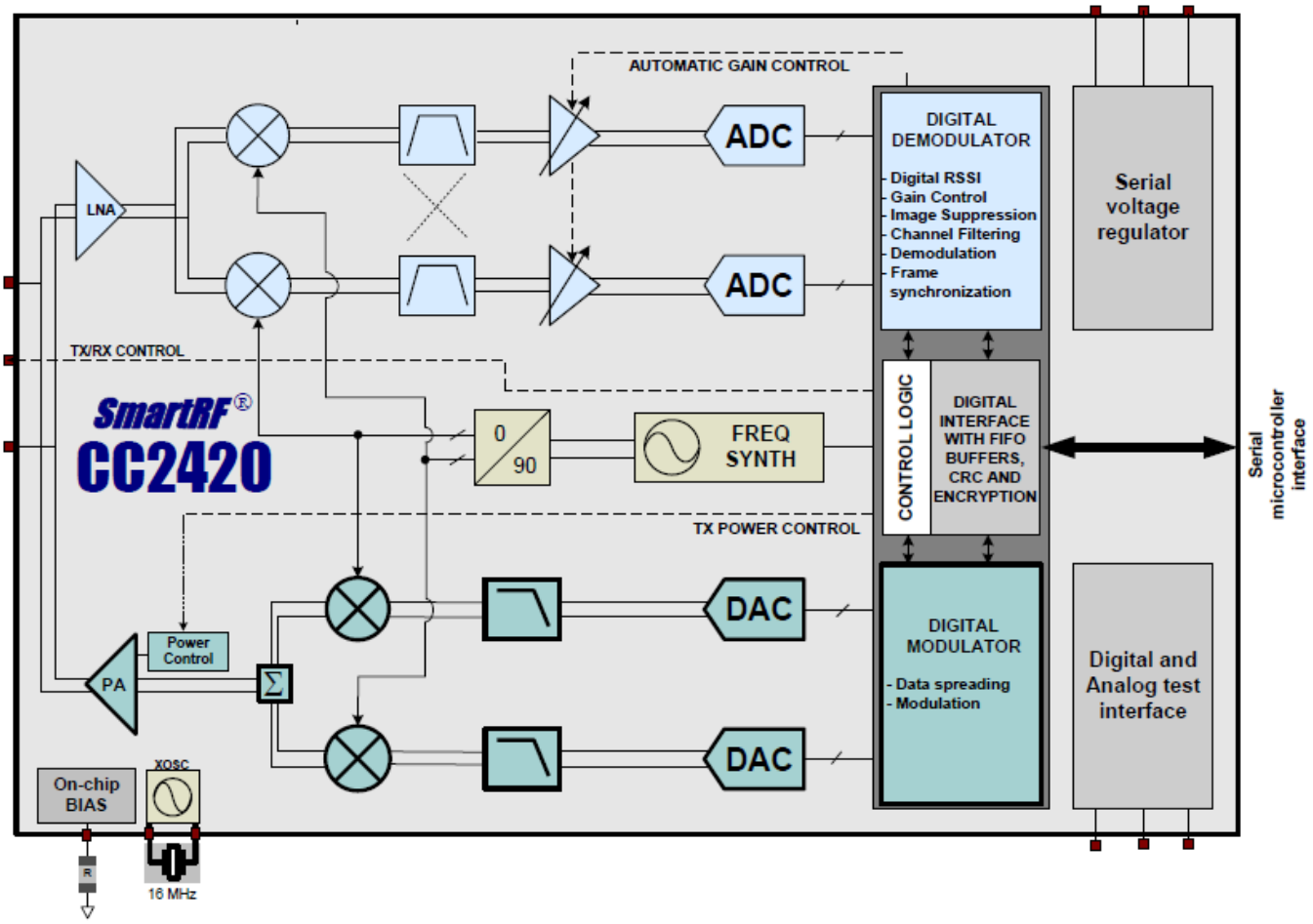

Figure 2: Internal Block Diagram of Radio

The frequency of the radio channel is set by programming the 10 bit frequency word in register FSCTRL. The operating frequency F_C in MHz is given by:

$$F_C = 2048 + FSCTRL \text{ (MHz)}$$

The frequency can be programmed with 1MHz resolution. In receive mode the actual LO frequency is F_C – 2 MHz, since a 2MHz IF is used. Direct conversion is used for transmission, so here the LO frequency equals F_C. The 2 MHz IF is automatically set by CC2420, so the frequency programming is equal for RX and TX. IEEE 802.15.4 specifies 16 channels within the 2.4 GHz band, in 5 MHz steps, numbered 11 through 26.

The RF frequency of channel k is given by [1]:

$$F_C = 2405 + 5\,(k-11) \text{ MHz, } k=11, 12, \ldots 26$$

For operation in channel k, the FSCTRL register should therefore be set to:

$$FSCTRL = 357 + 5\,(k-11)$$

This device allocates channels in the same fashion. The channel value is based on the value of the FREQ setting on the host walkthrough metal detector.

The following table shows FREQ values and their corresponding radio channels.

FREQ value	Radio Channel
2300 - 2262	0x0B
2261 - 2223	0x0C
2222 - 2184	0x0D
2183 - 2145	0x0E
2144 - 2106	0x0F
2105 - 2067	0x10
2066 - 2028	0x11
2027 - 1989	0x12
1988 - 1950	0x13
1949 - 1911	0x14
1910 - 1872	0x15
1871 - 1833	0x16
1832 - 1794	0x17
1793 - 1755	0x18
1754 - 1716	0x19
1715 - 1677	0x1A

Table 1: FREQ to Channel mapping

FREQ values below 1677 are not supported.

The CC2420 uses the 2.4 GHz direct sequence spread spectrum (DSSS) RF modulation format defined in IEEE 802.15.4.

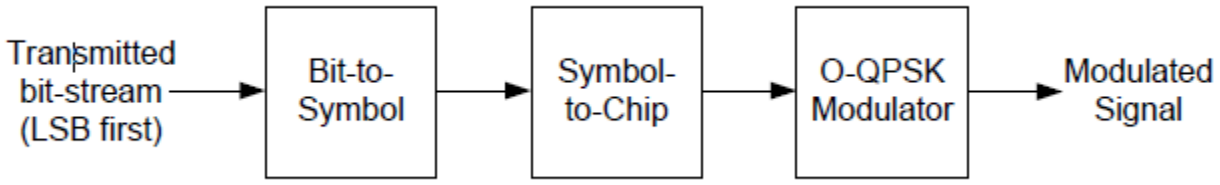

Figure 3: Modulation and spreading functions illustrated at block level

Each byte is divided into two symbols, 4 bits each. The least significant symbol is transmitted first. For multi-byte fields, the least significant byte is transmitted first, except for security related fields where the most significant byte is transmitted first.

Each symbol is mapped to one out of 16 pseudo-random sequences, 32 chips each. The symbol to chip mapping is shown in Table 3. The chip sequence is then transmitted at 2 MChips/s, with the least significant chip (C_0) transmitted first for each symbol.

Symbol	Chip sequence (C_0, C_1, C_2, … , C_{31})
0	1 1 0 1 1 0 0 1 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0
1	1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0
2	0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0
3	0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1
4	0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1
5	0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0
6	1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1
7	1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1
8	1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1
9	1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1
10	0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1
11	0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0
12	0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0
13	0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1
14	1 0 0 1 0 1 1 0 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0
15	1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0

Table 2: IEEE 802.15.4 Symbol-to-chip mapping

The modulation format is Offset-Quadrature Phase Shift Keying (O-QPSK) with half-sine chip shaping. This is equivalent to MSK modulation. Each chip is shaped as a half-sine, transmitted alternately in the I and Q channels with one half chip period offset.