UGPZAA User Manual

BLUETOOTH™ Low Energy Module

Model number	Function
UGPZAA	BLUETOOTH™ Version 5.2 (Class1.5)

Model number

Digit	Definition	Contents
Digit 1~3	Major model number	UGP: Wireless products
Digit 4	Destination	Z: Worldwide
Digit 5	Minor model number	A: CC2642
Digit 6	Specification	A: BLE with ANT

CAUTION:

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- This product （ or technology ） is subject to the Japanese Foreign Exchange and Foreign Trade law ,and is required to obtain an export license of the Japanese governmental agency , when exported from Japan.
- Do not use the product that is dropped in your process.
- Do not leave and treat the product in a place where it is subjected to strong magnetism or static electricity.
- Nozzle pressure for module mounting must be a 3N static load.
- This product is not water-resistant, dust-resistant and/or corrosion resistant for gas (e.g. hydrogen sulfide).

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1. GENERAL

This document contains the reference schematics. However, it is necessary to optimize according to the specification of selected Host CPU.

1-1. Features

1-1-1. Product Overview

This product is a radio frequency transceiver module compatible for BLUETOOTH™ Version 5.2 systems.

This product is BLUETOOTH™ Version 5.2 system in software.

The UGPZAA module include the Bluetooth protocols.
The Bluetooth protocol supports:

- Master, slave, multiple role support
- Extended advertising and scanning
- GAP: central, peripheral, observer or broadcaster roles
- ATT/GATT: client and server
- L2CAP
- Link Layer: AES-128 encryption and decryption
- RF Layer: Bluetooth Specification Version 5.2 compliant

This product supports a UART host interface for connecting the BLUETOOTH™ to the host processor.

♦ **UART Host Interface**

RS232 Protocol

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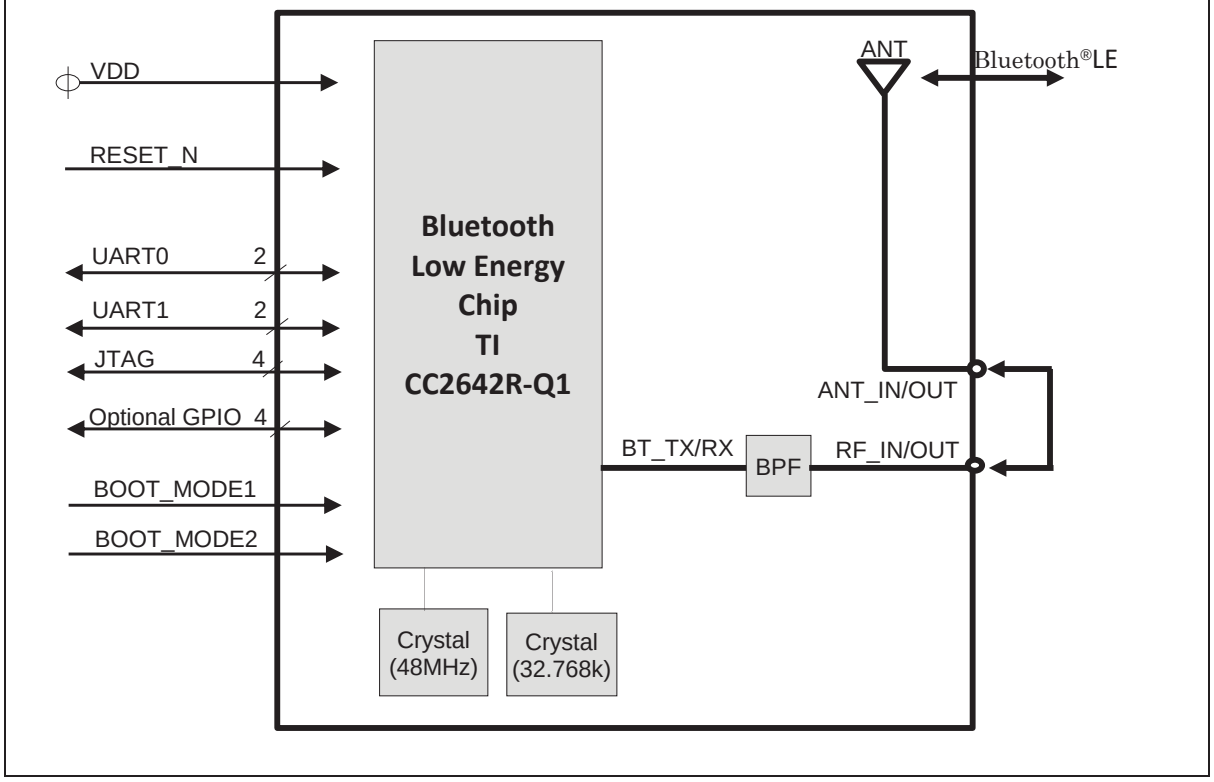
1-1-2. Block Diagram

Block Diagram



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1-2. Abbreviations

For the purposes of this document, the following abbreviations apply:

Abbre-viation	Definition
A	Ampere
AIO	Analog Input / Output
BALUN	Balance Un-balance circuit
BB	Base Band
BER	Bit Error Ratio
BPF	Band Pass Filter
bps	Bit Per Second
Co-ex	Co-existence
CPU	Central Processing Unit
CTS	Clear to Send
dBc	Electric power ratio to career
dBm	dB relative to 1 mW. *(1 mW = 0 dBm)*
ESD	Electrostatic Discharge
FEM	Front End Module
GND	Ground
HCI	Host Controller Interface
Hz	Hertz
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
IEEE	Institute of Electronic and Electrical Engineers
I/O	Input / Output
LDO	Low Drop Out regulator IC
LED	Light Emitting Diode
MAC	Media Access Control
Max.	Maximum
Min.	Minimum
NBS	Narrow Band Speech
NC	Non Connection

Abbre-viation	Definition
OTP	One Time Programming
PA	Power Amplifier
PCB	Printed Circuit Board
PER	Packet Error Ratio
PIO	Programmable Input / Output
ppm	Parts Per Million
PTA	PORTA
PTB	PORTB
PTC	PORTC
RAM	Random Access Memory
RF	Radio Frequency
RH	Relative humidity
ROM	Read Only Memory
RSSI	Received Signal Strength Indication
RTS	Request To Send
RX	Receive
s	Second
SoC	System on Chip
SPI	Serial Peripheral Interface
TCXO	Temperature Compensated X,tal Oscillator
Typ.	Typical
TX	Transmit
UART	Universal Asynchronous Receiver / Transmitter
V	Volt
X'tal	Crystal
ºC	degrees Celsius

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2. ELECTRICAL CHARACTERISTICS

2-1. Absolute Maximum Ratings

Item	Conditions
Storage Temperature	- 40 ~ + 105 [ºC]
Storage Humidity	~85 [%] RH (no-condensing)

Pin No. / Pin Name	Conditions
F14 / VDD	-0.3V ~ 4.1 [V]
--. Digital Input Pins	-0.3V ~ 4.1 [V]
--. RF Input Pins	+5.0 [dBm]

Note 1: The input maximum voltage must not exceed the V_{DD} absolute maximum voltage.

2-2. Operating Conditions

Items	Conditions	
Operating Temperature	Nominal:	+15 ~ +35 [ºC]
	Extreme:	-40 ~ +105 [ºC]

Pin No. / Pin Name	Conditions	
F14 / VDD	Nominal:	3.3 [V]
	Extreme:	3.0 ~ 3.63 [V]

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2-2-1. Digital Input / Output

VDD = 3.3V T= Operating Temperature

Pin No. / Pin Name	Conditions			
N6 UART0_TXD N5 UART0_RXD M9 UART1_TXD N9 UART1_RXD G14 RESET_N	V_{IN_Low}: V_{IN_High}: 2.5 ~ V_{OUT_Low}: V_{OUT_High}: 2.4 ~		~ 1.22 ~ 0.6	[V] [V] [V] [V]
M10 JTAG_TMSC N10 JTAG_TCKC J13 JTAG_TDI K13 JTAG_TDO	V_{IN_Low}: V_{IN_High}: 2.5 ~ V_{OUT_Low}: V_{OUT_High}: 2.4 ~		~ 1.22 ~ 0.6	[V] [V] [V] [V]
H14 BOOT_MODE1 J14 BOOT_MODE2	V_{IN_Low}: V_{IN_High}: 2.5 ~		~ 1.22	[V] [V]
G1 HOST_WAKE (option) H2 BLE_WAKE (option) J1 HOST_STATE (option) H1 BLE_STATE (option)	V_{IN_Low}: V_{IN_High}: 2.5 ~ V_{OUT_Low}: V_{OUT_High}: 2.4 ~		~ 1.22 ~ 0.6	[V] [V] [V] [V]

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3. RADIO CHARACTERISTICS

3-1. Common Physical Layer Characteristics

3-1-1. BLUETOOTH® Low Energy Specifications

Items	Conditions
Operating Frequency [MHz]	2402 ~ 2480 *1)
Operating channel spacing [MHz]	2
Number of Channel	40 *1)
Modulation	GFSK BT=0.5 2)

Note 1: The frequency and number of channels follows the regulatory domain.
Note 2: Data Rate and Modulation are as follows,

Data Rate [Mbps]	Modulation
1	GFSK BT=0.5
2	GFSK BT=0.5

LE Coded

Data Rate [kbps]	Modulation
500	GFSK BT=0.5
125	GFSK BT=0.5

3-2. Receiver Characteristics

The following specifications are guaranteed for nominal supply voltage and nominal temperature, unless otherwise specified.
This product is an antenna integrated communication module without RF connectors.
Therefore, the wireless characteristics described in this product specification are values at the module terminal "RF_IN/OUT".

3-2-1. BLUETOOTH® Low Energy Specifications

3-2-1-1. Receiver Sensitivity

VDD = 3.3V T=25℃

Data Rate [Mbps]	Min.	Typ.	Max.	Units
1	-	-95	-70	dBm
2	-	-90	-70	dBm
0.5	-	-98	-75	dBm
0.125	-	-103	-82	dBm

Note: PER < 30.8 [%]

3-3. Transmitter Characteristics

The following specifications are guaranteed for nominal supply voltage and nominal temperature, unless otherwise specified.
This product is an antenna integrated communication module without RF connectors.
Therefore, the wireless characteristics described in this product specification are values at the module terminal "RF_IN/OUT".

3-3-1. BLUETOOTH® Low Energy Specifications

3-3-1-1. Average Power

VDD = 3.3V T=25℃

Data Rate [Mbps]	Min.	Typ.	Max.	Units
1, 2, 0.5, 0.125	-	+2.0	-	dBm

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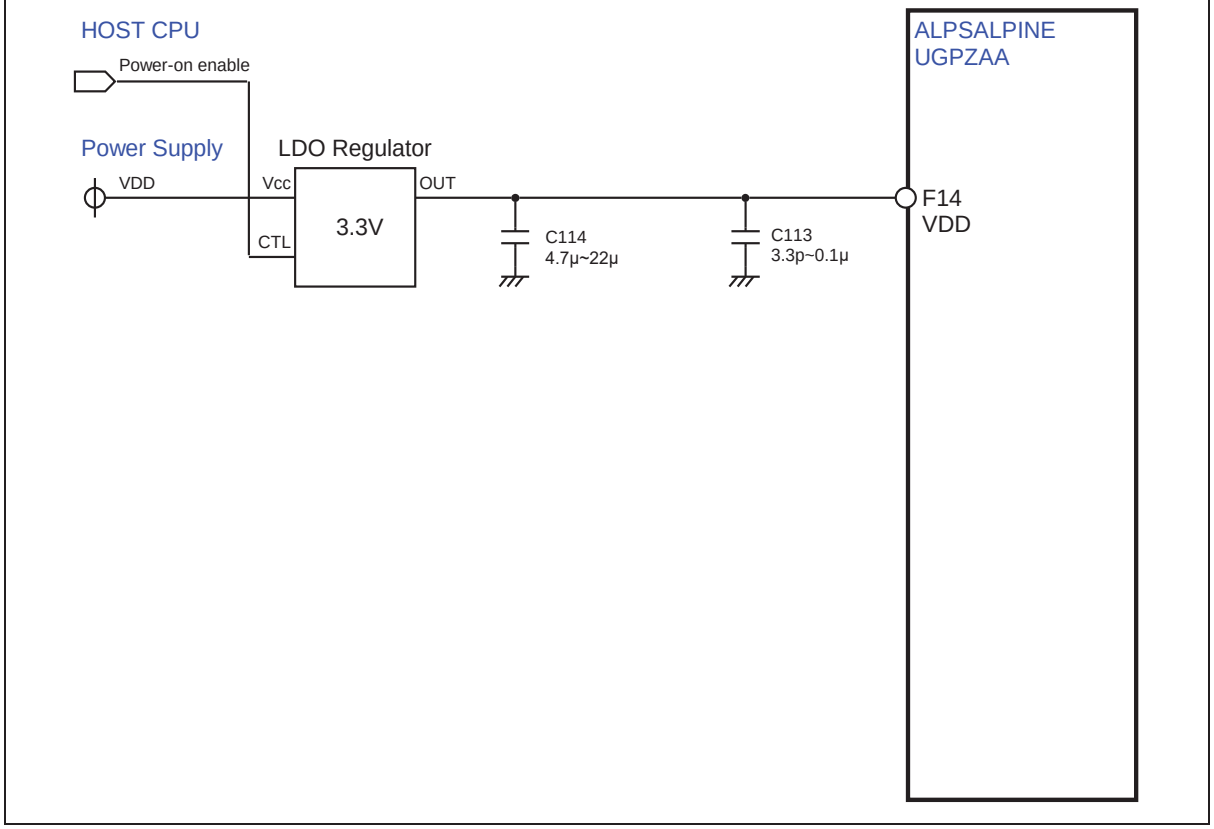
4. ELECTRICAL DESIGN INFORMATION

4-1. Power Supply Circuits

Thermal shutdown circuit and over-current protection circuit are recommended to be prepared. Please all bypass capacitors as close as possible to the terminals. In addition, the low ESL capacitor is recommended.

The share of regulator IC and the set to other voltage of the interface are possible besides a recommended circuits. However, take care about operating condition and stability condition.

Recommend circuit



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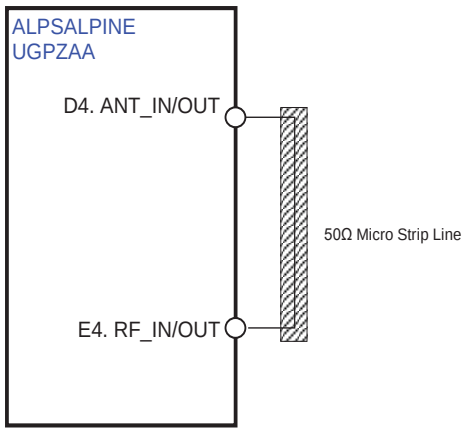
4-2. RF Connection Circuits

4-2-1. Connect Internal antenna 1

Recommend circuit



Note: The ground recommend to avoid the ANT pad and to be designed. In addition, the impedance of micro strip line should be use the 50Ω from ANT pad to RF connector, and its length should be shortest connecting.
The RF signal line should be surrounded by GND so that it is not affected by external noise.
Also, you should design with GND isolated from the RF signal line so as not to affect the 50Ω impedance line.

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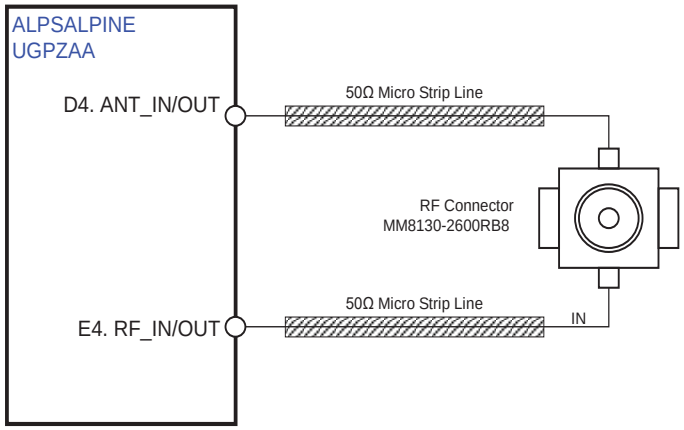
4-2-2. Connect Internal antenna and External connector 1

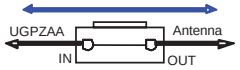
Recommend circuit



RF Connector

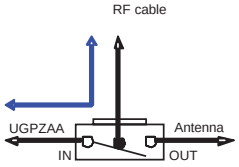
MM8130-2600RB8

Using an antenna
(Radiative)



if you use the antenna then don't insert connector.
(The antenna is shorted.)

Using a RF cable
(Conductive)



If you test the conductive performance then insert connector.
(The antenna is opened.)

Note: The ground recommend to avoid the ANT pad and to be designed. In addition, the impedance of micro strip line should be use the 50Ω from ANT pad to RF connector, and its length should be shortest connecting.
The 50Ω line should be routed on the back of the board on which the module will be mounted.
In that case, wire so that it does not overlap the ANT block of the module at the top and bottom.
The RF signal line should be surrounded by GND so that it is not affected by external noise.
Also, you should design with GND isolated from the RF signal line so as not to affect the 50Ω impedance line.

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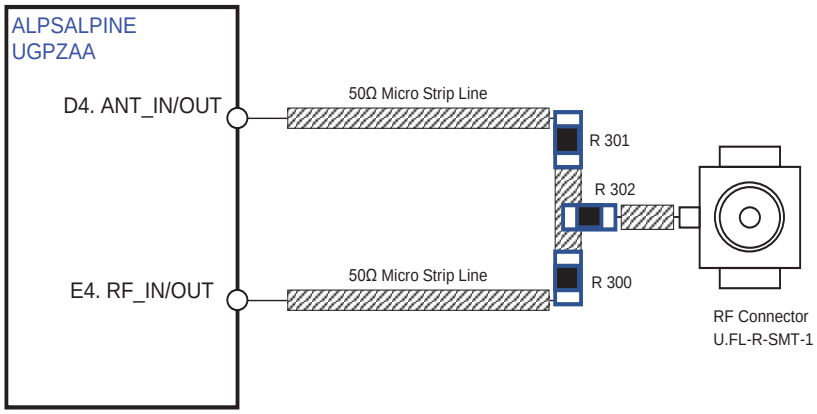
4-2-3. Connect Internal antenna and External connector 2

Recommend circuit



Note: The ground recommend to avoid the ANT pad and to be designed. In addition, the impedance of micro strip line should be use the 50Ω from ANT pad to RF connector, and its length should be shortest connecting.
The 50Ω line should be routed on the back of the board on which the module will be mounted.
In that case, wire so that it does not overlap the ANT block of the module at the top and bottom.
R3** is used as a bypass resistor(0Ω) when performing tests on wires. When using an internal antenna, R302 is NC.
The RF signal line should be surrounded by GND so that it is not affected by external noise.
Also, you should design with GND isolated from the RF signal line so as not to affect the 50Ω impedance line.

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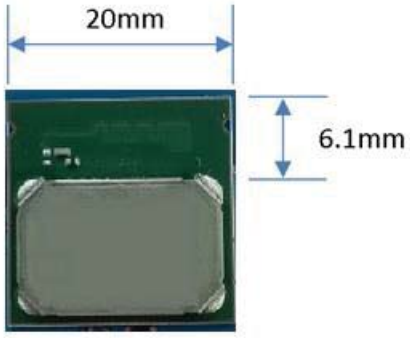
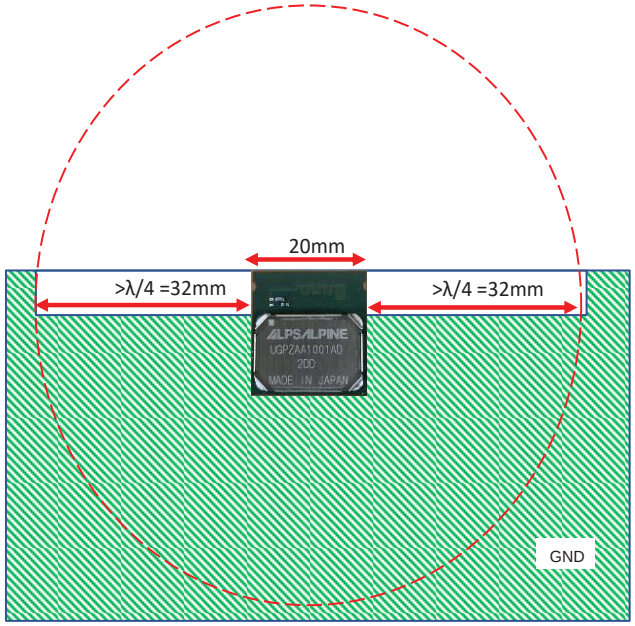
4-3. ANTENNA Information

Antenna	Antenna size	Antenna Type	VSWR	Peak Gain
Printed Antenna	20mm * 6.1mm	λ /4 Meander Line Antenna	2402-2480MHz 3.0 max	2.1 dBi



Recommended clearance from antenna to GND pattern



Note: From the antenna to GND, a clearance of 1/4 wavelength or more is desirable.
It is desirable that there are no metal parts in the red circle.

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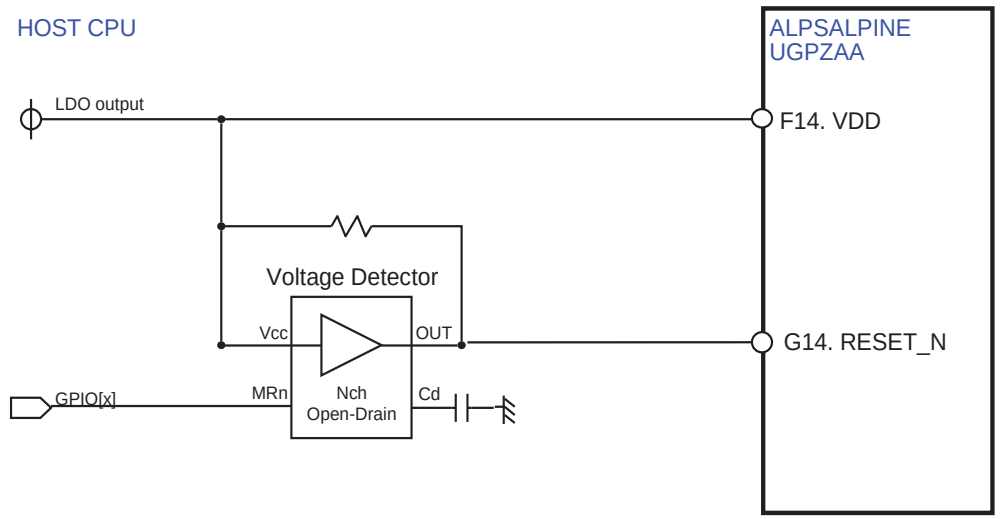
4-4. Hardware Reset Circuits

Proper design are important for optimal operation of the digital circuitry.

Synchronize to Detection of Voltage Drop [Basic]



Controls Directly from HOST CPU [Optional]

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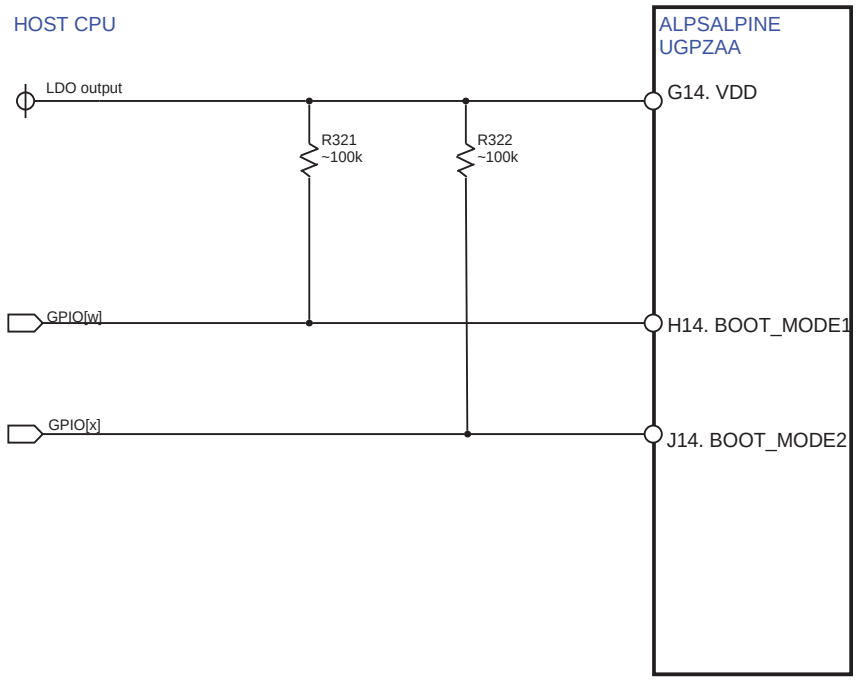
4-5. Boot Mode Configuration

4-5-1. Boot Mode Configuration

Application mode



Note: The pins listed in following Table is sampled when RESET_N de-assert to determine the various operating modes.

BOOT_MODE1	BOOT_MODE2	Mode
Low	X	Firm Ware download mode
High	Low	RF Test mode
High	High	Application mode

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4-6. Host Interface Circuits

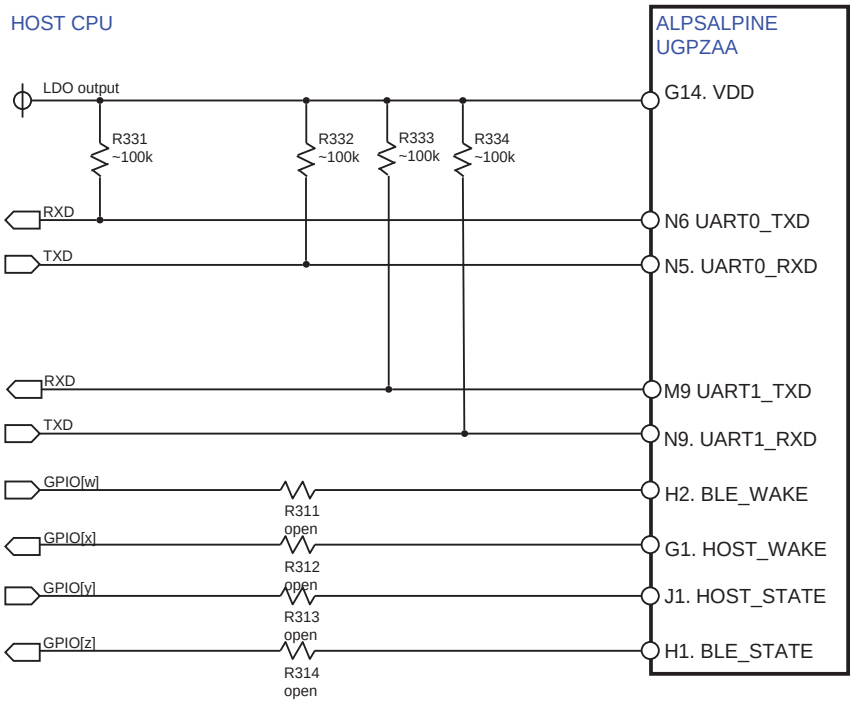
Proper design of data lines and clock lines are important for optimal operation of the digital circuitry. To prevent latch-up, short or some possible issues, keep drive voltage and current within range as specified.

4-6-1. Bluetooth™ Host Interface

The I/O voltage of UGPZAA and HOST CPU needs designing to same voltage.

4-6-1-1. UART Interface

No Flow Control Type



Note: Usually, the ref. R33x (pull-up resister) need. In addition, its resister should be optimizing to the host CPU.
The impedance of signal line should be matching to the clock rate.
BLE_STATE, BLE_WAKE, HOST_STATE and HOST_WAKE are connected to Host CPU only if used as the interrupt request signal.
UART1 are used only for RF testing.

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4-6-2. UART_0 Interface

The BLUETOOTH™ part has a standard UART serial interface that provides a simple mechanism for communicating using RS232 protocol. UART configuration parameters, such as baud rate and packet format, are set using firmware.

Parameter	Condition
Baud rate	Max 3M [bps]
Flow control	None or Hardware (RTS/CTS)
Parity	None
Number of stop bits	1
Bits per byte	8

Note: It is loaded by default setting when the Power On Sequence or Reset Sequence was executed.

4-6-2-1. Signal Description

Pin No. / Pin Name		I/O	Description		Signal
N6	UART0_TXD	O	[UART]	Data output	TXD
N5	UART0_RXD	I	[UART]	Data input	RXD

Note: I/O status : I = input / O = output / B = bi-directional / P = power supply.

4-6-3. UART_1 Interface

The BLUETOOTH™ part has a standard UART serial interface that provides a simple mechanism for communicating using RS232 protocol. UART configuration parameters, such as baud rate and packet format, are set using firmware.

Parameter	Condition
Baud rate	Max 3M [bps]
Flow control	None or Hardware (RTS/CTS)
Parity	None
Number of stop bits	1
Bits per byte	8

Note: It is loaded by default setting when the Power On Sequence or Reset Sequence was executed.

4-6-3-1. Signal Description

Pin No. / Pin Name		I/O	Description		Signal
M9	UART1_TXD	O	[UART]	Data output	TXD
N9	UART1_RXD	I	[UART]	Data input	RXD

Note: I/O status : I = input / O = output / B = bi-directional / P = power supply.

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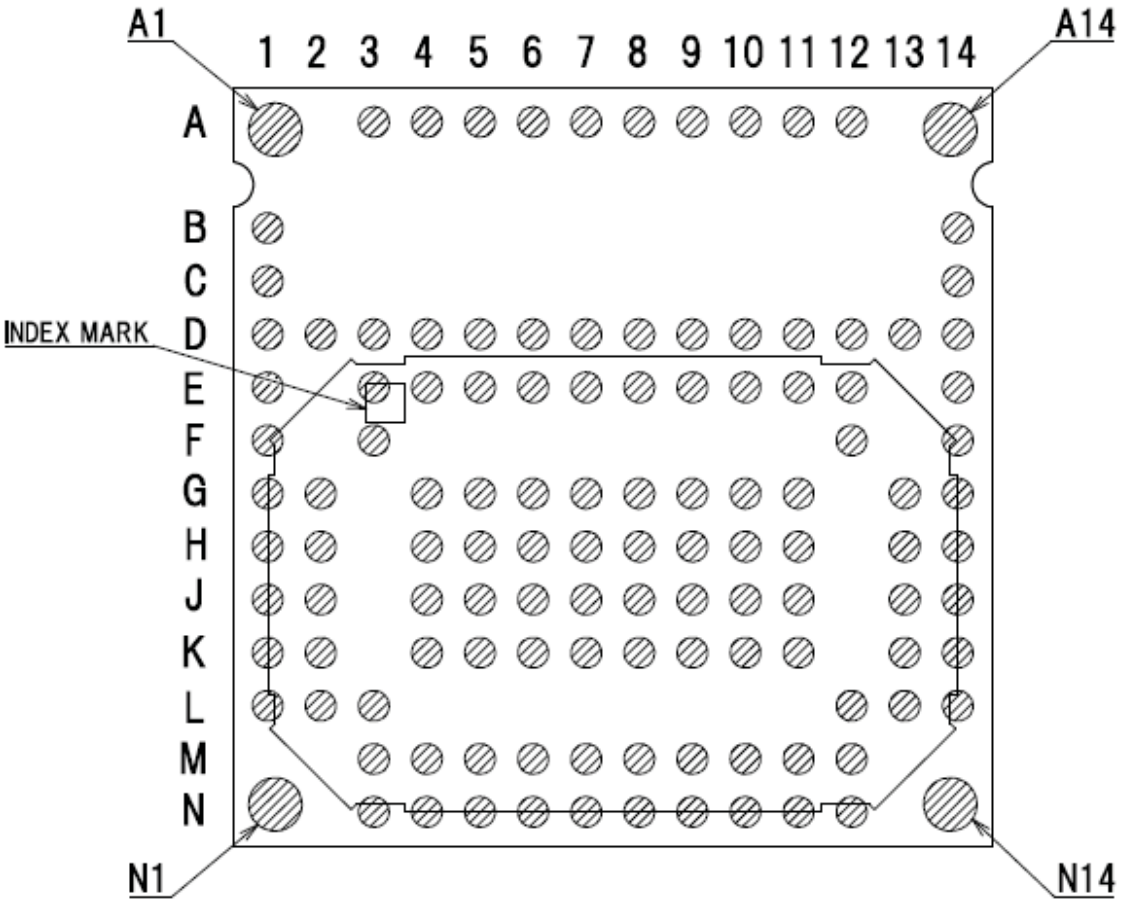
5. PIN CHARACTERISTICS

5-1. Pin Layout

Pin Number



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5-2. Pin Assignment

Pin No.	Pin Name	I/O	Description	
F14	VDD	P	[VDD]	Power supply
G14	RESET_N	I	[RESET]	Reset input (Active Low)
E4	RF_IN/OUT	B	[RF]	RF port for Bluetooth® Low energy
D4	ANT_IN/OUT	B	[ANT]	Port for module built-in Antenna
N6	UART0_TXD	O	[UART]	UART0 Data output
N5	UART0_RXD	I	[UART]	UART0 Data input
M9	UART1_TXD	O	[UART]	UART1 Data output (Test mode)
N9	UART1_RXD	I	[UART]	UART1 Data input (Test mode)
M10	JTAG_TMSC	I/O	[JTAG]	JTAG TSMC
N10	JTAG_TCKC	I	[JTAG]	JTAG clock
J13	JTAG_TDI	I	[JTAG]	JTAG Data input
K13	JTAG_TDO	O	[JTAG]	JTAG Data output
H14	BOOT_MODE1 (bit1)	I	[power on config]	MODE1: MODE2 0x= Firmware download mode 10=RF test mode 11= App mode (Internal pullup)
J14	BOOT_MODE2 (bit0)	I		
G1	HOST_WAKE (option)	O	[IRQ]	IRQ to HOST from BLE
H2	BLE_WAKE (option)	I	[IRQ]	IRQ to BLE from HOST
H1	BLE_STATE (option)	O	[STATE]	BLE STATE output
J1	HOST_STATE (option)	I	[STATE]	HOST STATE input
A1,A3,A4,A5,A6,A7,A8,A9,A10,A11,A12,A14,B1,B14,C1,C14,F1,G13,H13,L1,L3,L14,M5,M6,M7,M8,M11,N1,N3,N7,N8,N12,N14	NC	-		Non-connection terminal
D1,D2,D3,D5,D6,D7,D8,D9,D10,D11,D12,D13,D14,E1,E3,E5,E6,E7,E8,E9,E10,E11,E12,E14,F3,F12,G2,G4,G5,G6,G7,G8,G9,G10,G11,H4,H5,H6,H7,H8,H9,H10,H11,J2,J4,J5,J6,J7,J8,J9,J10,J11,K1,K2,K4,K5,K6,K7,K8,K9,K10,K11,K14,L2,L12,L13,M3,M4,M12,N4,N11	GND	-		Ground

Note: I/O status : I = input / O = output / B = bi-directional / P = power supply.
As for the un-used signal pin, it processes as well as NC (non-connection).

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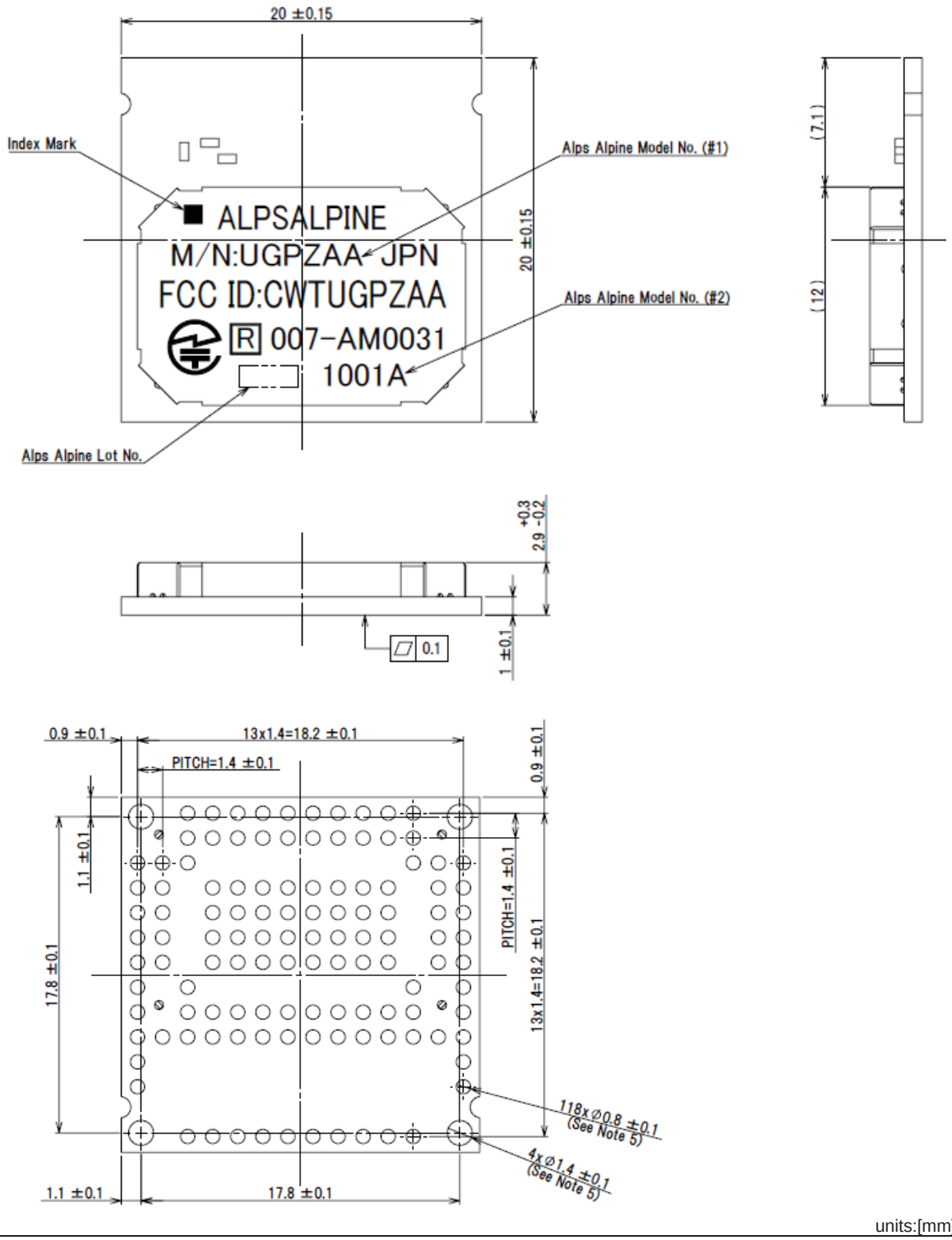
6. MECHANICAL CHARACTERISTICS

6-1. Mechanical Description

Description



units:[mm]

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Note: - Tolerances are ±0.3mm, unless otherwise specified.
- Alps Alpine Lot Number shall be conformed to Alps Alpine numbering rules.
- Dimensions in ( ) : It is reference dimension.
- The terminal coplanarity of module assumes the state of room temperature.
- Surface treatment specifications for module bottom terminal
  Material: Cu
  Surface finish: Ni-Au
  Ni 3um – 8um
  Au 0.05um – 0.15um
-The certification display shown in this figure is a sample display.

6-2. Mass

Typ. 1.6 [g]

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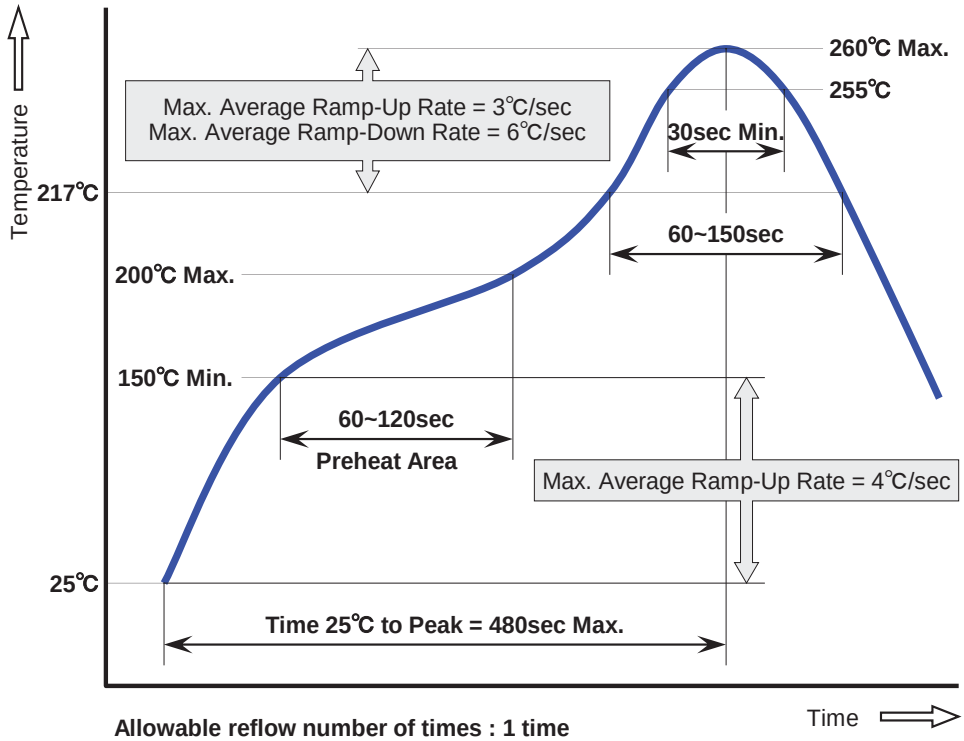
7. MECHANICAL DESIGN INFORMATION

The following drawings have been verified based on ALPS recommended reflow soldering condition and reference PCB. The reflow solderability should vary in accordance to thickness of PCB, reflow condition and pattern layout etc. As for the NC pin, please solder to the NC foot print pattern of the Main Board.

7-1. Soldering Conditions

7-1-1. Reflow heat resistance

Temperature profile



Allowable reflow number of times : 1 time

Note: 1.The measurement point is a center of the upper surface of the module.
2. Please execute the reflow soldering on the following conditions according to JEDEC J-STD-020D.
Peak Temperature：260℃Max Peak Time (≧255℃)：30secMax

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7-2. Storage Conditions

The following conditions shall be kept for soldering and keeping in storage this product.

1. Shelf life in dry bag: 12 months at 5 ~ 40 °C and < 85 % RH.

2. After dry bag is opened, module that will be subjected to soldering reflow or equivalent processing must be:

   a) Mounted within 168 hours at factory condition of < 30 °C / 60 % RH, or
   b) Stored at < 30 °C / 10 % RH.

3. Modules require baking, before mounting, if:

   a) Humidity Indicator Card is >10 % when read at 23 °C ± 5 °C, or
   b) Item 2.a) or 2.b) are not met.

4. If baking is required, device may be baked for 216 hours at 40 ~ 45 °C and < 5 % RH for low-temperature device containers.

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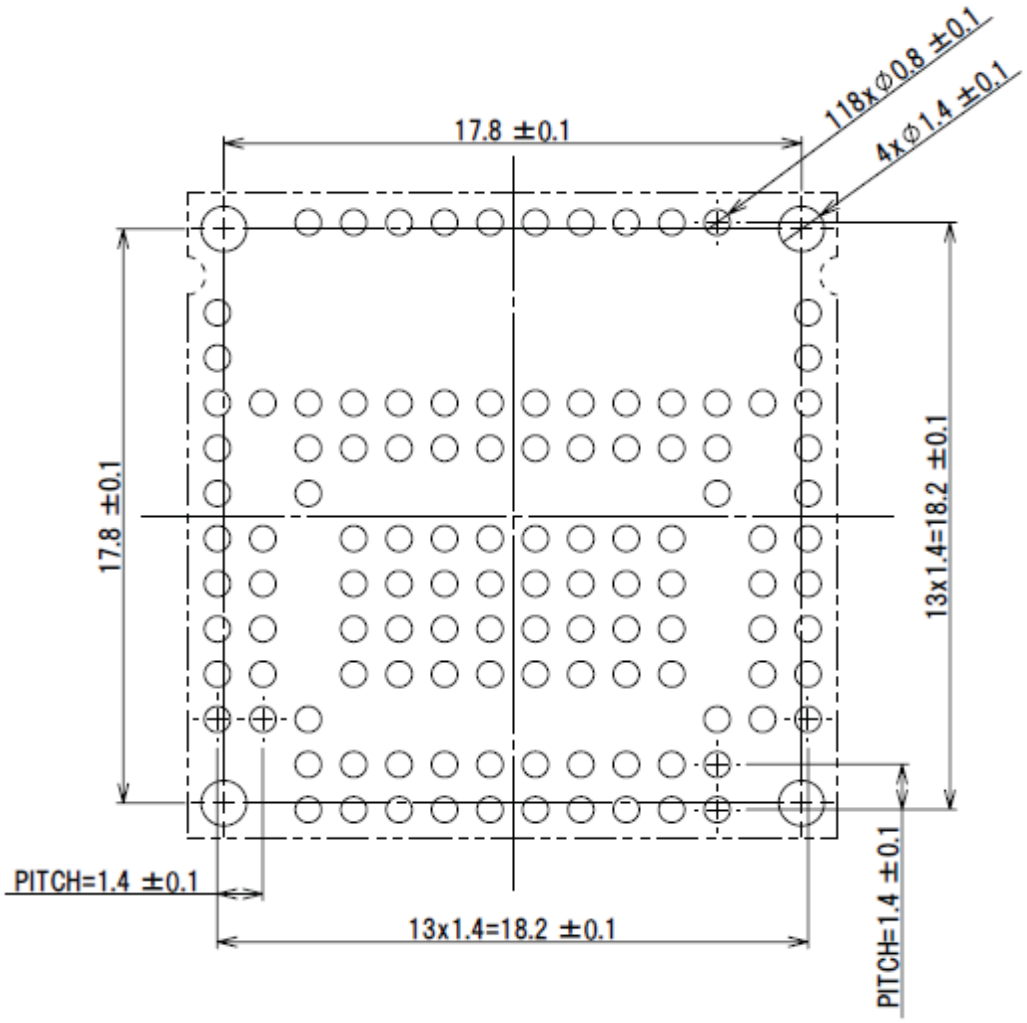
7-3. Copper Land Design

Top view



units : mm

Note: Tolerances are ±0.1mm, unless otherwise specified.
Dimensions in () : It is reference dimension.

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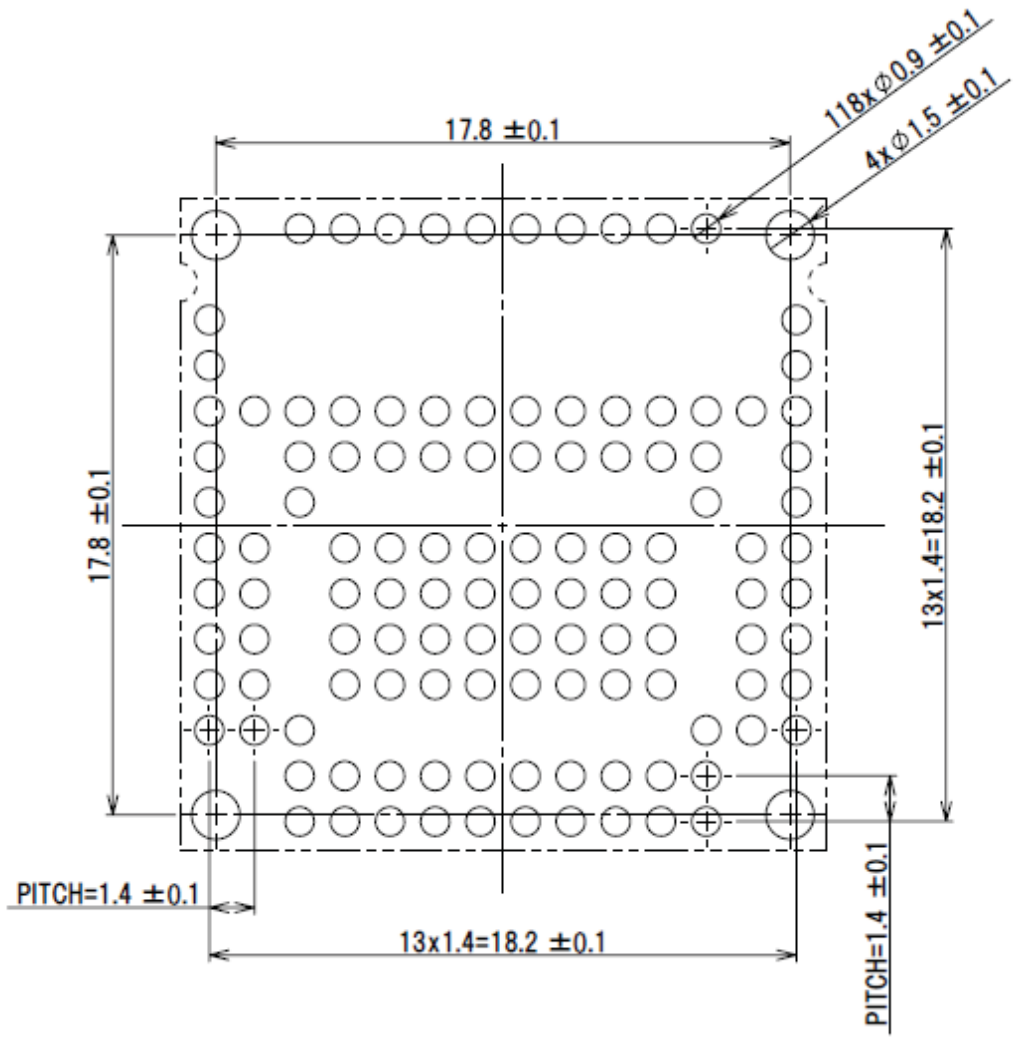
7-4. Solder Stop Mask Design

Top view



units : mm

Note: Tolerances are ±0.1mm, unless otherwise specified.
Dimensions in () : It is reference dimension.

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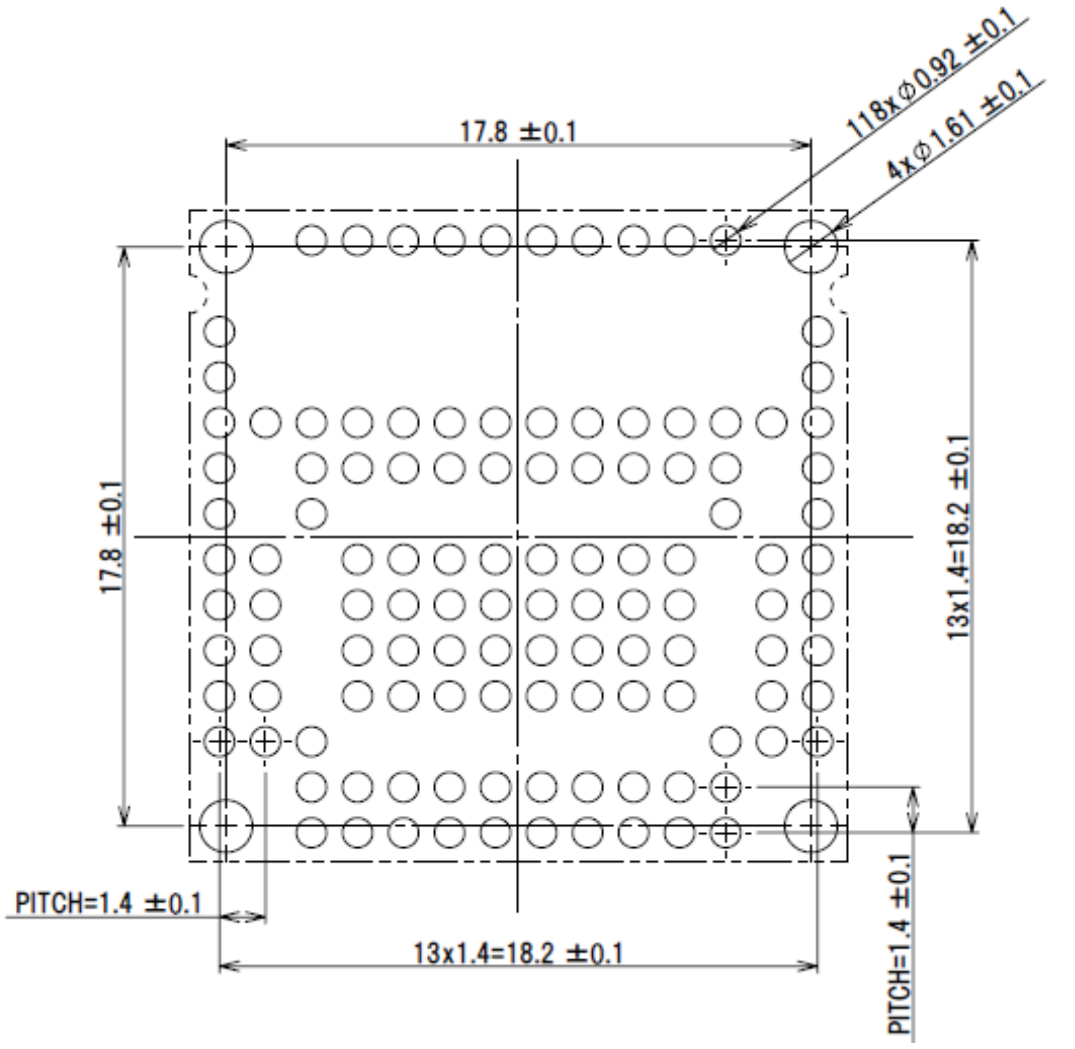
7-5. Solder Print Mask Design

Top view



units : mm

Note: Tolerances are ±0.1mm, unless otherwise specified.
Dimensions in () : It is reference dimension.
Metal thickness = 0.12 [mm]

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8. REGIONAL REGULATIONS

This Product has taken the following regulatory modular approval by the antenna described in the chapter 4-3.

a) Japanese Radio Law Certification
Article 2-1of the Certification Ordinance 19
b) FCC Certification
FCC Part15 SubpartC

Customer can certify their product without RF test for regulatory RF certification, if following conditions are satisfied. Otherwise additional RF certifications are necessary.

1) Antenna type (shape, size, etc.) shall be similar with the tested antenna by ALPSALPINE.
2) Antenna gain shall be lower than the tested antenna by ALPSALPINE.
3) EMC performance shall satisfy the condition of each certification.

These requirements shall be guaranteed by the customer.

9. FCC STATEMENT

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC CAUTION:
Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This transmitter must not be co-located or operated in conjunction with any other antenna or transmitter.

FCC requirements:

FCC KDB996369 D03 2.1 General : Applicable
This user manual describes the integration procedure per section 2.2 to 2.12 of KDB 996369 D03.

FCC KDB996369 D03 2.2 List of applicable FCC rules : Applicable
This device complies with below part 15 of the FCC Rules.
Part 15 Subpart C

FCC KDB996369 D03 2.3 Summarize the specific operational use conditions : Not applicable

FCC KDB996369 D03 2.4 Limited module procedures : Not applicable

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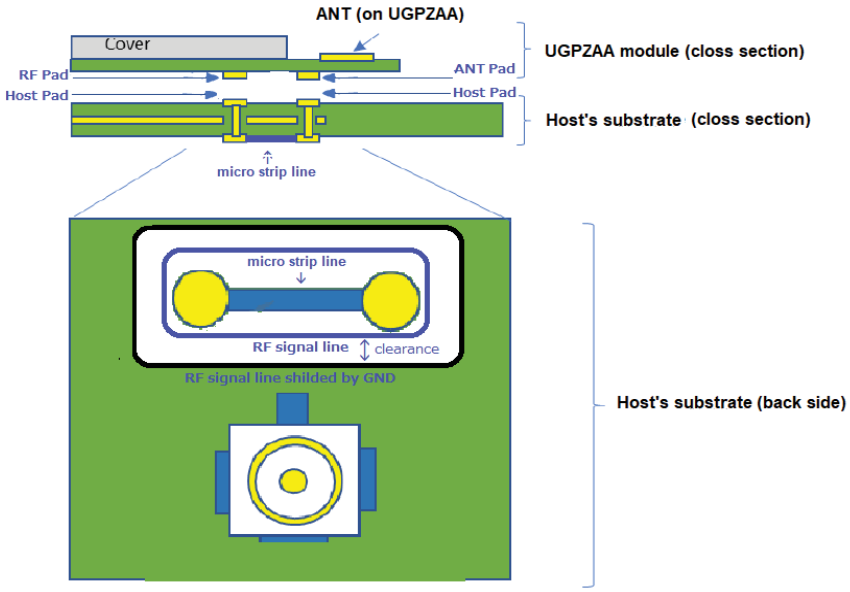
FCC KDB996369 D03 2.5 Trace antenna designs : Applicable

When this device implements to host device, host device should comply the following design guide for RF trace design.



1. Trace design layout

- Please connect the RF Pad and ANT Pad of UGPZAA module by using Host's micro strip line.
- The implementation of the Host Pads, through holes and the micro strip line are called "RF signal line".
- The impedance of the RF signal line should be using the 50Ω, and its length should be shortest connecting like above figure.
- Do not insert any amplifier in the RF signal line.
- Except for the RF signal line, make the surface layer of the mounting board solid ground as much as possible.
- Around the RF signal line, remove all layers of copper foil from the mounting board.
- From the RF signal line to GND, a clearance of 1/4 wavelength or more is desirable.

2. Parts list (BOM)

None (because it is directly connected)

3. Antenna (type)

λ/4 Meander Line Antenna of the UGPZAA

4. Connector (type)

None

5. Insulation requirements

The RF signal line should be surrounded by GND so that it is not affected by external noise. Also, you should design with GND isolated from the RF signal line so as not to affect the 50Ω impedance line.

And fine tuning of return loss etc. can be performed using the impedance matching circuit.
However, it is required to check "Class1 change" and "Class2 change" which the authorities define then.

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FCC KDB996369 D03 2.6 RF exposure considerations : Applicable

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment and meets
the FCC radio frequency (RF) Exposure Guidelines as this equipment has very low levels of RF energy.

FCC KDB996369 D03 2.7 Antennas : Applicable

The device is designed to use the antenna listed below. Do not modify the antenna or any other part of the module. Any modifications will invalidate the modular certifications and require new approvals for the host system.

Antenna Type : λ/4 Meander Line Antenna
Antenna Gain : Max. 2.1dBi

FCC KDB996369 D03 2.8 Label and compliance information : Applicable

Following information must be indicated on the host device of this module.
Contains Transmitter Module FCC ID: CWTUGPZAA
or
Contains FCC ID: CWTUGPZAA

FCC KDB996369 D03 2.9 Information on test modes and additional testing requirements : Applicable

Test modes should take into consideration different operational conditions for a stand-alone modular transmitter in a host, as well as for multiple simultaneously transmitting modules or other transmitters in a host product.

FCC KDB996369 D03 2.10 Additional testing, Part 15 Subpart B disclaimer : Applicable

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant FCC Part 15.247, and the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification.
The final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

FCC KDB996369 D03 2.11 Note EMI Considerations : Applicable

We recommend using "best practice" RF design engineering testing and evaluation in case non-linear interactions generate additional non-compliant limits due to module placement to host components or properties.
The host manufacturer is responsible for ensuring compliance with the applicable FCC rules for the transmitters operating individually and simultaneously. This includes compliance for the summation of all emissions from all outputs occupying the same or overlapping frequency ranges, as defined by the applicable rules.

FCC KDB996369 D03 2.12 How to make changes : Applicable

Only the grantee is permitted to make permissive changes. If any modification needed, please contact us, ALPS ALPINE CO., LTD..

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