2.2 Limiter circuit

The limiter circuit is a diode limiter amplifier comprising a reverse amplifier. Internal action point is set to 1/2Vcc. Gain is set so that limiter works when the input level of 1 pin, 22 pin is -13dBV (at 400Hz) or higher.

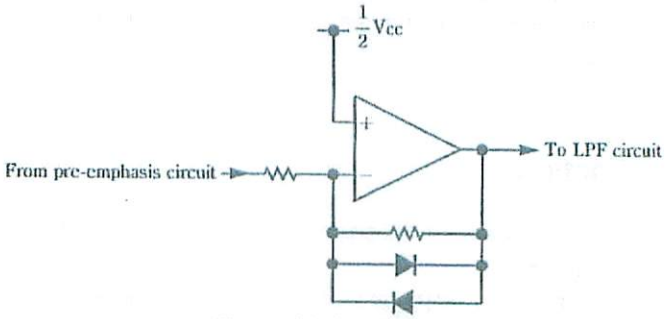

Fig. 2 Limiter circuit

2.3 LPF circuit

The LPF circuit comprises a multi feedback type secondary low pass filter. Filter characteristic is vessel characteristic where delay characteristic is flat. Cutoff frequency is set at 15kHZ. Filter constant is as shown below.

$Q=0.577,\ \omega_0=1.274,\ f_c=15kHz$

$R_1=R_2=R_3=R_f=100k\Omega$

$$C_f=\frac{1}{\omega_0 R_f}=\frac{1}{2\pi\times1.274\times15k\times100k}=83.28pF$$

$$C_1=3Q\ C_f=3\times0.577\times83.28p=144pF\fallingdotseq150pF$$

$$C_2=\frac{C_f}{3Q}=\frac{83.28p}{3\times0.577}=48pF\fallingdotseq50pF$$

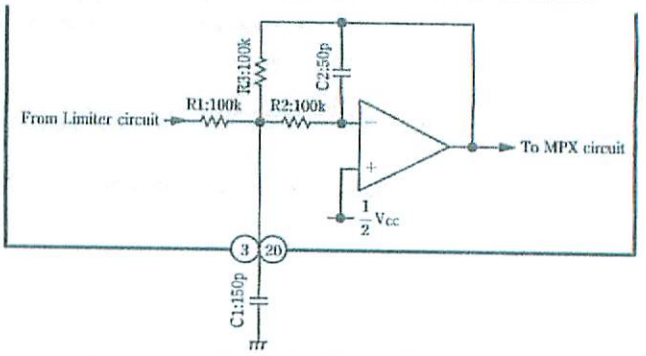

Fig. 3 LPF circuit

2.4 MPX circuit

Audio signals input from 1 pin, 22 pin are input via the pre emphasis circuit, the limiter circuit, the LPF circuit, to the MPX circuit. On the other hand, 7.6MHz crystal oscillator between 13 pin and 14 pin is divided into 1/200 and 38kHz sub carrier is made and it is divided into 1/2 and 19kHz pilot signal is made. Audio signals and 38kHz sub carrier are level modulated by multiplexer, and main signal of L + R, and sub signal DSB modulated by signal L - R of 38kHz sub carrier are generated, and further 19kHz pilot signal is added, and output as composite signal from 5 pin.

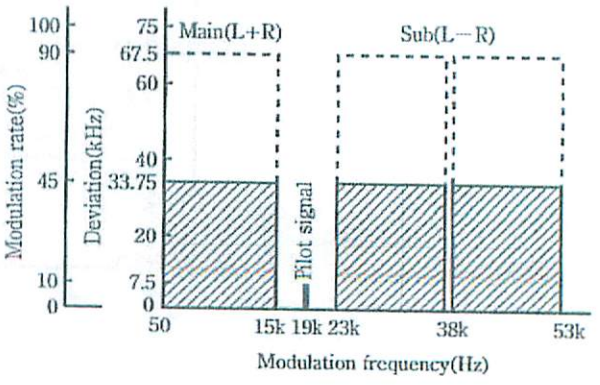

Fig. 4 GE-Zenith (pilot tone) method stereo broadcasting frequency spectrum

The MPX circuit is controlled by the serial data of 17 pin, and monaural action of only L + R signal is available (only BH1415F/FV and BH1418FV/KN). And, audio mute works by the control terminal of 18 pin. At this moment, the pilot signal remains output (only BH1415F/FV and BH1418FV/KN).

2.5 FM transmitter circuit

The FM transmitter circuit adopts PLL method and stabilizes frequency. This block comprises an RF oscillator, an RF amplifier, and a PLL frequency synthesizer. The FM modulator is structured by an external variable capacity diode. The RF oscillator becomes VCO of PLL, and FM modulation is made to this VCO directly by audio signal.

The RF oscillator comprises a deformed clap (colpits) circuit, and adds LC oscillation time constant to 9 pin as external part.

The oscillation waveform is amplified by RF amplifier 1 stage and output from 11 pin.

On the other hand, PLL phase compares oscillation frequency, and serial data in the case of BH1415F/FV and BH1418FV/KN, and the frequency given by hardware control in the case of BH1416F and BH1417F/FV, and outputs error component to 7 pin. As for the error component, DC component is fed back to VCO via LPF.

When the transmission frequency divided by N is higher than the reference frequency, high level is output from the PD output, and when it is lower, low level is output. At coincidence, high impedance gets in

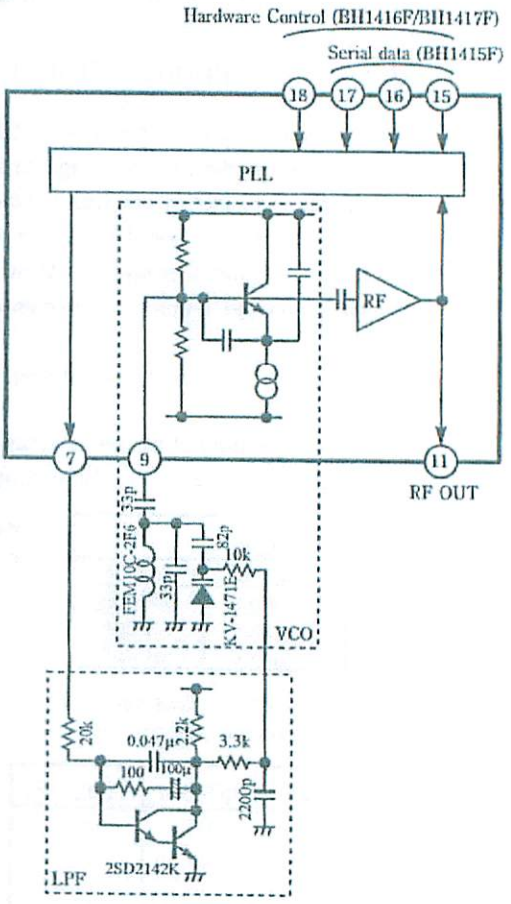

Fig. 5 FM transmitter circuit

3. Description of external parts

Note : The terminal numbers described in the present document are for BH1415F, BH1416F, and BH1417F of SOP20 package version.
As for BH1415FV, BH1417FV, BH1418FV of SSOP-B24 package version, and BH1418KN of VQFN28 package, replace the terminal numbers for use.

3.1 Pre emphasis (Pin 1, 2, 21, 22)

1 pin, 22 pin input terminal is set at 1/2Vcc by the internal bias, therefore be sure to connect it via a coupling capacitor C1 to the previous stage circuit. As for the polarities of the coupling capacitor, set the one whose DC voltage is higher by the output of the previous stage circuit and the input of IC as plus electrode.

By the value of C1 and the value of 1 pin, 22 pin input impedance, HPF is structured, and low area cutoff frequency of input is determined. When the value is small, the reduction of input signal is cut. And when the value is too large, a pop sound occurs when the power source is supplied, and starting take much time.

Input cutoff frequency $f_{CL} = \dfrac{1}{2\pi \cdot 43k \cdot C_1}\ (Hz)$

The time constant of the pre emphasis is determined by the capacitors C2 of 2 pin, 21 pin and resistance 22.7kΩ of IC inside. Time constant $\tau = 22.7k \cdot C_2$

Time constant	C2
50μsec	2200pF
75μsec	3300pF
107μsec	4700pF
155μsec	6800pF

Table 1 Pre emphasis time constant and external capacity value

Set the time constant at 155μsec (C2 = 6800pF) or below.
In the case not to work pre emphasis, open 2 pin, 21 pin.

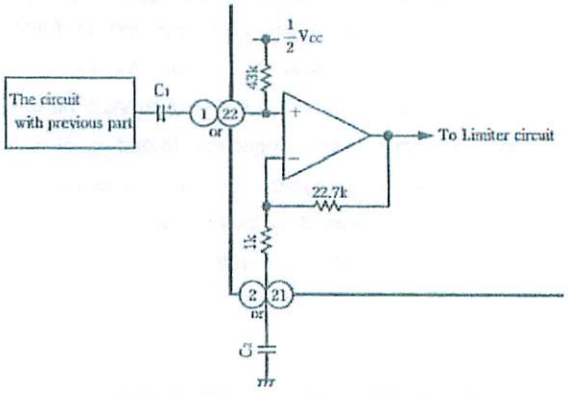

Fig. 6 Pre emphasis external parts

Frequency(Hz)	50μS(dB)	75μS(dB)
400	0.07	0.15
1k	0.41	0.87
2k	1.45	2.76
3k	2.76	4.77
4k	4.11	6.58
8k	8.64	11.82
10k	10.36	13.66
15k	13.66	17.07

Table 2 Pre emphasis frequency characteristic

Pre emphasis time constant is determined by the radio wave law of each country. 75μS in USA, 50μS in other countries. For use all over the world, 75μS is recommended. And to emphasize high area of audio, set it at 107μS or 155μS.

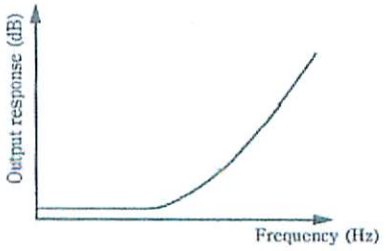

Fig. 7 Pre emphasis frequency characteristic

3.2 Low pass filter (Pin 3, 20)

Connect a 150pF capacitor to between 3 pin and GND and between 20 pin and GND. This is part of LPF circuit constant, therefore, even if this value is changed, the LPF cutoff frequency cannot be changed.

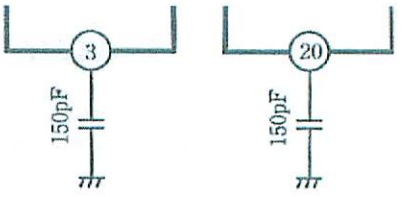

Fig. 8 LPF external parts

When audio of digital audio is input, a beat sound of several kHz may occur. This is because between the sampling frequency included in digital audio signal, and 38kHz as the sub carrier frequency of the IC, a beat occurs. And when a large amplification signal over 15kHz is input, a beat occurs between 19kHz as pilot signal, and the receiver sees malfunction and noise may occur.

To solve the above problem, cut the input signal of 15kHz or higher before 1 pin, 22 pin input terminal.

The circuit example using LPF manufactured by TOKO (19kHz/38kHz low pass trap filter) is shown below.

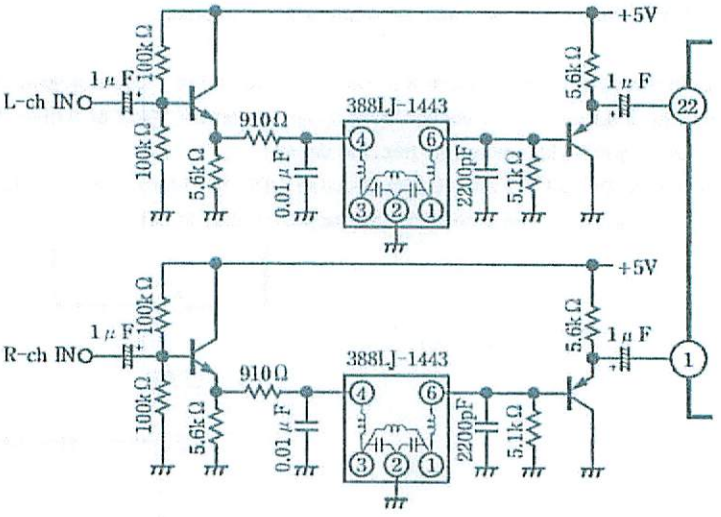

Fig. 9 19kHz/38kHz low pass trap filter circuit example

Item	Standard
14.0kHz att.	3.5dB max.
19.0kHz att.	18dB min.
19 ~ 38kHz att.	10dB min.
38.0kHz att.	30dB min.
38k ~ 100kHz att.	20dB min.
1.0kHz att.	1dB min.

Table 3 Characteristic of LPF 388LJ-1443manufactured by TOKO

By the way, in BH1414K, this 19kHz/38kHz low pass trap filter is built in, and countermeasures against this problem have been taken.

3.3 Power supply ripple filter (Pin 4)

Connect 10μF capacitor to between 4 pin and GND. If this value is small, distortion or mute attenuation amount deterioration occur. If it is large, the rise time at the power supply becomes long.

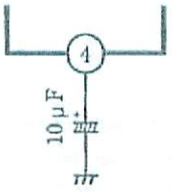

Fig. 10 Power supply external parts

3.4 Adjustment of modulation rate (Pin 5)

Adjustment of modulation rate is made between 5 pin composite signal output terminal and external FM modulator.

For example, in the case of adjustment of modulation rate by the method below, determine the values of R_1 and R_2 so that the load resistance viewed from 5 pin should be 10kΩ or higher. When the load resistance viewed from 5 pin is small, distortion may become worse.

C_1 is a capacitor for DC cut. C_1 and R_1, R_2 structure HPF, therefore select a value at which low area is not cut. By the way, the output impedance of 5 pin is approximately 200Ω.

Cutoff frequency $f_{CL} \fallingdotseq \dfrac{1}{2\pi C_1(R_1+R_2)}$ (Hz)

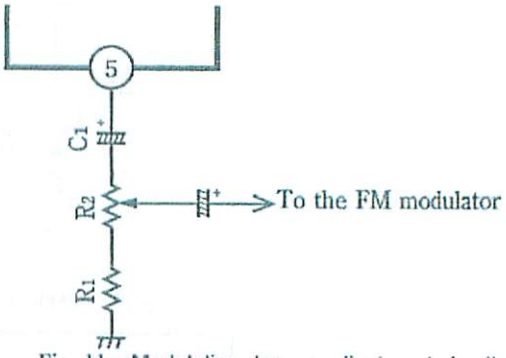

Fig. 11 Modulation degree adjustment circuit

This IC is set inside so that when a sine wave of 400Hz, -20dBV is input to 1 pin and 22 pin, in composite output of 5 pin, it should stand that L + R = 85%, Pilot = 15%. Pilot modulation degree is set at 15% as standard value because when the phase of the pilot signal is adjusted by separation adjustment and the likes, amplitude goes down, but modulation degree should not go down below 10% greatly. When you want to adjust the modulation degree of Pilot precisely, insert resistance between 19 pin and GND to lower the Pilot modulation degree.

As for the final modulation degree, adjust R_2 while measuring by a straight line detector so that the FM modulation degree should become 100% (for example, frequency deviation is ±75kHz).

3.5 VCO (Pin 9)

VCO is a deformed clap oscillator composed of bipolar transistors. The characteristics of this circuit are that drastic change of impedance in the parallel resonance circuits (L, C) is not likely to affect oscillation conditions and that stable oscillating performance can be obtained against the change of the transistors themselves because the capacity of the feedback capacitor (built in the IC) greatly exceeds the transistor capacity. Especially, because Q characteristics of the parallel resonance circuit using variable capacity diode fluctuates drastically by the control voltage, the more stable circuit will be required.

The VCO circuit is the most important section in PLL. Remove the VCO circuit from the loop and apply the control voltage at its upper limit and lower limit to confirm that VCO oscillates at the upper and lower limits within the specified frequency range. Particularly, note that, if the loop is locked in the high-frequency range, noise may be generated or the loop is unlocked at the margin of the upper/lower limit setting frequency by external factors. Therefore, VCO must be electrically and mechanically stabilized. From a view point of mechanism, pay special attention to fasten the coil. For a hollowed coil, fill paraffin with the coil to secure it. For a hollowed coil with bobbin, fix the coil with varnish, resin or adhesive. When a ferrite core or non-magnetic metallic core (for example, aluminum) is inserted in the bobbin, fix it securely so that it will not move by vibration. These treatments will make VCO less likely to be affected from modulation by vibration.

From a view point of temperature, it is preferable that the temperature characteristics are almost flat around the center of the frequency variable range. When the loop is locked, it apparently looks stable. However, the loop may be unlocked at the margin of the upper/lower limit setting frequency because the control voltage drifts by temperature accordingly.

Calculating the VCO constant

This example sets the VCO oscillation frequency within the range from 76.0MHz to 79.0MHz and sets control voltage V_T to 1V to 2V. Therefore, the best variable capacity diode VCD to be used is the one for synchronizing electrons in the VHF range. Select the variable capacity which can cover from several pFs to tens of pFs.

In the following case, KV1471E (Rank 2) of Toko is used.

Parameter	Min.	Typ.	Max.	Unit	Condition
Reverse voltage V_R	16	—	—	V	I_R=10μA
Capacitance C_1	33.30	35.60	37.13	pF	V_R=1V
Capacitance C_2		22.00		pF	V_R=2V
Capacitance C_3		12.00		pF	V_R=3V
Capacitance $C_{4.5}$	6.20	7.70	9.20	pF	V_R=4.5V
Capacitance C_5		6.50		pF	V_R=5V
Capacitance ratio A	5.00	—	—		C_1/C_5
Serial resister Rs	—	0.8	1.0	Ω	V_R=1.5V

Table 4 Characteristics of Variable Capacitance Diode KV1471E (Rank 2)

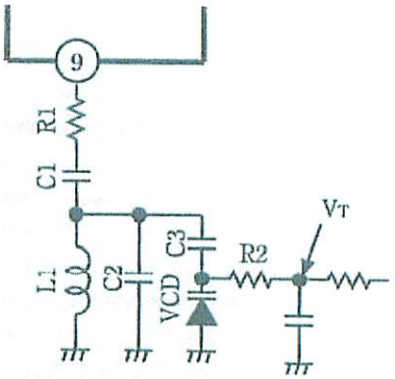

Fig. 12 VCO circuit

Padding capacitor C_3 to be inserted serially in the variable capacity diode VCD is intended to adjust the oscillation frequency range. Set the value to 47pF to 100pF, depending on the type of components of the variable capacity diode and oscillation circuit. As the value becomes larger, Q of the variable capacity diode VCD gives more influence to the LC resonance circuit. Since Q of the whole oscillation circuit falls, an oscillation may become unstable. On the other hand, as the value becomes smaller, the control voltage

variable range becomes larger to be applied to the variable capacity diode VCD in order to make the frequency value variable. As a result, Q of the variable capacity diode VCD will drastically fluctuate depending on frequency.

As the VCO sensitivity also changes, the modulation degree will greatly change depending on the transmission frequency. In this example, the value is set to 82pF through experiment.

Set the inductance value of coil L_1 so that reactance X1 becomes 50 to 100Ω.

When f_{TX} = 77.5MHz:

$$L1 = \frac{XL}{2\pi f_{TX}} = \frac{50}{2\times 3.14\times 77.5\times 10^{6}} = 0.103\,\mu H$$

The variable coil with bobbin in which a ferrite core is inserted, FEM10C-3F6 ($3\frac{1}{2}$T) manufactured by Sumida Corporation, is used.

Product name	Color	Number of turns	Core	Tuning capacitance	Q at non-load	Measured frequency
FEM10C-2F6	Red	$2\frac{1}{2}$T	Ferrite	61 pF ± 5% or more variable	115 or more	80MHz
FEM10C-3F6	Orange	$3\frac{1}{2}$T	Ferrite	43 pF ± 5% or more variable	115 or more	80MHz

Table 5 Oscillation coil characteristics

Capacitor C_2 to be connected in parallel to coil L_1 is intended to adjust the oscillation frequency range. As the C_2 capacity becomes larger, the variable range becomes narrower.

When fmin = 76MHz, the total capacity to be inserted parallel to coil L_1, C_{Tmin} is calculated as:

$$C_{Tmin} = \frac{1}{\omega^2 L_1} = \frac{1}{(2\times 3.14\times 76\times 10^{6})^2\times 0.103\times 10^{-6}} = 42.6pF$$

When fmax = 79 MHz, the total capacity to be inserted parallel to coil L1, C_{Tmax} is calculated as:

$$C_{Tmax} = \frac{1}{\omega^2 L_1} = \frac{1}{(2\times 3.14\times 79\times 10^{6})^2\times 0.103\times 10^{-6}} = 39.4pF$$

By subtracting the variable capacity diode VCD and padding capacitor C_3 serial capacity from the total parallel capacity, parallel capacity C_2 is calculated to be about 20pF. Then, through experiment, adjust the values of parallel capacitor C_2 and coil L_1 so that control voltage V_T becomes the given voltage value. In this example, the value of parallel capacitor C_2 is set to 33 pF and coil L_1 is adjusted so that control voltage V_T becomes 1.2V at 76.0MHz. Control voltage V_T at 79.0MHz becomes 2.0V.

To offset the positive temperature characteristics of coil L_1, a temperature compensation ceramic type parallel capacitor C_2 is used as parallel capacitor C_2. Generally, for the hollowed core coil, use RH type (-220 ± 60ppm/°C) or SH type (-330 ± 60ppm/°C), and for the ferrite core coil, use TH type (-470 ± 60ppm/°C) or UJ type (-750 ± 120ppm/°C).

To take measures against high harmonics, use coupling capacitor C_1 and dumping resister R_1. Select coupling capacitor C_1 of 33pF to 100pF. As the value becomes larger, change of the external circuit becomes more likely to affect the internal oscillation circuit and may cause unstable oscillation. On the other hand, as the value becomes smaller, Q of the oscillation circuit drops and oscillation is likely to stop.

In this example, the value is set to 33pF.

Then, monitor the antenna terminal using a spectrum analyzer to observe high harmonics. Be sure to establish impedance matching (50Ω and 75Ω). If not, you cannot observe the high harmonic level correctly.

Insert dumping resister R_1 so that the high harmonic level becomes less than the desired value. The value

should be 15Ω to 100Ω. The value must conform to the Radio Law of the country to which the product will be exported. (For example, compared to the primary wave, the second and third high harmonic waves should obtain 30dB or more attenuation, and the fourth or upper high harmonic waves should obtain 50dB or more attenuation.)

To confirm the oscillation margin,

1. Touch the oscillation circuit by hand to deactivate it. Then, let the circuit go and check that the circuit restarts oscillation.
2. Check that the circuit oscillates when power voltage is set below 2.0V. Note that PLL is unlocked.
3. Increase the predetermined value of dumping resister R_1 by two ranks (using the E12 series) and check that the circuit oscillates. For example, if 1 and 2 above are OK at 47Ω, change the R_1 value to 68Ω and check that the circuit oscillates.
   E12 series: 10, 12, 15, 18, 22, 27, 33, 39, 47, 56, 68, 82, 100Ω
4. If the circuit does not oscillate by the above methods, enlarge coupling capacitor C_1 and replace coil L_1 and variable capacity diode VCD with those having higher Q.

R_2 is inserted so as to enhance impedance of the circuit to be connected parallel to the variable capacity diode VCD. For R_2, insert resister of some tens kΩ. In this example, a resister of 10kΩ is used.

3.6 PLL loop filter (Pin 7)

When the active type loop filter is used, select the amplifier which has less input leak current (which has high input impedance). Otherwise, leakage will occur and generate noise, causing PLL with poor C/N ratio. For this reason, it is recommended that you should use the Darlington connection transistor or FET for the amplifier.

In this example, ROHM Darlington transistor 2SD2142K is used to construct a lag lead type filter featuring excellent response performance. The lag lead type filter is combination of lag (delay) and lead (advance). $(R_1 + R_2)*C_1$ is the element for lag time and R_2*C_1 is the element for lead time. In this filter, f_1 determines the main response time and f_2 determines the dumping characteristics (design to suppress overshoot and ringing. In this PLL, set shutoff frequency f_1 to a lower value in order to directly modulate sound to VCO.

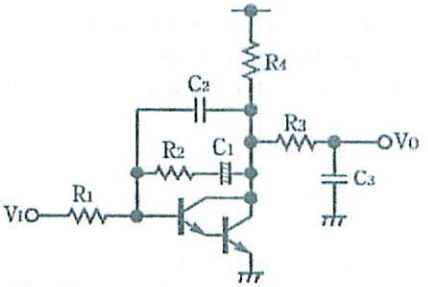

Fig. 13 PLL loop filter Characteristics

V_{CEO}(V)	Ic(A)	Pc(W) (Ta=25 °C)	h_{FE}
32	0.3	0.2(SMT3)	5k ~

Table 6 Transistor 2SD2142K Characteristics

The parameters are set as R1 = 20kΩ, R2 = 100Ω and C1 = 100μF.

$$f_1=\frac{1}{2\pi C_1(R_1+R_2)}$$

$$=\frac{1}{2\pi\cdot100\times10^{-6}\cdot(20\times10^{3}+100)}=78mHz$$

$$f_2=\frac{1}{2\pi C_1R_2}=\frac{1}{2\pi\cdot100\times10^{-6}\cdot100}=15.9Hz$$

$$\tau_1=C_1(R_1+R_2)$$

$$=100\times10^{-6}\cdot(20\times10^{3}+100)=2sec$$

$$\tau_2=C_1R_2$$

$$=100\times10^{-6}\cdot100=10msec$$

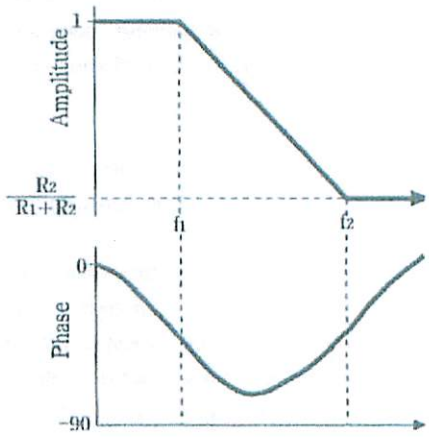

Fig. 14 PLL Loop Filter Characteristics

Because of large time constant, it takes long time to lock the value to the setting frequency. This shows a tradeoff relationship with the characteristics of amplitude and distortion by modulating at low range frequency (up to 100Hz).

In other words, by setting the frequency lock time faster, the distortion rate is deteriorated in the low range frequency, and by improving the characteristics of amplitude and distortion rate at the low range frequency, the frequency lock time becomes longer. Therefore, you should obtain the constant of LPF through experiment.

In the above expression, time constant τ_2 is considered to be equal to C1R2 ($\tau_2=C_1R_2$). However, by taking gain of the amplifier into account, $\tau_2=C_1\left(R_2-\frac{1}{g_m}\right)$

As R2 becomes smaller, influence of gm increases, making the loop operation unstable. By increasing the R4 value in order to increase bare gain of the amplifier, current which flows into the transistor is reduced, making gm smaller. Then, the loop operation becomes unstable as it does when setting the smaller value for R2. Increase the power voltage of the amplifier to cope with the situation.

C2 is a capacitor to improve the LPF dynamic range. When the input signal frequency exceeds $\frac{1}{2\pi C_1R_2}$, the circuit gain becomes R2/R1. If the ratio of R2 to R1 is large, pulses are likely to clip. Because control voltage VT to VCO is obtained from integrating pulses, VT is no longer a normal value after being clipped, making the lock up time longer. To avoid this condition, correct R2 in the high frequency range so as not to clip pulses. In this case, time constant ω_c should be 5 to 10 times of normal ω_n . When ω_c is too close to ω_n , the loop operation becomes unstable.

$$\omega_c=\frac{1}{C_2R_2} \qquad \omega_c=(5\sim10)\omega_n$$

Frequency at natural angle $\omega_n=\sqrt{\frac{K_\phi\cdot K_V}{\tau_1}}$

VH: Maximum output voltage of phase comparator [V]

VL: Minimum output voltage of phase comparator [V]

Gain constant of the phase comparator $K_\phi=\frac{1}{2\pi}\cdot\frac{VH-VL}{2}$ (V/rad)

VCO sensitivity $K_V=2\pi\frac{fmax-fmin}{Vmin-Vmax}$ $(rad/V\cdot s)$

$Vmin$: Voltage applied to variable capacity diode at $fmax$ [V]

$Vmax$: Voltage applied to variable capacity diode at $fmin$ [V]

The parameters are set as V_H = 5V, V_L = 0V, $fmax$ = 79.0MHz, $fmin$ = 76.0MHz, $Vmin$ = 2.0V and $Vmax$ = 1.2V.

$$K_\phi = \frac{1}{2\pi} \cdot \frac{5-0}{2} = 0.4 \ (V/rad)$$

$$K_V = 2\pi \frac{79\times10^6 - 76\times10^6}{2.0-1.2} = 23.56\times10^6 \ (rad/V\cdot s)$$

$$\omega_n = \sqrt{\frac{0.4 \cdot 23.56\times10^6}{663\times10^{-3}}} = 3770$$

$$\omega_c = (5\sim10) \cdot 3770 = 18850\sim37700$$

$$C_2 = \frac{1}{\omega_c R_2} = \frac{1}{(18850\sim37700)\cdot 100} = 0.27\sim0.53 \ (\mu F)$$

Because R2/R1 ratio is small, C2 is set to 0.047μF $(\omega_c = 56\omega_n)$

C3 and R3 are LPF to remove side band (comparison frequency). By using the active filter, noise generated from the amplifier affects the operation. To avoid this, passive filters are used in the system. In this case, time constant ωc should be more than 5 times of normal ωn. When ωc is too close to ωn, the loop operation becomes unstable.

The parameters are set as C3 = 2200pF and R3 = 3.3kΩ.

$$\omega_c = \frac{1}{C_3 R_3} = \frac{1}{2200\times10^{-12}\cdot 3300} = 137741$$

$$\omega_c = 36.5\omega_n$$

$$f_3 = \frac{1}{2\pi C_3 R_3} = \frac{1}{2\pi\cdot2200\times10^{-12}\cdot3300} = 21.9kHz$$

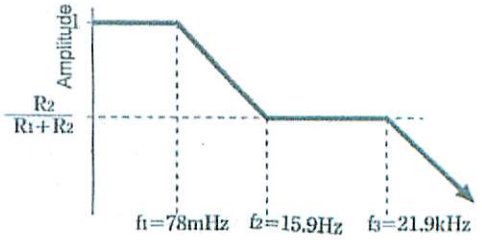

Fig. 15 PLL Filter Characteristics after Calculation

3.7 RF output (Pin 11)

In order to suppress generation of high frequency in the RF output, insert LPF or BPF between Pin 11 and the antenna. The output resistance of Pin 11 is set to 75Ω.

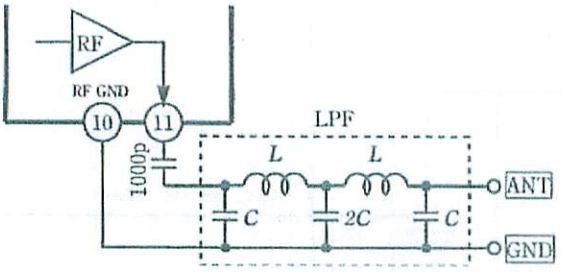

Fig. 16 The K Type LPF Circuit for RF Output

The figure at left shows the K type LPF. It is composed of 6 circuit elements. As the K type has 6dB/oct attenuation per circuit element, the total of 36dB/oct attenuation will be obtained.