RYZ012

Multi-Standard Wireless Communication Module for Bluetooth 5 Low Energy and 802.15.4

Description

The RYZ012 is a highly integrated multi-standard wireless communication module that provides a qualified solution for Bluetooth™ 5 Low Energy (LE) and several IEEE 802.15.4 based communication standards. The integrated RISC processor runs the network stack and can execute the user application.

The integrated Bluetooth 5 Low Energy chipset, a multi-standard wireless SoC solution with internal Flash and audio support, combines the features and functions needed for 2.4GHz IoT standards into a single SoC. The RYZ012 supports concurrent multi-standards, and for some use cases, the RYZ012 can concurrently run two standards. For example, stacks such as Bluetooth Low Energy and 802.15.4 can run concurrently with one application state but with dual radio communication channels that are used to interact with different devices. Working in this mode, the end product can maintain active connections to smart phones or other Bluetooth Low Energy devices while controlling and communicating with 802.15.4 or other 2.4GHz devices. In this case, the end product complies with the Bluetooth standard, supports Bluetooth Low Energy specification up to Bluetooth 5 and allows simple connectivity with Bluetooth Low Energy mobile phones, tablets and laptops. The Bluetooth Low Energy stack supports Bluetooth Low Energy slave and master mode operation, including broadcast, encryption, connection updates, and channel map updates. Combining Bluetooth Low Energy with IEEE 802.15.4 based standards such as ZigBee or Thread, creates an interoperable solution for use within the home.

The RYZ012 integrates hardware acceleration to support the complicated security operations required by HomeKit, Thread, and other standards without the requirement for an external DSP, resulting in a significant reduction in the product eBOM. The RYZ012 also supports single or dual analog microphones or a digital microphone along with stereo audio output with enhanced voice performance for voice search and similar applications. Including a full range of on-chip peripherals, the RYZ012 interfaces with external components such as LEDs, sensors, touch controllers, keyboards, external processors, and motors.

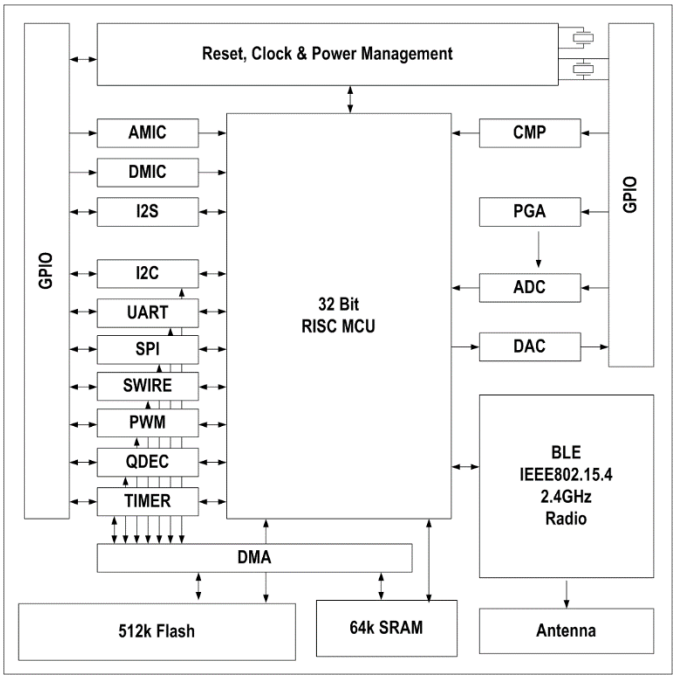
Typical Applications

- Portable devices and equipment
- Smart lighting, smart home devices
- Remote equipment
- Building automation
- Smart grid
- Intelligent logistics, transportation, and tracking
- Industrial control
- Health care

Supported Standards

- Bluetooth 5 Low Energy
- ZigBee
- 6LoWPAN / Thread
- RF4CE
- Concurrent operation

Block Diagram



General Features

- 4-byte chip UID (unique ID)
- Embedded 32-bit proprietary microcontroller
  - Better power-balanced performance than Arm® M0® core
  - Instruction cache controller
  - Maximum running speed up to 48MHz
- Program memory: internal 512kB Flash
- Data memory: 64kB on-chip SRAM, including up to 32K SRAM with retention in deep sleep, and one 32kB SRAM without retention in deep sleep
- RTC and other timers:
  - Clock source of 24MHz and 32.768kHz crystal and 32kHz/24MHz embedded RC oscillator
  - Three general 32-bit timers with four selectable modes in active mode
  - Watchdog timer
  - A low-frequency 32kHz timer available in low power mode
- A rich set of I/Os:
  - Up to 32/17 GPIOs depending on package option. All digital IOs can be used as GPIOS
  - Digital and analog microphone input
  - I2S
  - Stereo Audio output
  - SPI, I2C, and UART with hardware flow control and 7816 protocol support
  - Swire debug Interface.
- Up to 6 channels of differential PWM:
  - PWM1–PWM5: 5-channel normal PWM output.
  - PWM0: 1 channel with IR/IR FIFO/IR DMA FIFO mode for IR generation.
- Sensor:
  - 14-bit 10 channel (only GPIO input) SAR ADC, with 4 channel differential input PGA
  - Temperature sensor
- One quadrature decoder
- Embedded hardware AES and AES-CCM
- Embedded hardware acceleration for Elliptical curve cryptography (ECC) used in HomeKit, Thread, and Bluetooth 4.2 and above
- Embedded low power comparator
- Supports all 2.4GHz IoT standards into a single SoC, including Bluetooth Low Energy, Bluetooth Low Energy Mesh, ZigBee, RF4CE, HomeKit, 6LowPAN, Thread, ANT, and 2.4GHz proprietary technologies without the requirement for an external DSP

RF Features

- Bluetooth Low Energy/802.15.4/2.4GHz RF transceiver embedded, working in worldwide 2.4GHz ISM band
- Bluetooth 5 Compliant, 1Mbps, 2Mbps, Long Range 125kbps and 500kbps
- IEEE802.15.4 compliant, 250kbps
- 2.4GHz proprietary 1Mbps/2Mbps/250kbps/500kbps mode with Adaptive Frequency Hopping feature support
- ANT mode
- Rx Sensitivity: -96dBm at Bluetooth Low Energy 1Mbps, -99.5dBm at IEEE802.15.4 250kbps, -93dBm at Bluetooth Low Energy 2Mbps mode, -99dBm at Bluetooth Low Energy 500kbps mode, -101dBm at Bluetooth Low Energy 125kbps mode
- Tx output power: up to +10dBm
- Single-pin antenna interface
- RSSI monitoring with ±1dB resolution
- Auto acknowledgement, retransmission and flow control.
- Support full-function Bluetooth Low Energy location features

Power Management Features

- Embedded LDO and DCDC
- Battery monitor: supports low battery detection
- Multiple stage power management to minimize power consumption
- Low power consumption:
  - Whole Chip RX mode: 5.3mA
  - Whole Chip TX mode: 4.8mA at 0dBm with DCDC
  - Deep sleep with external wakeup (without SRAM retention): 0.4µA
  - Deep sleep with SRAM retention: 1µA (with 8kB SRAM retention), 1.2µA (with 16kB SRAM retention), 1.4µA (with 32kB SRAM retention)

Flash Features

- Total 512k bytes (4Mbits)
- Flexible architecture: 4kB per Sector, 64kB/32kB per block
- Up to 256 Bytes per programmable page
- Write protect all or portions of memory
- Sector erase (4kB)
- Block erase (32kB/64kB)
- Cycle Endurance: 100,000 program/erases
- Data Retention: typical 20-year retention
- Multi firmware encryption methods for anti-cloning protection

RF4CE Features

- Based on IEEE 802.15.4 Standard, certified RF4CE platform, with ZRC1.1/ZRC2.0 and MSO profile support
- Various transmission options including broadcast
- Provides a secured key generation mechanism
- Supports a simple pairing mechanism
- Only authorized devices are able to communicate
- Various power saving modes are supported for all device classes
- Supports AES-128bit encryption and AES-CCM (counter with the CBC-MAC) mode
- Extensible to vendor specific profiles
- Renesas extended profile with audio support for voice command-based searches
- Over the air (OTA) firmware upgrade with hardware support

ZigBee Features

- Based on IEEE 802.15.4 Standard, certified ZigBee Pro and ZigBee 3.0 platform, with ZHA/ZLL profile and ZigBee 3.0 device support
- Uses multi-hop mesh networking to eliminate single points of failure and expand the reach of networks
- Allows a low power operation with support for the Green Power feature
- Supports networks of thousands of nodes, providing a networking for the smart home or the smart city
- Uses a variety of security mechanisms, such as AES-128 encryption, device, and network keys and frame counters.
- Includes all application level functionality of ZigBee Smart Energy
- Support seamless interoperability with a wide variety of smart devices.
- Over the air (OTA) firmware upgrade with hardware support

6LowPAN and Thread Features

- Supports 6LowPAN, IPv6 and DHCPv6
- Supports UDP and DTLS
- Supports Thread v1.1 and up with Thread security and commission
- Supports networks of 250 nodes or greater

Bluetooth Low Energy Features

- Bluetooth 5 support
- Long range support with 125Kbps and 500Kbps data rate
- Bluetooth Mesh support
- Renesas proprietary Mesh support
- Bluetooth Low Energy location and up to 8-antenna indoor positioning support
- Renesas extended profile with audio support for voice command-based searches

Bluetooth Mesh Features

- Compatible with Bluetooth Mesh specification 1.0, with additional features from Renesas enhanced design
- Supports flexible mesh control such as N-to-1 and N-to-M
- Supports switch control for over 200 nodes without delay
- Supports real time status update for over 200 nodes
- Secure and safe control and scalable identification within network
- 8/16 groups can be controlled at the same time
- 128/256 nodes within mesh network
- Configurable to more or fewer hops within mesh network, single hop delay less than 15ms
- Flexible RF channel usage with both Bluetooth Low Energy advertising channels and data channels for good anti-interference performance

Concurrent Mode Feature

In concurrent mode, the chip supports multiple standard working concurrently. Typical combination is Bluetooth LE + 802.15.4 based standard (for example ZigBee, Thread, or 6LoWPAN): Bluetooth Low Energy and 802.15.4 based stacks can run concurrently with one application state based on time division technology; for example, Bluetooth Low Energy stack and Thread stack will run alternately during the divided time slots.

HomeKit Features

- Single-chip solution with hardware acceleration for all HomeKit security operations
- Apple (pre-)certified Software Development Kit reference design
- Conformant to latest HomeKit specification (HAP v2.0)
- Tested against Apple HomeKit Accessory Tester and Apple latest-version iOS HomeKit HOME application
- Support for all HAP defined services and characteristics
- Support for custom defined HAP services and characteristics
- HomeKit custom update over-the-air (OTA) profile for secure software upgrade

Contents

List of Figures

List of Tables

1. Pin Descriptions

Figure 1. Pin Assignments – Top View

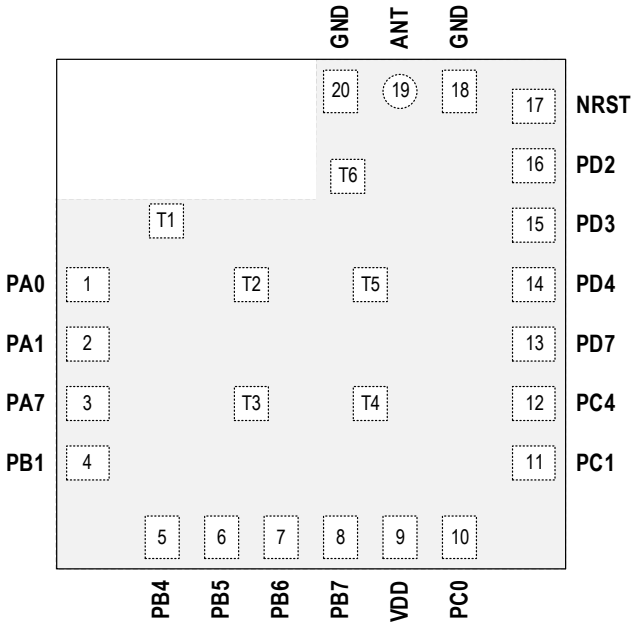


Table 1. Pin Descriptions

Pin No.	Name	Type	Driving Strength		Notes
			High	Low	
1	PA0	Digital I/O	4 mA	2 mA	UART RX
2	PA1	Digital I/O	4 mA	2 mA	Unused
3	PA7	Digital I/O	8 mA	4 mA	SWS enabled after power on
4	PB1	Digital I/O	8 mA	4 mA	UART TX
5	PB4	Digital I/O	16 mA	12 mA	Interrupt
6	PB5	Digital I/O	16 mA	12 mA	UART/SPI Select (Set low for UART, set high for SPI)
7	PB6	Digital I/O	16 mA	12 mA	SPI DI
8	PB7	Digital I/O	16 mA	12 mA	SPI DO
9	VDD	Supply	N/A		Power supply input
10	PC0	Digital I/O	4 mA	2 mA	UART RTS
11	PC1	Digital I/O	4 mA	2 mA	Unused
12	PC4	Digital I/O	4 mA	2 mA	UART CTS
13	PD7	Digital I/O	4 mA	2 mA	SPI Clock
14	PD4	Digital I/O	4 mA	2 mA	Unused
15	PD3	Digital I/O	4 mA	2 mA	Unused
16	PD2	Digital I/O	4 mA	2 mA	SPI CN
17	NRST	Reset	N/A		Reset
18	GND	Supply	N/A		Ground
19	ANT	Analog	N/A		50 Ω Antenna for RYZ012B No connection for RYZ012A
20	GND	Supply	N/A		Ground
T1 – T6	GND	Supply	N/A		Ground

2. MCU Description

The RYZ012 integrates a powerful 32-bit MCU. Due to a 16-bit instruction set, the binary code size is small, and due to a single cycle hardware multiplier, the data processing is fast. All data processing is done from internal registers.

The MCU services interrupt requests in a dedicated processing mode. The interrupt service mode has its own stack, program control and status registers, allowing for fast switching between interrupt service mode and normal mode.

2.1 Register Description

The RYZ012 incorporates a register file made of 13 general-purpose registers and eight special registers. The general-purpose registers R0 to R12 temporarily store data during code processing. Additionally, these registers pass arguments into functions and provide the return value to the caller.

The Stack Pointer register (SP) holds the current value of the call stack. It is decremented automatically when data is pushed to the stack and incremented when data is popped. As the MCU has two stacks for normal operation and interrupt servicing, the register file has two stack pointers. The stack that is active depends on the operating mode.

The Program Counter (PC) and Link Register (LR) are used to control the program flow. The PC always holds the address of the next function to be executed. The link register is used to store return addresses for function calls. When a function is called, the calling function sets the link address to the address of the instruction, which is executed immediately after returning from the call. On return from the caller, the caller sets the PC to the value of the link register.

The SPSR and CPSR registers carry execution status information.

Table 2. Register File

Normal Mode	Interrupt Mode	Address
R0		0x800680
R1		0x800684
R2		0x800688
R3		0x80068c
R4		0x800690
R5		0x800694
R6		0x800698
R7		0x80069c
R8		0x8006a0
R9		0x8006a4
R10		0x8006a8
R11		0x8006ac
R12		0x8006b0
SP_{NRM}	SP_{IRQ}	0x8006b4
LR_{NRM}	LR_{IRQ}	0x8006b8
PC		0x8006bc
CPSR		0x8006c0
$SPSR_{NRM}$	$SPSR_{IRQ}$	0x8006c4

2.2 Memory

The RYZ012 has an addressable memory space of 16 MByte. Flash memory, SRAM, and peripheral registers are mapped to this space as shown in Table 3.

Table 3. Physical Memory Map

Type	Description	Start Address	Size [Bytes]
SRAM Space	Standard SRAM	0x848000	32k
	Retention SRAM 3	0x844000	16k
	Retention SRAM 2	0x842000	8k
	Retention SRAM 1	0x840000	8k
Peripheral Space	MODEM	0x801200	
	LINK LAYER	0x800F00	256
	DMA	0x800c00	256
	DMA FIFO	0x800b00	256
	PWM	0x800780	128
	SYS_TIMER	0x800740	46
	TIMER	0x800620	224
	MCU	0x800600	32
	GPIO	0x800580	128
	AUDIO	0x800560	32
	AES	0x800540	32
	BASEBAND	0x800400	256
	I2C (address map)	0x8000E0	32
	QDEC	0x8000D0	16
	UART	0x8000B4	4
	SWIRE	0x8000B0	4
	UART	0x800090	16
	SCTL	0x800040	64
	SPI	0x800008	4
	I2C	0x800000	8
Flash Space	Flash Memory	0x000000	512k

2.2.1 Flash Memory

The flash memory serves as non-volatile storage for the application code and data. The flash memory is partitioned into blocks, sectors and pages as shown in Table 4. The flash interface supports device, sector, block, and double block erase operations. Write operations are supported page-wise.

Table 4. Flash Memory Partition

Partition	No of contained ...			
	...Bytes	...Pages	...Sectors	...Blocks
Device	512k	2k	128	16
Block	32k	128	8	1
Sector	4k	16	1	-
Page	256	1	-	-

For chip identification and traceability, the Flash is preloaded with a Unique ID (UID). The user is not allowed to modify this preloaded UID, but the user can read the UID through the corresponding API interface. The MCU uses the system frequency to load instructions, and it adopts the flash driver to access (read/write) flash with the speed of half of the system clock.

2.2.1.1 E-Fuse

As shown in Table 5, the non-volatile E-Fuse section is preloaded with a 4-byte decryption key and a 4-byte chip UID.

Table 5. E-Fuse Information

Decryption Key	Chip UID			
	Internal Information	Wafer Number	Lot Number.	Internal Information
Bit0–31	Bit32–47	Bit48–52	Bit53–55	Bit56–63

2.2.1.2 Readout Protection

The RYZ012 supports multiple firmware encryption methods to achieve anti-cloning protection including: UID-based authentication and Bootloader-based firmware encryption.

2.2.1.2.1 UID-based Authentication Code Generation

During firmware burning (such as through specific burning jig), the user can encrypt the UID read from the chip flash through AES, generating a unique cipher text that is written into the E-Fuse section.

During application startup, an encryption authentication procedure is added. The user should use the same key and AES encryption algorithm and key to encrypt the UID read from the chip flash and generate new cipher text. Before running the main application firmware, the new cipher text is compared with the cipher text read from the E-Fuse section. When the authentication passes (that is the comparison result matches), the main firmware is up and running; otherwise, the chip stops before running the main firmware.

2.2.1.2.2 Bootloader-based Firmware Encryption/Decryption

The firmware can be encrypted using a customer-provided security key. The customer security key is written into a specific secure register and becomes unreadable. Any attempt to read the key results in either all 1's or all 0's.

The encrypted firmware can be generated based on the plaintext firmware and the customer security key. The customer can burn both, the security key into the obscured memory area and the encrypted firmware into Flash.

The firmware is readable by all, but it does appear as unreadable binaries to a third party.

2.2.2 SRAM Memory

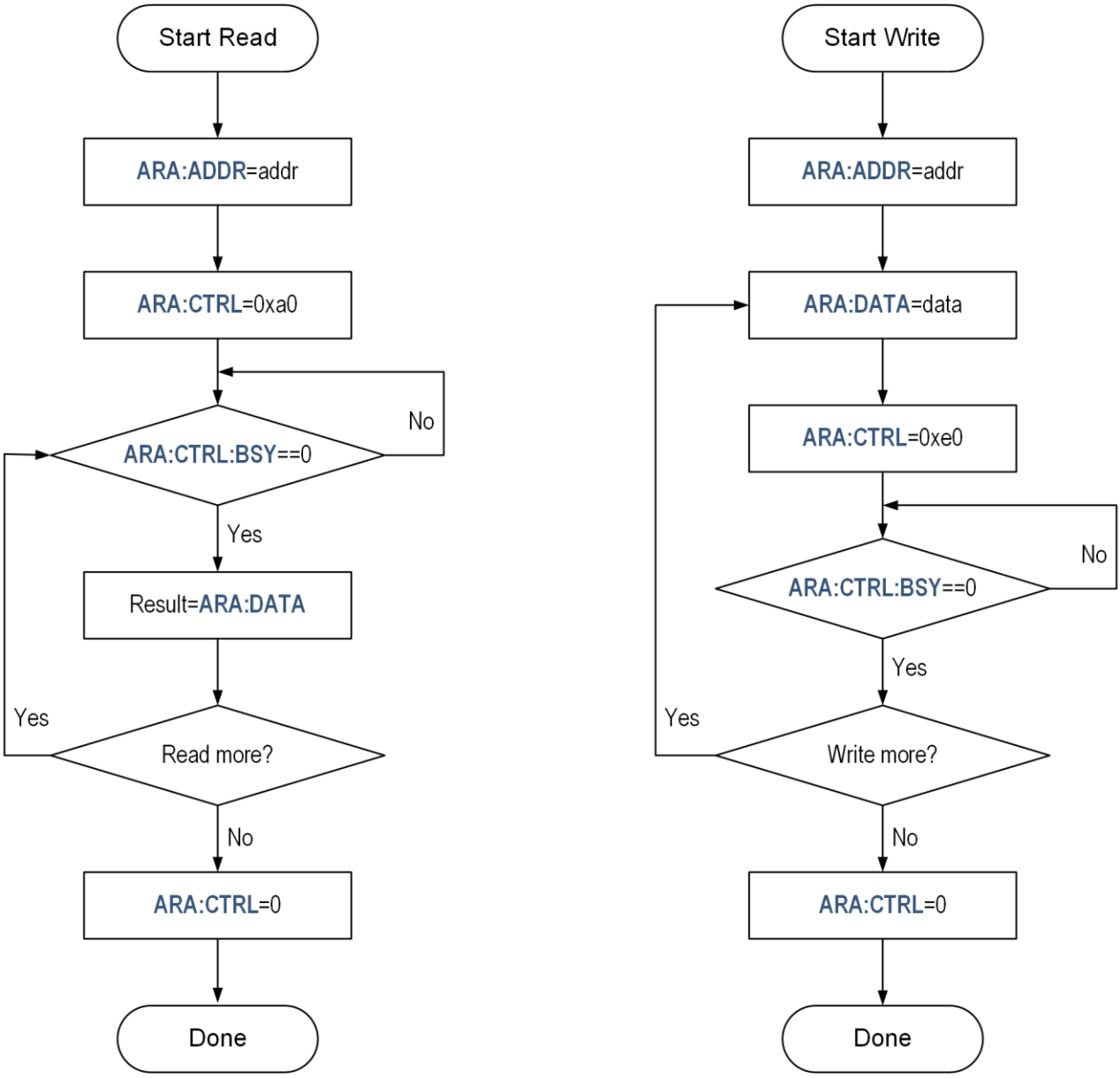
The SRAM is split into 4 independent blocks. The lower three blocks can be configured as a retention area that allows data to remain valid in Deep Sleep mode. The contents of the standard SRAM block are lost in Deep Sleep mode.

2.2.3 Peripheral Registers

In the digital domain, peripheral control registers are memory mapped, starting from address 0x800000. Similar to the SRAM, they are accessed by reading and writing the corresponding address. For convenience the SDK defines usable mnemonics.

Peripheral registers in the analog domain are not directly accessible. These registers need to be accessed indirectly through **ARA:CTRL**, **ARA:ADDR** and **ARA:DATA**. The figure below shows the register read and write procedures.

Figure 2. Reading and Writing Analog Registers



2.3 Register Reference

2.3.1 ARA:ADDR - Analog Register Address

Address: 0x00b8
Reset: 0x00

	7	6	5	4	3	2	1	0
ARA:ADDR	ADDR							
	rw, 0							

7:0 **ADDR** Address of the analog register to be accessed

2.3.2 ARA:DATA - Analog Register Data

Address: 0x00b9
Reset: 0x00

	7	6	5	4	3	2	1	0
ARA:DATA	DATA							
	rw, 0							

7:0 **DATA** Input/Output data

2.3.3 ARA:CTRL - Access Control

Address: 0x00ba
Reset: 0x00

	7	6	5	4	3	2	1	0
ARA:CTRL	RSVD	CYC	RDWR	CONT	RSVD			BSY
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0			r, 0

6 **CYC** ToDo

5 **RDWR** Read/write control

0: Read register

1: Write register

4 **CONT** Continuous access (read mode)

0: Single read operation

1: Automatically start new read cycle

0 **BSY** Analog register interface busy indicator

0: Analog register interface idle / last request completed

1: Analog register interface busy

3. System Control

3.1 Reset

The module supports different reset types, each with a different scope:

- Power-on-Reset - On power-on the whole chip is reset; consequently, all registers are set to their default values.
- Watchdog Reset - The RYZ012 includes a programmable watchdog timer to monitor software execution. If the watchdog is triggered, all the registers reset except for the retention analog registers **SCTL:RD5** to **SCTL:RD7**.
- Software Reset - The Peripheral Reset Register **SCTL:PRR** can be used to reset individual peripheral units. Peripheral reset causes all registers of the corresponding peripheral to be reset. The software can also trigger a system reset by setting bit **SCTL:LPRC:SRST** to 1. The behavior of the system reset is similar to the Watchdog Reset behavior.

3.2 Power Supply

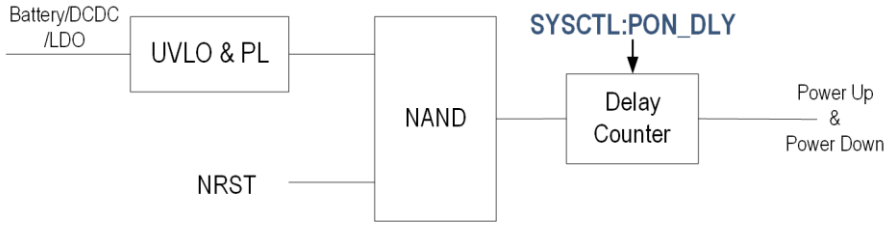
The device must be powered with an operating voltage between 1.8V and 3.6V. Internal DC/DC and LDO converters generate the internal supply voltages required for operation. The chip embedded DCDC generates 1.8V output voltage as power supply for the internal flash and generates 1.4V output voltage as input to the LDO.

The embedded LDO regulator takes the 1.4V voltage output from the DCDC, and generates 1.2V regulated voltage to supply power for 1.2V digital core and analog modules.

3.2.1 Power-On-Reset (POR) and Brown-out Detect

The modules power supply status is controlled by the UVLO (Ultra-low Voltage Lockout), PL (Power Logic) module and the external NRST pin through the logic shown in the figure below. UVLO takes the external power supply as input and releases the lock only when the power supply voltage is higher than a predefined threshold. Typical values for these thresholds are shown in Table 6. The NRST pin has an internal pull-up resistor; an external Cap can be connected on the NRST pin to control the POR delay.

Figure 3. Power Control Logic



After both UVLO and NRST release, there is a further configurable delay before the system reset signal (Sysrst) is released. The delay is adjusted by analog register **SCTL:PON_DLY**. As this register is reset by power cycle, watchdog reset and software reset, the delay change is only applicable when the module has not gone through one of these reset conditions, for example, after deep sleep wakeup.

Figure 4. Power-Up Sequence

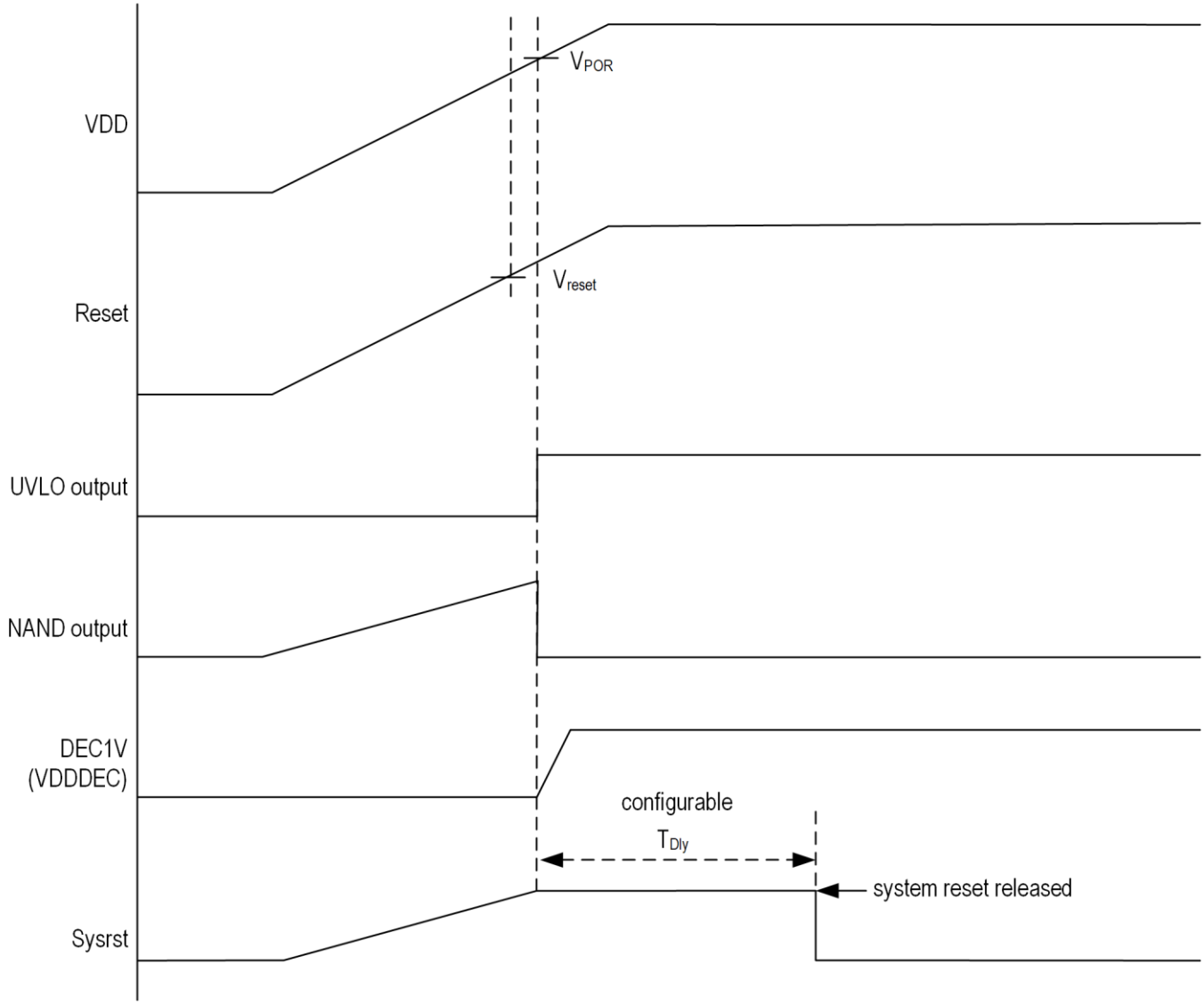


Figure 5. Power Down Sequence

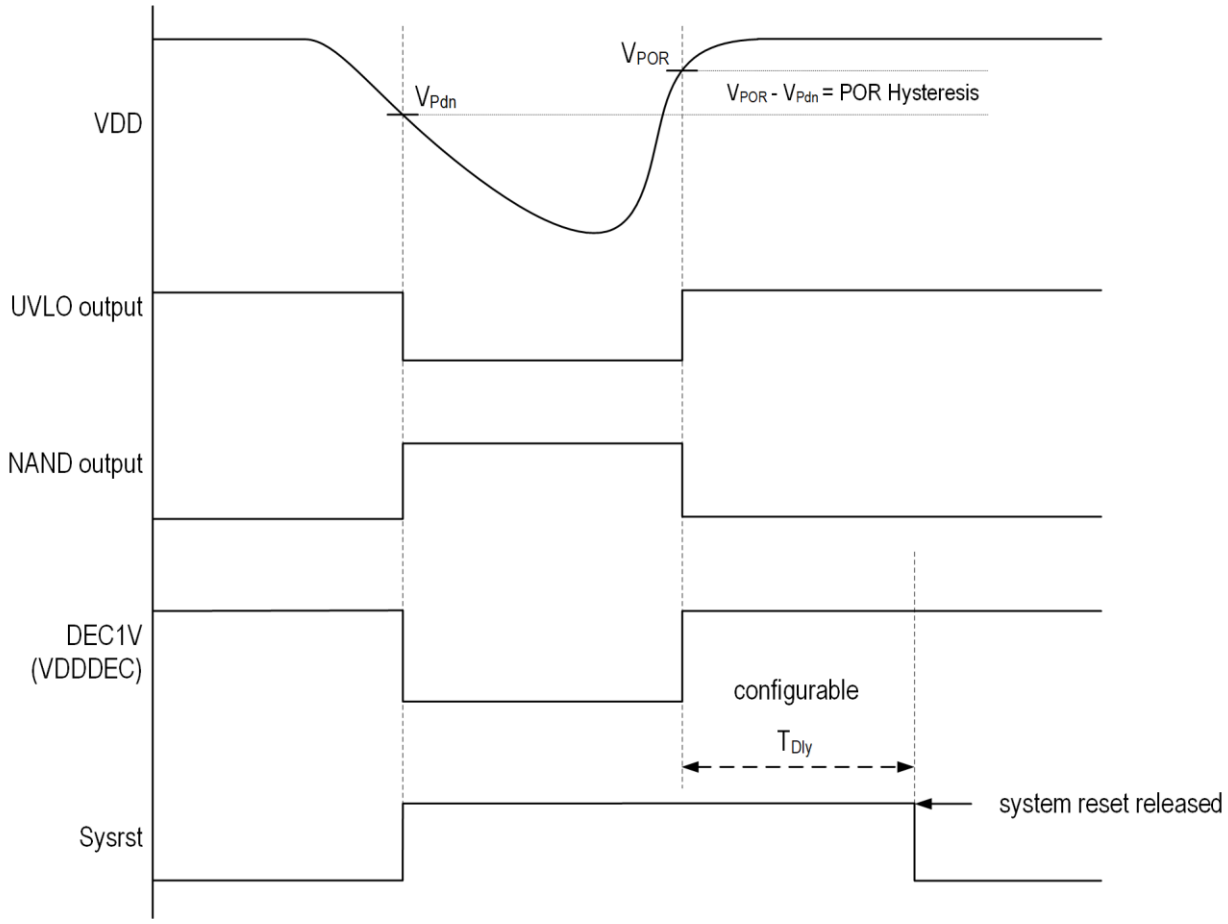


Table 6. Characteristics of the Power Control Logic

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{POR}	VDD voltage when VUVLO turns to high level		1.62		V
V_{PDN}	VDD voltage when VUVLO turns to low level		1.55		V
T_{DLY}	Delay counter value	Configurable through register **SCTL:PON_DLY**			16kHz clock cycles

3.3 Power Management

The RYZ012 provides six different power modes. Depending on the active power mode, different functional units are active or powered down. The Power Management module is always active and allows for flexible power control of individual peripheral units or the whole chip. Table 7 outlines the features and properties of the different power modes.

Table 7. Power Saving Modes Overview

Mode	Active	Idle	Suspend	Deep Sleep	Standby	Shutdown
Submodule Availability						
MCU	active	stalled	stalled	off	off	off
Retention SRAM	on	on	on	on	off	off
Standard SRAM	on	on	on	off	off	off
Radio	available	available	off	off	off	off
Audio	available	available	off	off	off	off
Wakeup Sources						
Reset pin	—	available	available	available	available	available
32K Timer	—	—	available	available	available	—
IO Pin	—	through interrupt	available	available	available	—
Low Power Comparator	—	—	available	available	available	—
Interrupt	—	available	—	—	—	—
Parameters						
Wakeup time to Active mode	—	0µs	100µs	Shorter than Standby, almost same as Suspend	1ms	10ms
Current	Table 23, DC Electrical Characteristics					

3.3.1 Active Mode

In Active mode, MCU is active, all SRAMs are accessible, and other modules are selectable whether to be at working state.

3.3.2 Idle Mode

The chip can switch to Idle mode to stall the MCU. In this mode, all SRAMs are still accessible, modules such as RF transceiver and Audio continue working if they had been enabled before. The chip can be triggered to Active mode by interrupt or NRST pin, and the time to switch to Active mode is negligible. To decrease power consumption to different levels, the chip can switch to power saving mode (Suspend, Deep Sleep, Standby, Shutdown) correspondingly (see Table 7).

3.3.3 Suspend Mode

In Suspend mode, MCU stalls, all SRAMs are still accessible, the PM module is active, modules such as RF transceiver and Audio are powered down. The chip can be triggered to Active mode by 32K Timer, IO pin, or NRST pin. It takes 100µs or so to switch from Suspend mode to Active mode.

3.3.4 Deep Sleep Mode

In Deep Sleep, the PM module is active, analog and digital modules (except for the two 8kB and one 16kB retention SRAMs) are powered down, while the retention SRAMs can be retained but not accessible. The chip can be triggered to Active mode by 32K Timer, IO pin or NRST pin. The time to switch to Active mode is shorter than Standby and close to Suspend.

3.3.5 Standby Mode

In Standby, only the PM module is active, while analog and digital modules including the retention SRAMs are powered down. The chip can be triggered to Active mode by 32K Timer, IO pin or NRST pin. The time to switch to Active mode is 1ms or so.

3.3.6 Shutdown Mode

In Shutdown mode, all digital and analog modules are powered down, and the PM module is active. The chip can be triggered to Active mode by the NRST pin. The time to switch to Active mode is estimated at 10ms.

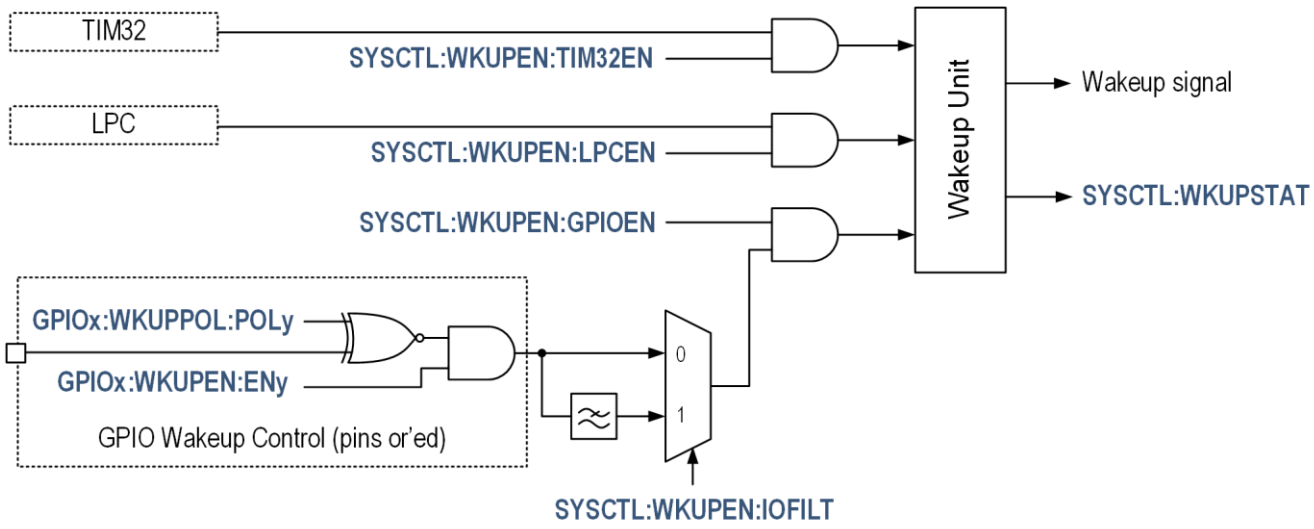
3.3.7 Wakeup Sources

The wakeup sources available to return to active mode differ for the individual low power modes. An overview of the available wakeup sources is given in Table 7.
Wakeup from idle mode is possible by interrupt from one of the active peripheral units or by reset, which is triggered by the NRST pin. GPIO wakeup can be supported if the GPIO interrupt functionality is used.

Wakeup from Suspend, Deep Sleep, and Standby mode is done through a wakeup logic as illustrated below. GPIO wakeup, 32kHz Timer, and Low Power Comparator wakeup can be enabled individually through bits in register **SCTL:WKUPEN**. After wakeup, the lower four bits of register **SCTL:SSTATUS** determine the source that triggered wakeup.

Each individual GPIO pin can be configured as wakeup pin through **GPIOx:WKUPEN**. The polarity of the wakeup signal is controlled **GPIOx:WKUPPOL**. GPIO wakeup provides an optional glitch filter, controlled through bit **SCTL:WKUPEN:IOFILT**.

Figure 6. Wakeup Logic



Wakeup from Shutdown Mode is only supported through NRST.

3.3.8 Retention Registers

The RYZ012 provides eight registers **SCTL:RD0** to **SCTL:RD7** which contents that are retained during all low-power modes except Shutdown Mode. Registers **SCTL:RD0** to **SCTL:RD4** are reset by System Reset, Watchdog Reset, and Power-On reset. Registers **SCTL:RD5** to **SCTL:RD7** are reset by Power-On Reset only.

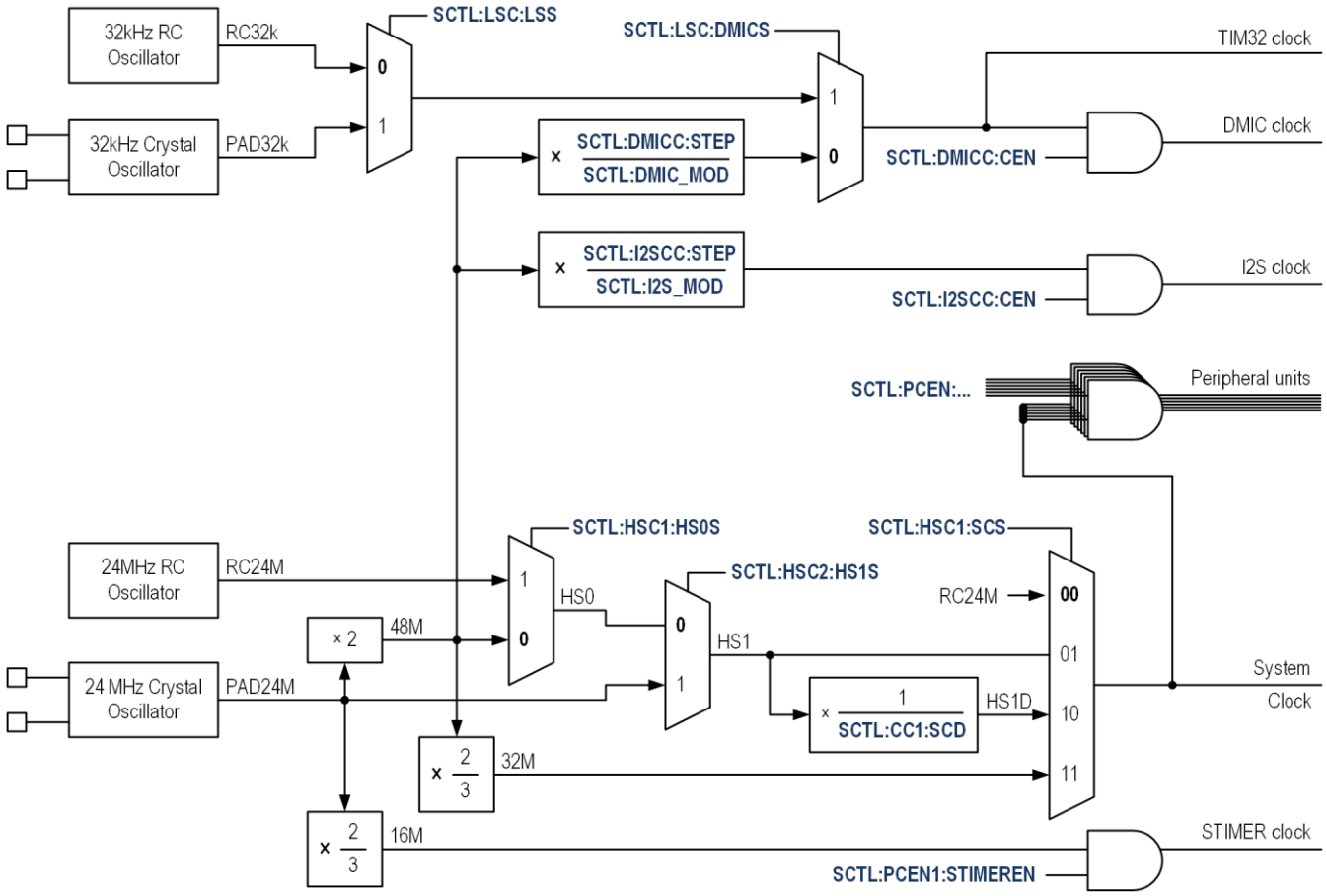
3.4 Clock

The MCU of the RYZ012 provides low and high-speed clocks with versatile configuration options to optimize the power consumption and system performance. The CPU clock and most of the peripheral clocks are derived from a 24 MHz high speed clock. The low speed clock is used to drive the digital microphone peripheral and the low power timer (LP_TIMER), which can be kept running in suspend and deep sleep modes. The MCU integrates RC oscillators for both of these clocks and provides the option to connect an external crystal oscillator for higher precision clocks.

After power on the internal oscillators are selected as clock sources. The application firmware can change this to a suitable configuration. The figure below gives an overview of the clock tree and shows the registers that are required to change the configuration of the clock tree.

Most peripheral clocks are gated through register **SCTL:PCEN** by default. The application firmware must enable the clocks of the peripheral units that are used by the application.

Figure 7. Clock Tree



3.4.1 System Clock

The system clock is selected from one of four possible sources. This can be either the 24 MHz RC clock, the internal clock HS1, HS1D that is HS1 divided by **SCTL:HSC1:SCD** or a fixed frequency 32 MHz clock derived from the high speed crystal oscillator. System clock selection is done through **SCTL:HSC1:SCS**.

Caution: For the HS1 clock divider, it must be ensured that **SCTL:HSC1:SCD** is never set to 0 or 1. The output frequency of the HS1 clock divider clock is $F_{HS1D} = F_{HS1} /$**SCTL:HSC1:SCD**. The only way to select the maximum clock of 48 MHz is by setting both, **SCTL:HSC1:HS0S** and **SCTL:HSC2:HS1S** to 1b'0 and **SCTL:HSC1:SCS** to 2b'01.

3.4.2 Peripheral Clocks

Register **SCTL:PCEN** is used to enable or disable clock for individual peripherals. It is strongly recommended to disable the clocks for all unused modules to keep the current consumption at a minimum.

3.4.2.1 System Timer Clock

System Timer clock is derived directly from 24M crystal oscillator with a 2/3 frequency divider. The clock frequency is fixed as 16MHz. The system timer may be used to verify the correct function of the PAD24M clock, before the System Clock is switched to a clock derived from clock PAD24M.

3.4.2.2 I2S Clock

I2S clock is derived from 48M clock through a frequency divider. The 48M clock is derived from 24M crystal oscillator through a frequency doubler.

The frequency of the I2S Clock is 48MHz * **SCTL:I2SCC:STEP** / **SCTL:I2S_MOD**. The I2S output is enabled by setting **SCTL:I2SCC:CEN** to 1b'1. **SCTL:I2S_MOD** must not be less than 2***SCTL:I2SCC:STEP**.

3.4.2.3 DMIC Clock

Bit **SCTL:DMICC:CEN** enables the DMIC clock output. For normal DMIC operation **SCTL:LSC:DMICS** should be set to 0b1, to select the clock derived from the 48MHz clock. The clock speed is configured as F_{DMIC} = 48MHz * **SCTL:DMICC:STEP** / **SCTL:DMIC_MOD**. **SCTL:DMIC_MOD** must not be less than 2 * **SCTL:DMICC:STEP**.

If the DMIC Clock is not required, but a clock for the 32kHz timer is required, **SCTL:LSC:DMICS** should be set to 0b0 and the required 32kHz oscillator should be selected through **SCTL:LSC:LSS**. A value of 0b0 selects the 32kHz RC oscillator. A value of 0b1 selects the external crystal as clock source.

3.5 Register Reference

3.5.1 SCTL:PRR - Peripheral Reset Register

This register is used to reset peripheral modules triggered by software. If the corresponding bit is set to 1, the peripheral is in reset state, otherwise its working normally.

Address: 0x0060

Reset: 0xc7ff7c

	7	6	5	4	3	2	1	0
SCTL:PRR[2]	MCIC1	RISC1	MCIC	RISC	RSVD	DFIFO	AUDIO	AIF
	r, 1	r, 1	rw, 0	rw, 0	rw, 0	rw, 1	rw, 1	rw, 1
SCTL:PRR[1]	RSVD	ALG	ADC	AES	ALGM	DMA	SYSTIM	BB
	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1
SCTL:PRR[0]	SWIRE	RSVD	QDEC	PWM	RSVD	UART	I2C	SPI
	rw, 0	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1	rw, 0	rw, 0

23 **MCIC1** MCIC reset

0: Module operating normally

1: Module is held in reset state

22	**RISC1**	RISC reset **0:** Module operating normally **1:** Module is held in reset state
21	**MCIC**	MCIC reset **0:** Module operating normally **1:** Module is held in reset state
20	**RISC**	RISC reset **0:** Module operating normally **1:** Module is held in reset state
18	**DFIFO**	DFIFO reset **0:** Module operating normally **1:** Module is held in reset state
17	**AUDIO**	Audio Reset **0:** Module operating normally **1:** Module is held in reset state
16	**AIF**	AIF reset **0:** Module operating normally **1:** Module is held in reset state
14	**ALG**	ALG reset **0:** Module operating normally **1:** Module is held in reset state
13	**ADC**	ADC reset **0:** Module operating normally **1:** Module is held in reset state
12	**AES**	AES reset **0:** Module operating normally **1:** Module is held in reset state
11	**ALGM**	ALGM reset **0:** Module operating normally **1:** Module is held in reset state
10	**DMA**	DMA reset **0:** Module operating normally **1:** Module is held in reset state
9	**SYSTIM**	System timer reset **0:** Module operating normally **1:** Module is held in reset state

8 **BB** Baseband module

0: Module operating normally

1: Module is held in reset state

7 **SWIRE** SWIRE reset

0: Module operating normally

1: Module is held in reset state

5 **QDEC** QDEC reset

0: Module operating normally

1: Module is held in reset state

4 **PWM** PWM reset

0: Module operating normally

1: Module is held in reset state

2 **UART** UART reset

0: Module operating normally

1: Module is held in reset state

1 **I2C** I2C reset

0: Module operating normally

1: Module is held in reset state

0 **SPI** SPI reset

0: Module operating normally

1: Module is held in reset state

3.5.2 SCTL:PCEN - Peripheral Clock Enable 1

Address: 0x0063
Reset: 0x300083

	7	6	5	4	3	2	1	0
SCTL:PCEN[2]	RSVD		MCICEN	RISCEN	DMAEN	DFIFOEN	AUDIOEN	AIFEN
	rw, 0		rw, 1	rw, 1	rw, 0	rw, 0	rw, 0	rw, 0
SCTL:PCEN[1]	RSVD			AESEN	ALGMEN	RSVD	SYSTIMEN	BBEN
	rw, 0			rw, 0	rw, 0	rw, 0	rw, 0	rw, 0
SCTL:PCEN[0]	SWIREEN	RSVD	QDECEN	PWMEN	RSVD	UARTEN	I2CEN	SPIEN
	rw, 1	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 1	rw, 1

21 **MCICEN** MCIC clock enable control

0: Disables module clock

1: Enables module clock

20	**RISCEN**	MC clock enable control **0:** Disables module clock **1:** Enables module clock
19	**DMAEN**	DMA clock enable control **0:** Disables module clock **1:** Enables module clock
18	**DFIFOEN**	DFIFO clock enable control **0:** Disables module clock **1:** Enables module clock
17	**AUDIOEN**	Audio clock enable control **0:** Disables module clock **1:** Enables module clock
16	**AIFEN**	AIF clock enable control **0:** Disables module clock **1:** Enables module clock
12	**AESEN**	AES clock enable control **0:** Disables module clock **1:** Enables module clock
11	**ALGMEN**	ALGM clock enable control **0:** Disables module clock **1:** Enables module clock
9	**SYSTIMEN**	System Timer clock enable control **0:** Disables module clock **1:** Enables module clock
8	**BBEN**	BB clock enable control **0:** Disables module clock **1:** Enables module clock
7	**SWIREEN**	SWIRE clock enable control **0:** Disables module clock **1:** Enables module clock
5	**QDECEN**	QDEC clock enable control **0:** Disables module clock **1:** Enables module clock
4	**PWMEN**	PWM clock enable control **0:** Disables module clock **1:** Enables module clock

2	**UARTEN**	UART (RS232) clock enable control **0:** Disables module clock **1:** Enables module clock
1	**I2CEN**	I2C clock enable control **0:** Disables module clock **1:** Enables module clock
0	**SPIEN**	SPI clock enable control **0:** Disables module clock **1:** Enables module clock

3.5.3 SCTL:HSC1 - System Clock Configuration

Address: 0x0066
Reset: 0x06

	7	6	5	4	3	2	1	0
SCTL:HSC1	HS0S	SCS		SCD				
	rw, 0	rw, 0		rw, 6				

7	**HS0S**	HS0 clock selection **0:** Selects 48M clock **1:** Selects RC24 clock
6:5	**SCS**	System clock selection **00:** RC24 clock selected as System Clock source **01:** HS1 clock selected as System Clock source **10:** HS1/SCS selected as System Clock source **11:** 32M clock selected as System Clock source
4:0	**SCD**	System Clock divider (must exceed 1). If SCS is set as 2b'10, F_{SYS} = F<HS1> / SCD.

3.5.4 SCTL:I2SCC - I2S Clock Control

Address: 0x0067
Reset: 0x00

	7	6	5	4	3	2	1	0
SCTL:I2SCC	CEN				STEP			
	rw, 0				rw, 0			

7 **CEN** Enable I2S clock

0: Disables I2S clock

1: Enables I2S clock

6:0 **STEP** I2S step

3.5.5 SCTL:I2S_MOD - I2S Clock Modifier

Address: 0x0068
Reset: 0x02

	7	6	5	4	3	2	1	0
SCTL:I2S_MOD	I2S_MOD							
	rw, 2							

7:0 **I2S_MOD** F_{I2S} = 48M * I2SCC:STEP / I2S_MOD

I2S_MOD should be larger than or equal to 2 * I2SCC:STEP

3.5.6 SCTL:DMICC - DCMI Clock Control

Address: 0x006c
Reset: 0x01

	7	6	5	4	3	2	1	0
SCTL:DMICC	CEN				STEP			
	rw, 0				rw, 1			

7 **CEN** Enable Digital MIC clock

0: Disables DMIC clock

1: Enables DMIC clock

6:0 **STEP** DMIC step

3.5.7 SCTL:DMIC_MOD - DCMI Clock Modifier

Address: 0x006d
Reset: 0x02

	7	6	5	4	3	2	1	0
SCTL:DMIC_MOD	DMIC_MOD							
	rw, 2							

7:0 **DMIC_MOD** F_{DMIC} = 48MHz * DMICC:STEP / DMIC_MOD

DMIC_MOD should be larger than or equal to 2 * DMICC:STEP

3.5.8 SCTL:WAKEUPEN - Wakeup Enable Digital Module Control

Address: 0x006e
Reset: 0x1f

	7	6	5	4	3	2	1	0
SCTL:WAKEUPEN	SLEEPEN	RSVD	RGPIOEN	I2CSYNEN	GPIOEN	RSVD	SPIEN	I2CEN
	rw, 0	rw, 0	rw, 0	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1

7 **SLEEPEN** Enable sleep wakeup/resume reset system

0: Disables sleep wakeup

1: Enables sleep wakeup

5 **RGPIOEN** Enable GPIO remote wakeup/resume

0: Disables remote GPIO wakeup

1: Enables remote GPIO wakeup

4 **I2CSYNEN** Enable I2C synchronous interface wakeup

0: Disables wakeup from I2C synchronous interface

1: Enables wakeup from I2C synchronous interface

3 **GPIOEN** Enable GPIO wakeup

0: Disables wakeup from GPIO

1: Enables wakeup from GPIO

1 **SPIEN** Enable SPI host wakeup

0: Disables wakeup from SPI host

1: Enables wakeup from SPI host

0 **I2CEN** Enable I2C host wakeup

0: Disables wakeup from I2C host

1: Enables wakeup from I2C host

3.5.9 SCTL:LPRC - Low-Power and Reset Control

Address: 0x006f
Reset: 0x00

	7	6	5	4	3	2	1	0
SCTL:LPRC	SUSPTRIG	RSVD	SRST	RSVD				SUSP
	w, 0	rw, 0	rw, 0	rw, 0				rw, 0

7 **SUSPTRIG** Suspend trigger

0: No action

1: Trigger low power mode entry

If bit SUSP is set, system will enter Suspend Mode

If bit SUSP is cleared, the MCU will be stalled

5 **SRST** Reset all (act as watchdog reset)

0: No action

1: Resets the whole chip (similar to watchdog reset)

0 **SUSP** Suspend Mode control

0: Disables suspend mode

1: Enables suspend mode

3.5.10 SCTL:HSC2 - HS1 Clock Configuration

Address: 0x0070
Reset: 0x00

	7	6	5	4	3	2	1	0
SCTL:HSC2	RSVD							HS1S
	rw, 0							rw, 0

0 **HS1S** HS1 clock selection

0: Select HS0 clock for HS1

1: Select PAD24 clock for HS1

3.5.11 SCTL:WDSTATE - Watchdog Status

Address: 0x0072
Reset: 0x00

7	6	5	4	3	2	1	0
SCTL:WDSTATE	RSVD						STATE
	rw, 0						rw, 0

0 **STATE** Watch dog status indication

0: No Watchdog indication detected

1: Watchdog indication detected

Write 1 to clear.

3.5.12 SCTL:LSC - Oscillator Clock Configuration

Address: 0x0073
Reset: 0x04

7	6	5	4	3	2	1	0
SCTL:LSC	RSVD					DMICS	LSS
	rw, 1					w, 0	rw, 0

1 **DMICS** DMIC clock select

0: Select DMIC clock divider

1: Select 32kHz oscillator

0 **LSS** Low speed clock select

0: Select RC_32k from RC oscillator

1: Select PAD_32k from 32K crystal oscillator

3.6 Analog Register Reference

3.6.1 SCTL:PDC0 - Power Down Control

Address: 0x0005
Reset: 0x02

	7	6	5	4	3	2	1	0
SCTL:PDC0	BBPLDOPD	BUSLDOPD	DCDCPD	PLPD	X24MPD	RC24MPD	X32KPD	RC32KPD
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 1	rw, 0

7 **BBPLDOPD** Power control baseband PLL LDO

0: Power-up module

1: Power-down module

6 **BUSLDOPD** Power control of VBUS_LDO

0: Power-up module

1: Power-down module

5 **DCDCPD** Power control of DCDC

0: Power-up module

1: Power-down module

4 **PLPD** Power control of power logic, 4.2V VBUS_LDO and DCDC

0: Power-up module

1: Power-down module

3 **X24MPD** Power control of 24MHz crystal oscillator

0: Power-up module

1: Power-down module

2 **RC24MPD** Power control of 24MHz RC oscillator

0: Power-up module

1: Power-down module

1 **X32KPD** Power control 32kHz crystal

0: Power-up module

1: Power-down module

0 **RC32KPD** Power control 32kHz RC oscillator

0: Power-up module

1: Power-down module

3.6.2 SCTL:PDC1 - Power Down Control

Address: 0x0007
Reset: 0x1d

	7	6	5	4	3	2	1	0
SCTL:PDC1	RSVD			TSPD	LPCPD	RDPD	DLDOPD	SPDLDO
	rw, 0			rw, 1	rw, 1	rw, 1	rw, 0	rw, 1

4 **TSPD** Power control of temperature sensor
0: Power-up module
1: Power-down module

3 **LPCPD** Power control of LPC
0: Power-up module
1: Power-down module

2 **RDPD** Power control of retention LDO
0: Power-up module
1: Power-down module

1 **DLDOPD** Power control of main digital LDO
0: Power-up module
1: Power-down module

0 **SPDLDO** Power control of SPD LDO
0: Power-up module
1: Power-down module

3.6.3 SCTL:PON_DLY - Power on delay

Address: 0x001f
Reset: 0x40

	7	6	5	4	3	2	1	0
SCTL:PON_DLY	PON_DLY							
	rw, 64							

7:0 **PON_DLY** DCDC converter ready wait count (16kHz count)

3.6.4 SCTL:WKUPEN - Wakeup Enable Module Control

Address: 0x0026
Reset: 0x00

	7	6	5	4	3	2	1	0
SCTL:WKUPEN	LPCEN	TIM32EN	RSVD	GPIOEN	IOFILT	RSVD		
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0		

7 **LPCEN** LPC wakeup control

0: Disables module as wakeup source

1: Enables module as wakeup source

6 **TIM32EN** 32kHz timer wakeup control

0: Disables module as wakeup source

1: Enables module as wakeup source

4 **GPIOEN** GPIO wake up control

0: Disables module as wakeup source

1: Enables module as wakeup source

3 **IOFILT** GPIO wakeup filter control

0: Combinational logic output (disable filter)

1: Select 16µs filter to filter out jitter on IO PAD input.

3.6.5 SCTL:RD0 - Retention Data 0

Address: 0x0035
Reset: 0x20

	7	6	5	4	3	2	1	0
SCTL:RD0	RD0							
	rw, 32							

7:0 **RD0** Application data buffer

3.6.6 SCTL:RD1 - Retention Data 1

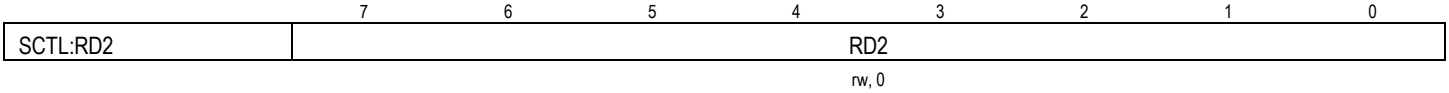
Address: 0x0036
Reset: 0x00

	7	6	5	4	3	2	1	0
SCTL:RD1	RD1							
	rw, 0							

7:0 **RD1** Application data buffer

3.6.7 SCTL:RD2 - Retention Data 2

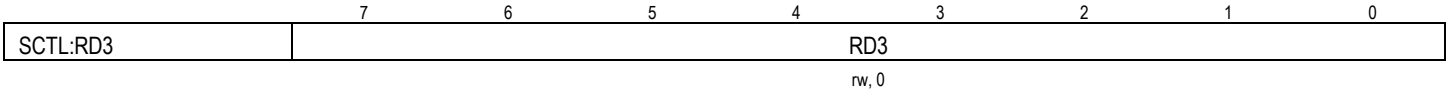
Address: 0x0037
Reset: 0x00



7:0 **RD2** Application data buffer

3.6.8 SCTL:RD3 - Retention Data 3

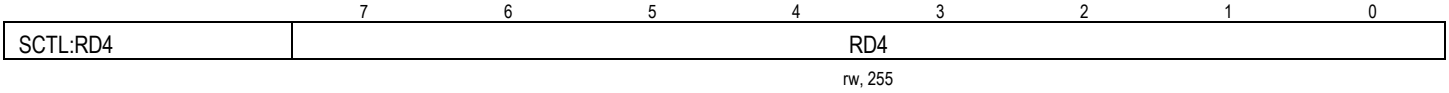
Address: 0x0038
Reset: 0x00



7:0 **RD3** Application data buffer

3.6.9 SCTL:RD4 - Retention Data 4

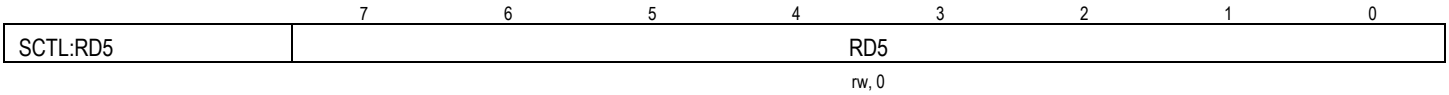
Address: 0x0039
Reset: 0xff



7:0 **RD4** Application data buffer

3.6.10 SCTL:RD5 - Retention Data 5

Address: 0x003a
Reset: 0x00



7:0 **RD5** Application data buffer

Note: This field is only reset by power on reset. Data is retained after Watchdog or System Reset.

3.6.11 SCTL:RD6 - Retention Data 6

Address: 0x003b
Reset: 0x00

	7	6	5	4	3	2	1	0
SCTL:RD6	RD6							
	rw, 0							

7:0 **RD6** Application data buffer

Note: This field is only reset by power on reset. Data is retained after Watchdog or System Reset.

3.6.12 SCTL:RD7 - Retention Data 7

Address: 0x003c
Reset: 0x00

	7	6	5	4	3	2	1	0
SCTL:RD7	RD7							
	rw, 0							

7:0 **RD7** Application data buffer

Note: This field is only reset by power on reset. Data is retained after Watchdog or System Reset.

3.6.13 SCTL:SSTATUS - System Status

Address: 0x0044
Reset: 0x00

	7	6	5	4	3	2	1	0
SCTL:SSTATUS	DCDC_RDY	WD_STATE	CAL_24M	CAL_32K	IO_WKUP	RSVD	T32_WKUP	LPC_WKUP
	r, 0	rw1c, 0	r, 0	r, 0	rw1c, 0	r, 0	rw1c, 0	rw1c, 0

7 **DCDC_RDY** DCDC converter status

0: DCDC is NOT ready

1: DCDC is ready

6 **WD_STATE** Watch dog status

Write 1 to clear.

0: Watchdog was not triggered

1: Watchdog was triggered

5 **CAL_24M** 24MHz clock calibration status

0: 24MHz clock is not calibrated

1: 24MHz clock is calibrated

4	**CAL_32K**	32kHz clock calibration status **0:** 32kHz clock is not calibrated **1:** 32kHz clock is calibrated
3	**IO_WKUP**	Set to 1 if last wakeup event was triggered from GPIO Write 1 to clear.
1	**T32_WKUP**	Set to 1 if last wakeup event was triggered from 32kHz timer Write 1 to clear.
0	**LPC_WKUP**	Set to 1 if last wakeup event was triggered from LPC Write 1 to clear.

3.6.14 SCTL:APCTRL - Analog Power Control

Address: 0x00fc
Reset: 0xE0

	7	6	5	4	3	2	1	0
SCTL:APCTRL	PGAR	PGAL	ADC	RSVD				
	rw, 1	rw, 1	rw, 1	rw, 0				

7	**PGAR**	PGA right channel power control (low active) **0:** Enable module power **1:** Disable module power
6	**PGAL**	PGA left channel power control (low active) **0:** Enable module power **1:** Disable module power
5	**ADC**	ADC power control (low active) **0:** Enable module power **1:** Disable module power

4. Interrupt System

The RYZ has 24 interrupt lines that can interrupt normal program flow, allowing quick handling of external or internal events. When an interrupt is triggered, the normal program flow is stopped, and the MCU jumps into an Interrupt Service Routine (ISR) that handles the event processing. On completion of the ISR, normal code execution is continued.

The RYZ012 provides 16 level triggered interrupts and 8 edge triggered interrupts. Table 8 lists the available interrupt sources. Each of the interrupt lines can be enabled or disabled individually by setting the corresponding bit in register **IRQ:MASK**. Sometimes it is required to disable interrupt processing completely for the processing of critical sections. This can be done by enabling or disabling interrupts globally through register **IRQ:GIEN**.

The priority of each interrupt is configurable through register **IRQ:PRIO** to be at one of two possible levels: high priority or low priority. High priority interrupts can interrupt low priority ISRs.

Table 8. List of interrupts

Nr.	Unit	Description
Level triggered interrupts		
0	TIM0	Timer 0 interrupt
1	TIM1	Timer 1 interrupt
2	TIM2	Timer 2 interrupt
4	DMA	DMA interrupt
5	DFIFO	DFIFO interrupt
6	UART	UART interrupt
7	I2C_SPI	I2C Slave mapping mode or SPI Slave interrupt
8 - 12	RSVD	
13	BB	Baseband interrupt
14	PWM	PWM interrupt
15	RSVD	
Edge triggered interrupts		
16, 17	RSVD	
18	GPIO	GPIO interrupt
19	LSTIM	32kHz timer wakeup interrupt
20	STIM	System timer interrupt
21	GPIO2RISC	GPIO to RISC 0 interrupt
22	GPIO2RISC	GPIO to RISC 1 interrupt
23	RSVD	

The status of the individual interrupt lines is indicated in register **IRQ:IPS**. When an IRQ occurs, the corresponding bit will be set in **IRQ:IPS**. When an IRQ is processed, the corresponding bit must be reset. For edge triggered interrupts this is done by writing 0b1 to the corresponding bit. Level triggered interrupts are cleared through registers in the peripheral. For example to clear Timer 0 interrupt, write 0b1 to bit **TIMER:STATUS:TS0**.

4.1 Register Reference

4.1.1 IRQ:MASK - Interrupt Mask Configuration

Address: 0x0640
Reset: 0x000000

	7	6	5	4	3	2	1	0
IRQ:MASK[2]	RSVD	G2R1	G2R0	SYSTIM	LSTIM	GPIO	RSVD	
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	
IRQ:MASK[1]	RSVD	PWM	BB	RSVD				
	rw, 0	rw, 0	rw, 0	rw, 0				
IRQ:MASK[0]	I2C_SPI	UART	DFIFO	DMA	RSVD	TIM2	TIM1	TIM0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

22 **G2R1** Configure GPIO to RISC1 interrupt enable mask bit

0: Deactivate GPIO to RISC1 level-triggered interrupt

1: Activate GPIO to RISC1 level-triggered interrupt

21 **G2R0** Configure GPIO to RISC0 interrupt enable mask bit

0: Deactivate GPIO to RISC0 level-triggered interrupt

1: Activate GPIO to RISC0 level-triggered interrupt

20 **SYSTIM** Configure System Timer interrupt enable mask bit

0: Deactivate System Timer level-triggered interrupt

1: Activate System Timer level-triggered interrupt

19 **LSTIM** Configure PMTM interrupt enable mask bit

0: Deactivate PMTM level-triggered interrupt

1: Activate PMTM level-triggered interrupt

18 **GPIO** Configure GIPO interrupt enable mask bit

0: Deactivate GPIO level-triggered interrupt

1: Activate GPIO level-triggered interrupt

14 **PWM** Configure PWM interrupt enable mask bit

0: Deactivate PWM level-triggered interrupt

1: Activate PWM level-triggered interrupt

13 **BB** Configure BB interrupt enable mask bit

0: Deactivate BB level-triggered interrupt

1: Activate BB level-triggered interrupt

7 **I2C_SPI** Configure MIX or host triggered interrupt enable mask bit

0: Deactivate MIX level-triggered interrupt

1: Activate MIX level-triggered interrupt

6	**UART**	Configure UART interrupt enable mask bit **0:** Deactivate UART level-triggered interrupt **1:** Activate UART level-triggered interrupt
5	**DFIFO**	Configure DFIFO interrupt enable mask bit **0:** Deactivate DFIFO level-triggered interrupt **1:** Activate DFIFO level-triggered interrupt
4	**DMA**	Configure DMA interrupt enable mask bit **0:** Deactivate DMA level-triggered interrupt **1:** Activate DMA level-triggered interrupt
2	**TIM2**	Configure Timer 2 interrupt enable mask bit **0:** Deactivate Timer 2 level-triggered interrupt **1:** Activate Timer 2 level-triggered interrupt
1	**TIM1**	Configure Timer 1 interrupt enable mask bit **0:** Deactivate Timer 1 level-triggered interrupt **1:** Activate Timer 1 level-triggered interrupt
0	**TIM0**	Configure Timer 0 interrupt enable mask bit **0:** Deactivate Timer 0 level-triggered interrupt **1:** Activate Timer 0 level-triggered interrupt

4.1.2 IRQ:GIEN - Global Interrupt Enable

Address: 0x0643
Reset: 0x00

7	6	5	4	3	2	1	0
IRQ:GIEN			RSVD				GIEN
			rw, 0				rw, 0

0	**GIEN**	Global interrupt enable bit **0:** Global interrupts are disabled (pending interrupts are not serviced) **1:** Global interrupts are enabled

4.1.3 IRQ:PRIO - Interrupt Priority Configuration

Address: 0x0644
Reset: 0x000000

	7	6	5	4	3	2	1	0
IRQ:PRIO[2]	RSVD	G2R1	G2R0	SYSTIM	LSTIM	GPIO	RSVD	
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	
IRQ:PRIO[1]	RSVD	PWM	BB	RSVD				
	rw, 0	rw, 0	rw, 0	rw, 0				
IRQ:PRIO[0]	I2C_SPI	UART	DFIFO	DMA	RSVD	TIM2	TIM1	TIM0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

22 **G2R1** Configure GPIO to RISC1 interrupt priority configuration bit

0: Set LOW priority interrupt to specified module

1: Set HIGH priority interrupt to specified module

21 **G2R0** Configure GPIO to RISC0 interrupt priority configuration bit

0: Set LOW priority interrupt to specified module

1: Set HIGH priority interrupt to specified module

20 **SYSTIM** Configure System Timer interrupt priority configuration bit

0: Set LOW priority interrupt to specified module

1: Set HIGH priority interrupt to specified module

19 **LSTIM** Configure PMTM interrupt priority configuration bit

0: Set LOW priority interrupt to specified module

1: Set HIGH priority interrupt to specified module

18 **GPIO** Configure GIPO interrupt priority configuration bit

0: Set LOW priority interrupt to specified module

1: Set HIGH priority interrupt to specified module

14 **PWM** Configure PWM interrupt priority configuration bit

0: Set LOW priority interrupt to specified module

1: Set HIGH priority interrupt to specified module

13 **BB** Configure BB interrupt priority configuration bit

0: Set LOW priority interrupt to specified module

1: Set HIGH priority interrupt to specified module

7 **I2C_SPI** Configure MIX or host triggered interrupt priority configuration bit

0: Set LOW priority interrupt to specified module

1: Set HIGH priority interrupt to specified module

6 **UART** Configure UART interrupt priority configuration bit

0: Set LOW priority interrupt to specified module

1: Set HIGH priority interrupt to specified module

5 **DFIFO** Configure DFIFO interrupt priority configuration bit

0: Set LOW priority interrupt to specified module

1: Set HIGH priority interrupt to specified module

4 **DMA** Configure DMA interrupt priority configuration bit

0: Set LOW priority interrupt to specified module

1: Set HIGH priority interrupt to specified module

2 **TIM2** Configure Timer 2 interrupt priority configuration bit

0: Set LOW priority interrupt to specified module

1: Set HIGH priority interrupt to specified module

1 **TIM1** Configure Timer 1 interrupt priority configuration bit

0: Set LOW priority interrupt to specified module

1: Set HIGH priority interrupt to specified module

0 **TIM0** Configure Timer 0 interrupt priority configuration bit

0: Set LOW priority interrupt to specified module

1: Set HIGH priority interrupt to specified module

4.1.4 IRQ:IPS - Interrupt Pending Status

Address: 0x0648
Reset: 0x000000

	7	6	5	4	3	2	1	0
IRQ:IPS[2]	RSVD	G2R1	G2R0	SYSTIM	LSTIM	GPIO	RSVD	
	r, 0	rw1, 0	rw1, 0	rw1, 0	rw1, 0	rw1, 0	r, 0	
IRQ:IPS[1]	RSVD	PWM	BB	RSVD				
	r, 0	r, 0	r, 0	r, 0				
IRQ:IPS[0]	I2C_SPI	UART	DFIFO	DMA	RSVD	TIM2	TIM1	TIM0
	r, 0	r, 0	r, 0	r, 0	r, 0	r, 0	r, 0	r, 0

22 **G2R1** Read GPIO to RISC1 interrupt trigger state

0: There is NO triggered interrupt on specified module

21 **G2R0** Read GPIO to RISC0 interrupt trigger state

0: There is NO triggered interrupt on specified module

1: There is A triggered interrupt on the specified module

20 **SYSTIM** Read System Timer interrupt trigger state

0: There is NO triggered interrupt on specified module

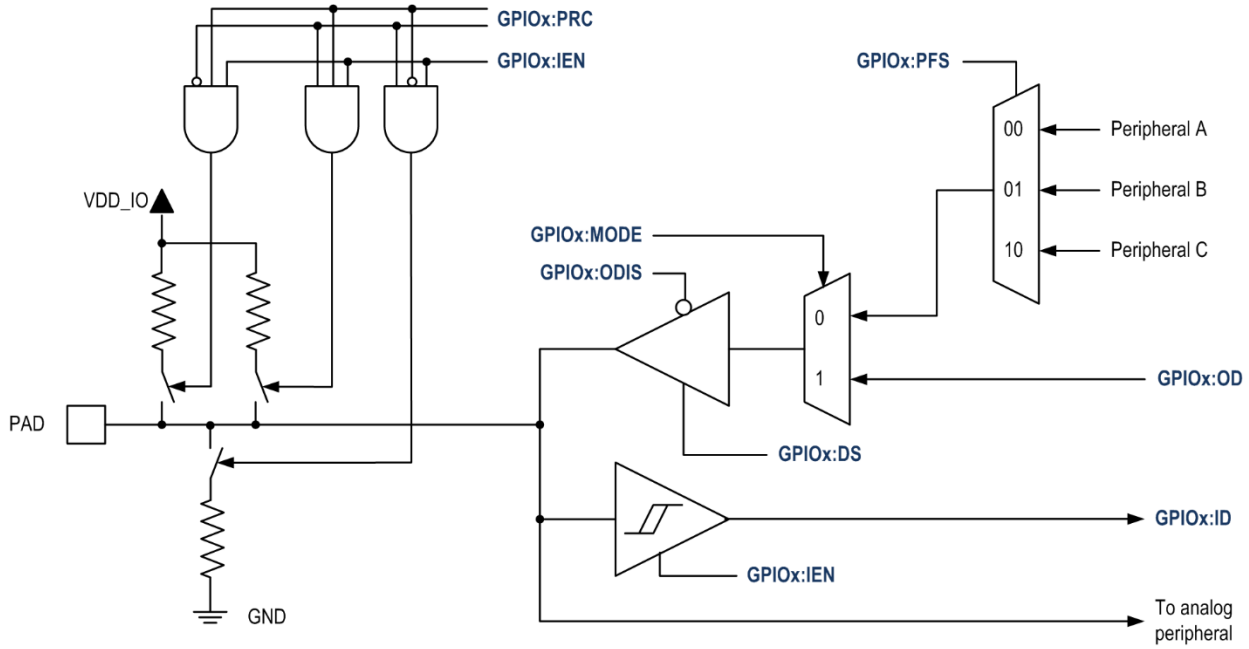
1: There is A triggered interrupt on the specified module

19	**LSTIM**	Read PMTM interrupt trigger state **0:** There is NO triggered interrupt on specified module **1:** There is A triggered interrupt on the specified module
18	**GPIO**	Read GPIO interrupt trigger state **0:** There is GPIO triggered interrupt on specified module **1:** There is GPIO triggered interrupt on the specified module
14	**PWM**	Read PWM interrupt trigger state **0:** There is NO triggered interrupt on specified module **1:** There is A triggered interrupt on the specified module
13	**BB**	Read BB interrupt trigger state **0:** There is BB triggered interrupt on specified module **1:** There is BB triggered interrupt on the specified module
7	**I2C_SPI**	Read MIX or host triggered interrupt trigger state **0:** There is NO triggered interrupt on specified module **1:** There is A triggered interrupt on the specified module
6	**UART**	Read UART interrupt trigger state **0:** There is NO triggered interrupt on specified module **1:** There is A triggered interrupt on the specified module
5	**DFIFO**	Read DFIFO interrupt trigger state **0:** There is NO triggered interrupt on specified module **1:** There is A triggered interrupt on the specified module
4	**DMA**	Read DMA interrupt trigger state **0:** There is NO triggered interrupt on specified module **1:** There is A triggered interrupt on the specified module
2	**TIM2**	Read Timer 2 interrupt trigger state **0:** There is NO triggered interrupt on specified module **1:** There is A triggered interrupt on the specified module
1	**TIM1**	Read Timer 1 interrupt trigger state **0:** There is NO triggered interrupt on specified module **1:** There is A triggered interrupt on the specified module
0	**TIM0**	Read Timer 0 interrupt trigger state **0:** There is NO triggered interrupt on specified module **1:** There is A triggered interrupt on the specified module

5. General Purpose IO

The 17 GPIO pins of the RYZ012 module are configurable as general-purpose I/O pins, which are freely controllable from the application or act as I/O pins for different peripheral units. A schematic of a GPIO is shown in the figure below.

Figure 8. Schematic of a GPIO bit



There are 4 GPIO blocks, named GPIOA to GPIOD. Each of these blocks has a set of registers to configure the behavior of the individual pins. An overview of the registers is given in Table 9. The last column provides a quick link to the detailed description of the corresponding register for each GPIO block.

Table 9. GPIO Configuration Register Overview

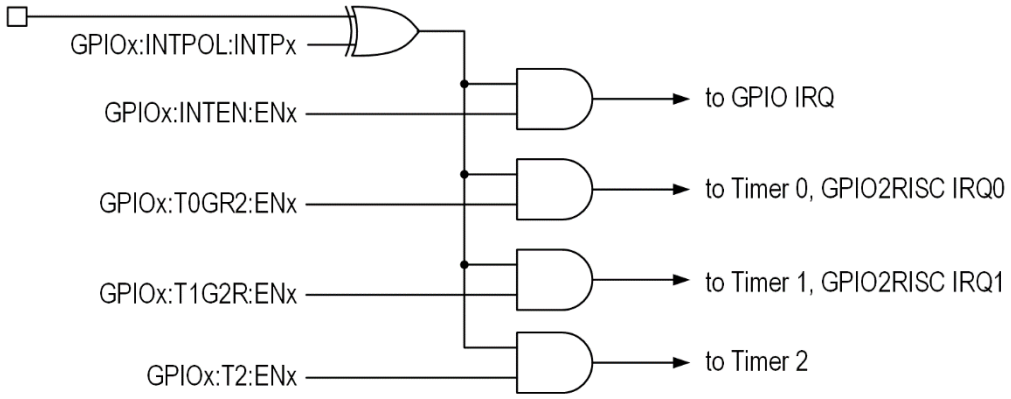
Register Name	Description	Link
Digital Registers		
IEN	Input enable. Set to 1 to enable input capture.	A, B, C, D
ID	Input data register. Holds the last value captured on corresponding pin.	A, B, C, D
ODIS	Output disable. Set to 1 to disable the output driver.	A, B, C, D
OD	Output data register. Values written to this registers are driven on the output if corresponding ODIS register is cleared.	A, B, C, D
DS	Driving strength control. A value of 0b1 selects high driving strength. See Table 1 for absolute values.	A, B, C, D
MODE	GPIO or peripheral mode select. If bit is set to 0b1, GPIO mode is selected, otherwise, one of the peripheral functions is used. The actual peripheral is selected through PFS register.	A, B, C, D
INTEN	Interrupt enable. If this bit is set to 0b1, interrupt generation on level change is enabled. Interrupt polarity is selected through INTPOL register.	A, B, C, D
INTPOL	Interrupt polarity control. A value of 0b0 selects rising edge as interrupt source.	A, B, C, D
PFS	Peripheral function select. See table Table 10.	A, B, C, D
T0G2R	Timer 0 and GPIO2RISC0 output enable. If this bit is set, the corresponding pin acts as input to Timer 0 or GPIO2RISC0 IRQ.	A, B, C, D
T1G2R	Timer 1 and GPIO2RISC1 output enable. If this bit is set, the corresponding pin acts as input to Timer 1 or GPIO2RISC1 IRQ.	A, B, C, D
T2	Timer 2 output enable. If this bit is set, the corresponding pin acts as input to Timer 2.	A, B, C, D

Register Name	Description	Link
	Analog Registers	
PRC	Pull resistor control. Pins configured in input mode (IE=0b1) can select from one of the following options: 2b'00 - No resistor connected 2b'01 - Weak pull-up resistor connected (typical 1MΩ) 2b'10 - Pull-down resistor connected (typical 160kΩ) 2b'11 - Strong pull-up resistor connected (typical 18kΩ)	**A**, **B**, **C**, **D**
WKUPEN	Wakeup enable. Set to 0b1 to enable wakeup from Suspend, Deep Sleep, or Standby Mode.	**A**, **B**, **C**, **D**
WKUPPOL	Wakeup polarity. Set to 0b1 to select wakeup on high level input or 0b0 to select wakeup on low level input.	**A**, **B**, **C**, **D**

5.1 GPIO to Timer and Interrupt Mapping

Individual GPIO pins can be configured to work as input to Timers or as interrupt source. The logic to realize this function is shown in the figure below. For both, timer input and interrupt input, the incoming GPIO signal is XOR'ed with **GPIOx:INTPOL** to control the phase that is used to trigger the timer action or interrupt. The registers **GPIOx:INTEN**, **GPIOx:T0G2R**, **GPIOx:T1G2R**, and **GPIOx:T2** control to which units the GPIO signal is forwarded.

Figure 9. GPIO Signal Forwarding to Timers and Interrupt System



5.2 GPIO / Peripheral Multiplexing

Table 10 shows a matrix of all available peripheral functions on a single page. Most GPIO pins are configured in GPIO mode after reset. However, PA7 is configured as SWS; and PB6, PB7, PD2, and PD7 are configured as SPI pins after reset.

A GPIO pin can be configured as Peripheral pin with the following procedure:

1. Clear the corresponding bit in register GPIOx:MODE to select Peripheral Mode.
2. Set the PFS register to the desired function.

Similarly, to switch from a Peripheral Mode to GPIO Mode the following procedure has to be executed:

1. Set the corresponding bit in register GPIOx:MODE to select GPIO Mode.
2. Perform additional configuration steps to such as enabling the output driver or pull-up/pull-down selection.

Table 10 Peripheral Function Mapping

Port		A			B					C					D			
Pin		0	1	7	1	4	5	6	7	0	1	2	3	4	2	3	4	7
Pin-Nr.		2	3	4	5	9	10	11	12	15	16	17	18	19	22	23	24	1
UART	RX	2							2				1					
	TX				1													
	RTS			1				2		2								
	CTS													1				
7816	TRX											1				2		2
	CLK		1															
SPI	DI							1										
	DO								1									
	CK																	0
	CN														0			
DMIC	DI	0																
	CLK		0															
I2S	SDI															1		
	SDO																1	
	LR														1			
	CLK		2															
	BCLK																	1
I2C	SCK										0		2					
	SDA									0		2						
PWM0		1(N)									2	0		2(N)				
PWM1											1(N)		0			0(N)		
PWM2														0			2(N)	
PWM3															2			
PWM4					0	1				1(N)								
PWM5							1											
SDM						0:P0	0:N0	0:P1	0:N1									
Analog	ADC				1	4	5	6	7					8				
	LPC				1	4	5	6	7									
	PGA									0P	0N	1P	1N					
SWIRE	SWS			0														
	SWM																0	

5.3 GPIOA Register Reference

5.3.1 GPIOA:ID - GPIOA Input Data

Address: 0x0580
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOA:ID	IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0
	r, 0	r, 0	r, 0	r, 0	r, 0	r, 0	r, 0	r, 0

0, 1, 2, 3, 4, 5, 6, 7 **INx** GPIOA Input Data

The input signal level is indicated bitwise for the corresponding pin.

0: Digital LOW level signal is available at the corresponding pin

1: Digital HIGH level signal is available at the corresponding pin

5.3.2 GPIOA:IEN - GPIOA Input Enable

For all unused GPIOs the corresponding IEx must be disabled.

Address: 0x0581

Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOA:IEN	IE7	IE6	IE5	IE4	IE3	IE2	IE1	IE0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **IEx** GPIOA Input Enable

Enable the corresponding bit as GPIO input.

0: Disable corresponding pin as Input

1: Enable corresponding pin as Input

5.3.3 GPIOA:ODIS - GPIOA Output Disable

Address: 0x0582
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOA:ODIS	ODIS7	ODIS6	ODIS5	ODIS4	ODIS3	ODIS2	ODIS1	ODIS0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **ODISx** GPIOA Output Disable

Disable the corresponding bit as GPIO output.

0: Enable corresponding pin as Output

1: Disable corresponding pin as Output

5.3.4 GPIOA:OD - GPIOA Output Data

Address: 0x0583
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOA:OD	CFGO7	CFGO6	CFGO5	CFGO4	CFGO3	CFGO2	CFGO1	CFGO0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **CFGOx** GPIOA Output Data

Set digital output level to corresponding pin.

0: Set digital LOW on corresponding pin

1: Set digital HIGH on corresponding pin

5.3.5 GPIOA:INTPOL - GPIOA Interrupt Polarity

Address: 0x0584
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOA:INTPOL	INTP7	INTP6	INTP5	INTP4	INTP3	INTP2	INTP1	INTP0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **INTPx** GPIO Polarity

Use the corresponding bit to set the interrupt polarity.

0: Interrupt is LOW active on corresponding pin

1: Interrupt is HIGH active on corresponding pin

5.3.6 GPIOA:DS - GPIOA Driving Strength

Address: 0x0585
Reset: 0xFF

	7	6	5	4	3	2	1	0
GPIOA:DS	DS7	DS6	DS5	DS4	DS3	DS2	DS1	DS0
	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1

0, 1, 2, 3, 4, 5, 6, 7 **DSx** GPIO Driver strength (DS)

Use the corresponding bit to set the driving level.

0: Set minimum driving level on corresponding pin

1: Set maximum driving level on corresponding pin

5.3.7 GPIOA:MODE - GPIOA Mode Selection

Address: 0x0586
Reset: 0x3F

	7	6	5	4	3	2	1	0
GPIOA:MODE	MODE7	MODE6	MODE5	MODE4	MODE3	MODE2	MODE1	MODE0
	rw, 0	rw, 0	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1

0, 1, 2, 3, 4, 5, 6, 7 **MODEx** GPIOA Mode Selection

Controls whether GPIO or peripheral mode is used for the corresponding bit.

0: Pin is controlled by peripheral selected through PFS register

1: Pin is used as general-purpose I/O

5.3.8 GPIOA:INTEN - GPIOA Interrupt Enable

Address: 0x0587
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOA:INTEN	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **ENx** GPIOA Interrupt Enable

Enable the corresponding bit as GPIO interrupt source. The interrupt polarity is controlled by register GPIOx:INTP.

0: Disable interrupt generation on corresponding pin

1: Enable interrupt generation on corresponding pin

5.3.9 GPIOA:PFS - Peripheral Function Selection Register

Address: 0x05a8
Reset: 0x0000

	7	6	5	4	3	2	1	0
GPIOA:PFS[1]	PF7		RSVD					
	rw, 0		rw, 0					
GPIOA:PFS[0]	RSVD				PF1		PF0	
	rw, 0				rw, 0		rw, 0	

15:14 **PF7** Peripheral select if pin is configured in peripheral mode.

00: SWS (Default)

01: UART_RTS

10: Not used

3:2 **PF1** Peripheral select if pin is configured in peripheral mode.

00: DMIC_CLK

01: 7816_CLK

10: I2S_CLK

1:0 **PF0** Peripheral select if pin is configured in peripheral mode.

00: DMIC_DI

01: PWM0_N

10: UART_RX

5.3.10 GPIOA:T0G2R - GPIOA Extra Peripheral Mapping 0

Address: 0x05b8
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOA:T0G2R	T0G2R7	T0G2R6	T0G2R5	T0G2R4	T0G2R3	T0G2R2	T0G2R1	T0G2R0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **T0G2Rx** GPIO extra peripheral mapping

Using this register individual GPIO pins can be mapped to Timer 0 and to the GPIO2RISC IRQ0 interrupt source.

0: GPIO is not mapped to Timer 0 and GPIO2RISC IRQ0

1: GPIO is mapped to Timer 0 and GPIO2RISC IRQ0

5.3.11 GPIOA:T1G2R - GPIOA Extra Peripheral Mapping 1

Address: 0x05c0
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOA:T1G2R	T1G2R7	T1G2R6	T1G2R5	T1G2R4	T1G2R3	T1G2R2	T1G2R1	T1G2R0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **T1G2Rx** GPIO extra peripheral mapping

Using this register individual GPIO pins can be mapped to Timer 1 or to the GPIO2RISC IRQ1 interrupt source.

0: GPIO is not mapped to Timer 1 and GPIO2RISC IRQ1

1: GPIO is mapped to Timer 1 and GPIO2RISC IRQ1

5.3.12 GPIOA:T2 - GPIOA Extra Peripheral Mapping 2

Address: 0x05c8
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOA:T2	T2_7	T2_6	T2_5	T2_4	T2_3	T2_2	T2_1	T2_0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **T2_x** GPIO extra peripheral mapping

Using this register individual GPIO pins can be mapped to Timer 2.

0: GPIO is not mapped to Timer 2

1: GPIO is mapped to Timer 2

5.4 GPIOA Analog Register Reference

5.4.1 GPIOA:PRC - Port A Pull Register Control Low

Address: 0x000e
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOA:PRC[1]	PSEL7		PSEL6		PSEL5		PSEL4	
	rw, 0		rw, 0		rw, 0		rw, 0	
GPIOA:PRC[0]	PSEL3		PSEL2		PSEL1		PSEL0	
	rw, 0		rw, 0		rw, 0		rw, 0	

1:0, 3:2, 5:4, 7:6, 9:8, 11:10, 13:12, 15:14 **PSELx** Pull-up/pull-down resistor configuration

00: No pull-up or pull-down connected

01: Weak pull-up register connected (typical 1MΩ)

10: Pull-down resistor connected (typical 160kΩ)

11: Strong pull-up resistor connected (typical 18kΩ)

5.4.2 GPIOA:WKUPPOL - GPIOA Wakeup Polarity Control

Address: 0x0021
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOA:WKUPPOL	POL7	POL6	POL5	POL4	POL3	POL2	POL1	POL0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **POLx** PA corresponding pin wakeup polarity level selection

0: Select LOW level on Port Pin to trigger wakeup

1: Select HIGH level on Port Pin to trigger wakeup

5.4.3 GPIOA:WKUPEN - GPIOA Wakeup Enable

Address: 0x0027
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOA:WKUPEN	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **Enx** Enable PA as wakeup source for corresponding pin

0: Disables Port Pin as wakeup source

1: Enables Port Pin as wakeup source

5.5 GPIOB Register Reference

5.5.1 GPIOB:ID - GPIOB Input Data

Address: 0x0588
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOB:ID	IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0
	r, 0	r, 0	r, 0	r, 0	r, 0	r, 0	r, 0	r, 0

0, 1, 2, 3, 4, 5, 6, 7 **INx** GPIOB Input Data

The input signal level is indicated bitwise for the corresponding pin.

0: Digital LOW level signal is available at the corresponding pin

1: Digital HIGH level signal is available at the corresponding pin

5.5.2 GPIOB:IEN - GPIOB Input Enable

For all unused GPIOs the corresponding IEx must be disabled.

Address: 0x0589

Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOB:IEN	IE7	IE6	IE5	IE4	IE3	IE2	IE1	IE0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **IEx** GPIOB Input Enable

Enable the corresponding bit as GPIO input.

0: Disable corresponding pin as Input

1: Enable corresponding pin as Input

5.5.3 GPIOB:ODIS - GPIOB Output Disable

Address: 0x058a
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOB:ODIS	ODIS7	ODIS6	ODIS5	ODIS4	ODIS3	ODIS2	ODIS1	ODIS0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **ODISx** GPIOB Output Disable

Disable the corresponding bit as GPIO output.

0: Enable corresponding pin as Output

1: Disable corresponding pin as Output

5.5.4 GPIOB:OD - GPIOB Output Data

Address: 0x058b
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOB:OD	CFGO7	CFGO6	CFGO5	CFGO4	CFGO3	CFGO2	CFGO1	CFGO0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **CFGOx** GPIOB Output Data

Set digital output level to corresponding pin.

0: Set digital LOW on corresponding pin

1: Set digital HIGH on corresponding pin

5.5.5 GPIOB:INTPOL - GPIOB Interrupt Polarity

Address: 0x058c
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOB:INTPOL	INTP7	INTP6	INTP5	INTP4	INTP3	INTP2	INTP1	INTP0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **INTPx** GPIOB Interrupt Polarity

Use the corresponding bit to set the interrupt polarity.

0: Interrupt is LOW active on corresponding pin

1: Interrupt is HIGH active on corresponding pin

5.5.6 GPIOB:DS - GPIOB Driving strength

Address: 0x058d
Reset: 0xFF

	7	6	5	4	3	2	1	0
GPIOB:DS	DS7	DS6	DS5	DS4	DS3	DS2	DS1	DS0
	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1

0, 1, 2, 3, 4, 5, 6, 7 **DSx** GPIOB Driving strength

Use the corresponding bit to set the driving level.

0: Set minimum driving level on corresponding pin

1: Set maximum driving level on corresponding pin

5.5.7 GPIOB:MODE - GPIOB Mode Selection

Address: 0x058e
Reset: 0x3F

	7	6	5	4	3	2	1	0
GPIOB:MODE	MODE7	MODE6	MODE5	MODE4	MODE3	MODE2	MODE1	MODE0
	rw, 0	rw, 0	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1

0, 1, 2, 3, 4, 5, 6, 7 **MODEx** GPIOB Mode Selection

Controls whether GPIO or peripheral mode is used for the corresponding bit.

0: Pin is controlled by peripheral selected through PFS register

1: Pin is used as general-purpose I/O

5.5.8 GPIOB:INTEN - GPIO Interrupt Enable PB

Address: 0x058f
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOB:INTEN	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **ENx** GPIOB Interrupt Enable

Enable the corresponding bit as GPIO interrupt source. The interrupt polarity is controlled by register GPIOx:INTP.

0: Disable interrupt generation on corresponding pin

1: Enable interrupt generation on corresponding pin

5.5.9 GPIOB:PFS - Peripheral Function Selection Register

Address: 0x05aa
Reset: 0x5000

	7	6	5	4	3	2	1	0
GPIOB:PFS[1]	PF7		PF6		PF5		PF4	
	rw, 1		rw, 1		rw, 0		rw, 0	
GPIOB:PFS[0]	RSVD				PF1		RSVD	
	rw, 0				rw, 0		rw, 0	

15:14 **PF7** Peripheral select if pin is configured in peripheral mode.

00: SDM_N1

01: SPI_DO

10: UART_RX

13:12 **PF6** Peripheral select if pin is configured in peripheral mode.

00: SDM_P1

01: SPI_DI

10: UART_RTS

11:10 **PF5** Peripheral select if pin is configured in peripheral mode.

00: SDM_N0

01: PWM5

10: Not used

9:8 **PF4** Peripheral select if pin is configured in peripheral mode.

00: SDM_P0

01: PWM4

10: Not used

3:2 **PF1** Peripheral select if pin is configured in peripheral mode.

00: PWM4

01: UART_TX

10: ATSEL2

5.5.10 GPIOB:T0G2R - GPIOB Extra Peripheral Mapping 0

Address: 0x05b9
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOB:T0G2R	T0G2R7	T0G2R6	T0G2R5	T0G2R4	T0G2R3	T0G2R2	T0G2R1	T0G2R0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **T0G2Rx** GPIO extra peripheral mapping

Using this register individual GPIO pins can be mapped to Timer 0 and to the GPIO2RISC IRQ0 interrupt source.

0: GPIO is not mapped to Timer 0 and GPIO2RISC IRQ0

1: GPIO is mapped to Timer 0 and GPIO2RISC IRQ0

5.5.11 GPIOB:T1G2R - GPIOB Extra Peripheral Mapping 1

Address: 0x05c1
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOB:T1G2R	T1G2R7	T1G2R6	T1G2R5	T1G2R4	T1G2R3	T1G2R2	T1G2R1	T1G2R0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **T1G2Rx** GPIO extra peripheral mapping

Using this register individual GPIO pins can be mapped to Timer 1 or to the GPIO2RISC IRQ1 interrupt source.

0: GPIO is not mapped to Timer 1 and GPIO2RISC IRQ1

1: GPIO is mapped to Timer 1 and GPIO2RISC IRQ1

5.5.12 GPIOB:T2 - GPIOB Extra Peripheral Mapping 2

Address: 0x05c9
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOB:T2	T2_7	T2_6	T2_5	T2_4	T2_3	T2_2	T2_1	T2_0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **T2_x** GPIO extra peripheral mapping

Using this register individual GPIO pins can be mapped to Timer 2.

0: GPIO is not mapped to Timer 2

1: GPIO is mapped to Timer 2

5.6 GPIOB Analog Register Reference

5.6.1 GPIOB:PRC - Port B Pull Resistor Control Low

Address: 0x0010
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOB:PRC[1]	PSEL7		PSEL6		PSEL5		PSEL4	
	rw, 0		rw, 0		rw, 0		rw, 0	
GPIOB:PRC[0]	PSEL3		PSEL2		PSEL1		PSEL0	
	rw, 0		rw, 0		rw, 0		rw, 0	

1:0, 3:2, 5:4, 7:6, 9:8, 11:10, 13:12, 15:14 **PSELx** Pull-up/pull-down resistor configuration

00: No pull-up or pull-down connected

01: Weak pull-up register connected (typical 1MΩ)

10: Pull-down resistor connected (typical 160kΩ)

11: Strong pull-up resistor connected (typical 18kΩ)

5.6.2 GPIOB:WKUPPOL - GPIOB Wakeup Polarity Control

Address: 0x0022
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOB:WKUPPOL	POL7	POL6	POL5	POL4	POL3	POL2	POL1	POL0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **POLx** PB corresponding pin wakeup polarity level selection

0: Select LOW level on Port Pin to trigger wakeup

1: Select HIGH level on Port Pin to trigger wakeup

5.6.3 GPIOB:WKUPEN - GPIOB Wakeup Enable

Address: 0x0028
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOB:WKUPEN	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **Enx** Enable PB as wakeup source for corresponding pin

0: Disables Port Pin as wakeup source

1: Enables Port Pin as wakeup source

5.7 GPIOC Register Reference

5.7.1 GPIOC:ID - GPIOC Input Data

Address: 0x0590
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOC:ID	IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0
	r, 0	r, 0	r, 0	r, 0	r, 0	r, 0	r, 0	r, 0

0, 1, 2, 3, 4, 5, 6, 7 **INx** GPIOC Input Data

The input signal level is indicated bitwise for the corresponding pin.

0: Digital LOW level signal is available at the corresponding pin

1: Digital HIGH level signal is available at the corresponding pin

5.7.2 GPIOC:IEN - GPIOC Input Enable

For all unused GPIOs the corresponding IEx must be disabled.

Address: 0x0591

Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOC:IEN	IE7	IE6	IE5	IE4	IE3	IE2	IE1	IE0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **IEx** GPIOC Input Enable

Enable the corresponding bit as GPIO input.

0: Disable corresponding pin as Input

1: Enable corresponding pin as Input

5.7.3 GPIOC:ODIS - GPIOC Output Disable

Address: 0x0592
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOC:ODIS	ODIS7	ODIS6	ODIS5	ODIS4	ODIS3	ODIS2	ODIS1	ODIS0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **ODISx** GPIOC Output Disable

Disable the corresponding bit as GPIO output.

0: Enable corresponding pin as Output

1: Disable corresponding pin as Output

5.7.4 GPIOC:OD - GPIOC Output Data

Address: 0x0593
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOC:OD	CFGO7	CFGO6	CFGO5	CFGO4	CFGO3	CFGO2	CFGO1	CFGO0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **CFGOx** GPIOC Output Data

Set digital output level to corresponding pin.

0: Set digital LOW on corresponding pin

1: Set digital HIGH on corresponding pin

5.7.5 GPIOC:INTPOL - GPIOC Interrupt Polarity

Address: 0x0594
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOC:INTPOL	INTP7	INTP6	INTP5	INTP4	INTP3	INTP2	INTP1	INTP0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **INTPx** GPIOC Interrupt Polarity

Use the corresponding bit to set the interrupt polarity.

0: Interrupt is LOW active on corresponding pin

1: Interrupt is HIGH active on corresponding pin

5.7.6 GPIOC:DS - GPIOC Driving Strength

Address: 0x0595
Reset: 0xFF

	7	6	5	4	3	2	1	0
GPIOC:DS	DS7	DS6	DS5	DS4	DS3	DS2	DS1	DS0
	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1

0, 1, 2, 3, 4, 5, 6, 7	**DSx**	GPIO Driving Strength (DS) Use the corresponding bit to set the driving level. **0:** Set minimum driving level on corresponding pin **1:** Set maximum driving level on corresponding pin

5.7.7 GPIOC:MODE - GPIOC Mode Selection

Address: 0x0596
Reset: 0x3F

	7	6	5	4	3	2	1	0
GPIOC:MODE	MODE7	MODE6	MODE5	MODE4	MODE3	MODE2	MODE1	MODE0
	rw, 0	rw, 0	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1

0, 1, 2, 3, 4, 5, 6, 7	**MODEx**	GPIOC Mode Selection Controls whether GPIO or peripheral mode is used for the corresponding bit. **0:** Pin is controlled by peripheral selected through PFS register **1:** Pin is used as general-purpose I/O

5.7.8 GPIOC:INTEN - GPIOC Interrupt Enable PC

Address: 0x0597
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOC:INTEN	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7	**ENx**	GPIOC Interrupt Enable Enable the corresponding bit as GPIO interrupt source. The interrupt polarity is controlled by register GPIOx:INTP. **0:** Disable interrupt generation on corresponding pin **1:** Enable interrupt generation on corresponding pin

5.7.9 GPIOC:PFS - Peripheral Function Selection Register

Address: 0x05ac
Reset: 0x0050

	7	6	5	4	3	2	1	0
GPIOC:PFS[1]	RSVD						PF4	
	rw, 0						rw, 0	
GPIOC:PFS[0]	PF3		PF2		PF1		PF0	
	rw, 1		rw, 1		rw, 0		rw, 0	

9:8 **PF4** Peripheral select if pin is configured in peripheral mode.

00: PWM2

01: UART_CTS

10: PWM0_N

7:6 **PF3** Peripheral select if pin is configured in peripheral mode.

00: PWM1

01: UART_RX

10: I2C_SCK

5:4 **PF2** Peripheral select if pin is configured in peripheral mode.

00: PWM0

01: UART_TX

10: I2C_SDA

3:2 **PF1** Peripheral select if pin is configured in peripheral mode.

00: I2C_SCK

01: PWM1_N

10: PWM0

1:0 **PF0** Peripheral select if pin is configured in peripheral mode.

00: I2C_SDA

01: PWM4_N

10: UART_RTS

5.7.10 GPIOC:T0G2R - GPIOC Extra Peripheral Mapping 0

Address: 0x05ba
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOC:T0G2R	T0G2R7	T0G2R6	T0G2R5	T0G2R4	T0G2R3	T0G2R2	T0G2R1	T0G2R0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **T0G2Rx** GPIO extra peripheral mapping

Using this register individual GPIO pins can be mapped to Timer 0 and to the GPIO2RISC IRQ0 interrupt source.

0: GPIO is not mapped to Timer 0 and GPIO2RISC IRQ0

1: GPIO is mapped to Timer 0 and GPIO2RISC IRQ0

5.7.11 GPIOC:T1G2R - GPIOC Extra Peripheral Mapping 1

Address: 0x05c2
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOC:T1G2R	T1G2R7	T1G2R6	T1G2R5	T1G2R4	T1G2R3	T1G2R2	T1G2R1	T1G2R0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **T1G2Rx** GPIO extra peripheral mapping

Using this register individual GPIO pins can be mapped to Timer 1 or to the GPIO2RISC IRQ1 interrupt source.

0: GPIO is not mapped to Timer 1 and GPIO2RISC IRQ1

1: GPIO is mapped to Timer 1 and GPIO2RISC IRQ1

5.7.12 GPIOC:T2 - GPIOC Extra Peripheral Mapping 2

Address: 0x05ca
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOC:T2	T2_7	T2_6	T2_5	T2_4	T2_3	T2_2	T2_1	T2_0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **T2_x** GPIO extra peripheral mapping

Using this register individual GPIO pins can be mapped to Timer 2.

0: GPIO is not mapped to Timer 2

1: GPIO is mapped to Timer 2

5.8 GPIOC Analog Register Reference

5.8.1 GPIOC:PRC - Port C Pull Resistor Control Low

Address: 0x0012
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOC:PRC[1]	PSEL7		PSEL6		PSEL5		PSEL4	
	rw, 0		rw, 0		rw, 0		rw, 0	
GPIOC:PRC[0]	PSEL3		PSEL2		PSEL1		PSEL0	
	rw, 0		rw, 0		rw, 0		rw, 0	

1:0, 3:2, 5:4, 7:6, 9:8, 11:10, 13:12, 15:14 **PSELx** Pull-up/pull-down resistor configuration

00: No pull-up or pull-down connected

01: Weak Pull-up register connected (typical 1MΩ)

10: Pull-down resistor connected (typical 160kΩ)

11: Strong pull-up resistor connected (typical 18kΩ)

5.8.2 GPIOC:WKUPPOL - GPIOC Wakeup Polarity Control

Address: 0x0023
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOC:WKUPPOL	POL7	POL6	POL5	POL4	POL3	POL2	POL1	POL0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **POLx** PC corresponding pin wakeup polarity level selection

0: Select LOW level on Port Pin to trigger wakeup

1: Select HIGH level on Port Pin to trigger wakeup

5.8.3 GPIOC:WKUPEN - GPIOC Wakeup Enable

Address: 0x0029
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOC:WKUPEN	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **Enx** Enable PC as wakeup source for corresponding pin

0: Disables Port Pin as wakeup source

1: Enables Port Pin as wakeup source

5.9 GPIOD Register Reference

5.9.1 GPIOD:ID - GPIOD Input Data

Address: 0x0598
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOD:ID	IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0
	r, 0	r, 0	r, 0	r, 0	r, 0	r, 0	r, 0	r, 0

0, 1, 2, 3, 4, 5, 6, 7 **INx** GPIOD Input Data

The input signal level is indicated bitwise for the corresponding pin.

0: Digital LOW level signal is available at the corresponding pin

1: Digital HIGH level signal is available at the corresponding pin

5.9.2 GPIOD:IEN - GPIOD Input Enable

For all unused GPIOs the corresponding IEx must be disabled.

Address: 0x0599

Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOD:IEN	IE7	IE6	IE5	IE4	IE3	IE2	IE1	IE0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **IEx** GPIOD Input Enable

Enable the corresponding bit as GPIO input.

0: Disable corresponding pin as Input

1: Enable corresponding pin as Input

5.9.3 GPIOD:ODIS - GPIOD Output Disable

Address: 0x059a
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOD:ODIS	ODIS7	ODIS6	ODIS5	ODIS4	ODIS3	ODIS2	ODIS1	ODIS0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **ODISx** GPIOD Output Disable

Disable the corresponding bit as GPIO output.

0: Enable corresponding pin as Output

1: Disable corresponding pin as Output

5.9.4 GPIOD:OD - GPIOD Output Data

Address: 0x059b
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOD:OD	CFGO7	CFGO6	CFGO5	CFGO4	CFGO3	CFGO2	CFGO1	CFGO0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **CFGOx** GPIOD Output Data

Set digital output level to corresponding pin.

0: Set digital LOW on corresponding pin

1: Set digital HIGH on corresponding pin

5.9.5 GPIOD:INTPOL - GPIOD Interrupt Polarity

Address: 0x059c
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOD:INTPOL	INTP7	INTP6	INTP5	INTP4	INTP3	INTP2	INTP1	INTP0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **INTPx** GPIOD Interrupt Polarity

Use the corresponding bit to set the interrupt polarity.

0: Interrupt is LOW active on corresponding pin

1: Interrupt is HIGH active on corresponding pin

5.9.6 GPIOD:DS - GPIOD Driving strength

Address: 0x059d
Reset: 0xFF

	7	6	5	4	3	2	1	0
GPIOD:DS	DS7	DS6	DS5	DS4	DS3	DS2	DS1	DS0
	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1

0, 1, 2, 3, 4, 5, 6, 7 **DSx** GPIOD Driving strength

Use the corresponding bit to set the driving level.

0: Set minimum driving level on corresponding pin

1: Set maximum driving level on corresponding pin

5.9.7 GPIOD:MODE - GPIOD Mode Selection

Address: 0x059e
Reset: 0x3F

	7	6	5	4	3	2	1	0
GPIOD:MODE	MODE7	MODE6	MODE5	MODE4	MODE3	MODE2	MODE1	MODE0
	rw, 0	rw, 0	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1

0, 1, 2, 3, 4, 5, 6, 7 **MODEx** GPIOD Mode Selection

Controls whether GPIO or peripheral mode is used for the corresponding bit.

0: Pin is controlled by peripheral selected through PFS register

1: Pin is used as general-purpose I/O

5.9.8 GPIOD:INTEN - GPIOD Interrupt Enable

Address: 0x059f
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOD:INTEN	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **ENx** GPIOD Interrupt Enable

Enable the corresponding bit as GPIO interrupt source. The interrupt polarity is controlled by register GPIOx:INTP.

0: Disable interrupt generation on corresponding pin

1: Enable interrupt generation on corresponding pin

5.9.9 GPIOD:PFS - Peripheral Function Selection Register

Address: 0x05ae
Reset: 0x0000

	7	6	5	4	3	2	1	0
GPIOD:PFS[1]	PF7		RSVD				PF4	
	rw, 0		rw, 0				rw, 0	
GPIOD:PFS[0]	PF3		PF2		RSVD			
	rw, 0		rw, 0		rw, 0			

15:14 **PF7** Peripheral select if pin is configured in peripheral mode.

00: SPI_CK

01: I2S_BCK

10: UART_TX

9:8 **PF4** Peripheral select if pin is configured in peripheral mode.

00: SWM

01: I2S_SDO

10: PWM2_N

7:6 **PF3** Peripheral select if pin is configured in peripheral mode.

00: PWM1_N

01: I2S_SDI

10: UART_TX

5:4 **PF2** Peripheral select if pin is configured in peripheral mode.

00: SPI_CN

01: I2S_LR

10: PWM3

5.9.10 GPIOD:T0G2R - GPIOD Extra Peripheral Mapping 0

Address: 0x05bb
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOD:T0G2R	T0G2R7	T0G2R6	T0G2R5	T0G2R4	T0G2R3	T0G2R2	T0G2R1	T0G2R0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **T0G2Rx** GPIO extra peripheral mapping

Using this register individual GPIO pins can be mapped to Timer 0 and to the GPIO2RISC IRQ0 interrupt source.

0: GPIO is not mapped to Timer 0 and GPIO2RISC IRQ0

1: GPIO is mapped to Timer 0 and GPIO2RISC IRQ0

5.9.11 GPIOD:T1G2R - GPIOD Extra Peripheral Mapping 1

Address: 0x05c3
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOD:T1G2R	T1G2R7	T1G2R6	T1G2R5	T1G2R4	T1G2R3	T1G2R2	T1G2R1	T1G2R0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **T1G2Rx** GPIO extra peripheral mapping

Using this register individual GPIO pins can be mapped to Timer 1 or to the GPIO2RISC IRQ1 interrupt source.

0: GPIO is not mapped to Timer 1 and GPIO2RISC IRQ1

1: GPIO is mapped to Timer 1 and GPIO2RISC IRQ1

5.9.12 GPIOD:T2 - GPIOD Extra Peripheral Mapping 2

Address: 0x05cb
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOD:T2	T2_7	T2_6	T2_5	T2_4	T2_3	T2_2	T2_1	T2_0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **T2_x** GPIO extra peripheral mapping

Using this register individual GPIO pins can be mapped to Timer 2.

0: GPIO is not mapped to Timer 2

1: GPIO is mapped to Timer 2

5.10 GPIOD Analog Register Reference

5.10.1 GPIOD:PRC - Port D Pull Register Control Low

Address: 0x0014
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOD:PRC[1]	PSEL7		PSEL6		PSEL5		PSEL4	
	rw, 0		rw, 0		rw, 0		rw, 0	
GPIOD:PRC[0]	PSEL3		PSEL2		PSEL1		PSEL0	
	rw, 0		rw, 0		rw, 0		rw, 0	

1:0, 3:2, 5:4, 7:6, 9:8, 11:10, 13:12, 15:14 **PSELx** Pull-up/pull-down resistor configuration

00: No pull-up or pull-down connected

01: Weak Pull-up register connected (typical 1MΩ)

10: Pull-down resistor connected (typical 160kΩ)

11: Strong pull-up resistor connected (typical 18kΩ)

5.10.2 GPIOD:WKUPPOL - GPIOD Wakeup Polarity Control

Address: 0x0024
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOD:WKUPPOL	POL7	POL6	POL5	POL4	POL3	POL2	POL1	POL0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **POLx** PD corresponding pin wakeup polarity level selection

0: Select LOW level on Port Pin to trigger wakeup

1: Select HIGH level on Port Pin to trigger wakeup

5.10.3 GPIOD:WKUPEN - GPIOD Wakeup Enable

Address: 0x0029
Reset: 0x00

	7	6	5	4	3	2	1	0
GPIOD:WKUPEN	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5, 6, 7 **Enx** Enable PD as wakeup source for corresponding pin

0: Disables Port Pin as wakeup source

1: Enables Port Pin as wakeup source

6. I2C Interface

The RYZ012 embeds an I2C hardware module, which can act as I2C Master or I2C Slave. I2C is a popular inter-IC interface requiring only 2 bus lines, a serial data line (SDA) and a serial clock line (SCL).

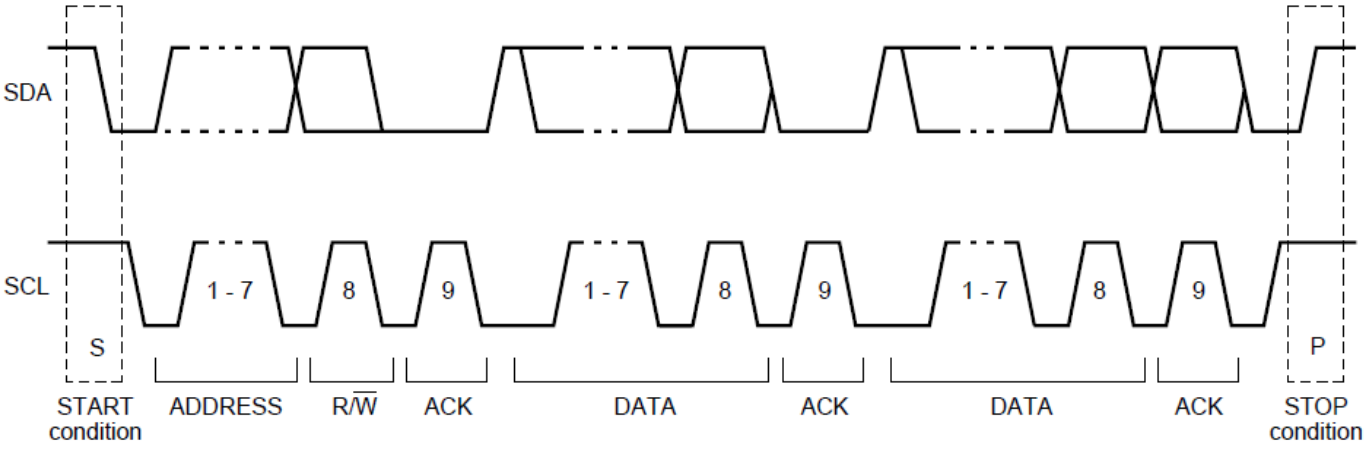
6.1 Communication Protocol

The I2C unit supports I2C Standard Mode (100kbps) and I2C Fast Mode (400kbps) with restriction that system clock must be running at least at 10x the data rate. The two wires, SDA and SCL (SCK) carry information between master device and slave device connected to the bus. Each device is identified by unique address (ID). The master initiates the data transfer on the bus and generates the clock signals used for this transfer. The slave device is the device addressed by the master.

Both SDA and SCL are bidirectional lines connected to a positive supply voltage with a pull-up resister. It is recommended to use an external 3.3kΩ pull-up resistor. For standard mode, the strong internal pull-up resistor can be used instead of the external 3.3kΩ resistor.

When the bus is free, both lines are HIGH. Data on the SDA line must remain stable while the clock signal (SCL) is at high level. SDA level changes are allowed when SCL is low, with the exception of the I2C Start and I2C Stop Condition, which initiate and terminate a transmission.

Figure 10. I2C Timing Chart



A start condition is always followed by an address byte. The I2C master sends the 7 bit ID of the slave followed by a bit that defines whether data is sent to the slave (RW=0) or read from the slave (RW=1). The slave being addressed needs to acknowledge the transfer by pulling SDA low. Each byte of the following bytes needs to be acknowledged by the slave (in case of write) or by the master (in case of read).

6.2 I2C Slave Mode

By default, the I2C unit of the RYZ012 is working in Slave Mode. The I2C slave address of the device is configured in register **I2C:SADR**. In I2C Slave Mode, either Direct Memory Access (DMA) Mode or Mapping Mode can be used. The operating mode is selected by bit **I2C:CTRL:MMEN**.

In I2C Slave Mode, the device waits for an incoming connection. When the master starts a request to the slave address configured in **I2C:SADR**, the I2C unit acknowledges this request automatically. The application can configure an GPIO interrupt to detect activity on SCL or SDA to be informed about an incoming I2C transfer.

6.2.1 DMA Mode

In DMA mode, the Master can (read/write) access a designated address in the register space and/or SRAM of the RYZ012. The I2C module of the RYZ012 handles the read/write request from the I2C master automatically. However, it has to be noted, that the system clock should be at least 10x faster than I2C bit rate.

In DMA Mode, the master must first write the address to be read or written into the RYZ012. The address is three bytes long, by which the MSB is transmitted first. For a write operation, the data to be written can follow the address immediately. For read access, another start byte must be transmitted with read bit set. The received address is automatically offset by 0x800000. Therefore, if the address consists of the three bytes 0x04, 0x00 and 0xf0, the address accessed on the device is 0x8400f0. If bit **I2C:CTRL:AAINC** is set, consecutive memory address can be read or written without the need to send another address sequence. The figures below show I2C read and write transfers in DMA Mode for single bytes.

Figure 11. I2C DMA Mode Read Sequence

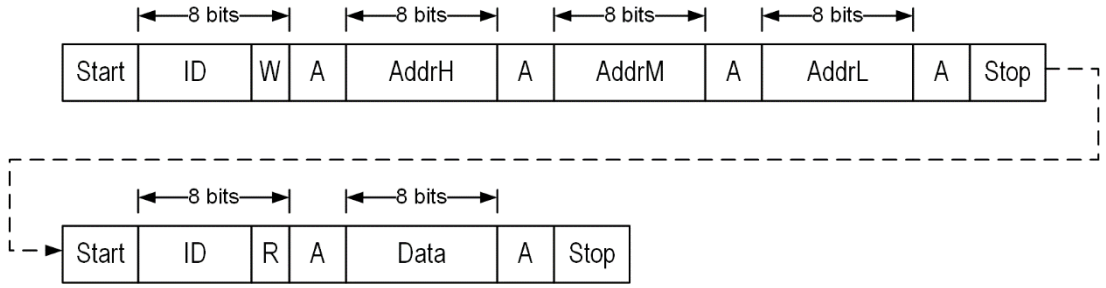


Figure 12. I2C DMA Mode Write Sequence

6.2.2 Mapping Mode

In Mapping mode, data I2C data access is limited to a user defined 128-byte buffer in SRAM. The buffer start address is configured in register **I2C:MMADR**. The lower 64 bytes buffer space is for written data and the other half is for data read by the master. Every new I2C data transfer following an I2C Stop Condition will reset the internal address counter to the start address of the read/write buffer. Register **I2C:LHADR** holds the offset of the last accessed byte of the previous transfer. This register is updated on a Stop Condition. Mapping mode is enabled by setting bit **I2C:CTRL:MMEN**. The figures below show I2C read and write transfers in Mapping Mode.

Figure 13. I2C Mapping Mode Read Sequence

Figure 14. I2C Mapping Mode Write Sequence

6.3 Master Mode

In Master Mode, the RYZ012 must provide the clock for I2C transfers. The clock speed is configured in register **I2C:CPRE**. The resulting I2C clock frequency is $F_{I2C} = F_{SYS} / (4 * \text{I2C:CPRE})$. I2C master transfers are configured in register **I2C:CYCTRL**. The single bits in this register allow inclusion or exclusion of certain stages of an I2C transfer. Register **I2C:MST** carries master status information.

6.3.1 Write Transfer

A full write transfer containing Start Condition, slave address byte followed by 3 bytes of data and a stop condition can be realized with the following sequence:

1. Set bit **I2C:CTRL:MSTREN** to enable master mode.
2. Write address of slave to be accessed into register **I2C:SADR**.
3. Write the three data bytes to registers **I2C:W1D**, **I2C:W2D** and **I2C:W3RD**, where **I2C:W1D** contains the first byte to be transmitted.
4. Write 0x3f to register **I2C:CYCTRL**.

The I2C hardware will carry out the whole transfer without further application interaction. The status of the transfer can be monitored in register **I2C:MST**.

Write transfers with more than 3 bytes can be implemented by leaving out the corresponding stages in **I2C:CYCTRL**.

6.3.2 Read Transfer

For read transfers in master mode **I2C:CYCTRL** is used similarly to write transfers. However, the RYZ012 has only one byte receive buffer which is **I2C:W3RD**. Therefore, read transfers have to be carried out byte by byte. In order to implement a full single byte read transfer including transmission of a Start Condition, slave address, acknowledge and a final stop byte, the master must execute the following sequence:

1. Set bit **I2C:CTRL:MSTREN** to enable master mode.
2. Write address of slave to be accessed into register **I2C:SADR**.
3. Write 0xf9 to register **I2C:CYCTRL**.
4. Wait for **I2C:MST:BSY** to be cleared.
5. Read data from register **I2C:W3RD**.

Read transfers with more than 1 byte can be implemented by disabling the corresponding stages in **I2C:CYCTRL**.

6.4 Notes on Concurrent I2C and SPI Usage

I2C hardware and SPI hardware modules on the RYZ012 share parts of the hardware; as a result, when both hardware interfaces are in use, I2C and SPI must not be operated in slave mode at the same time.

6.5 Register Reference

6.5.1 I2C:CPRE - I2C Clock Prescaler Configuration

Address: 0x0000
Reset: 0x1f

7	6	5	4	3	2	1	0
I2C:CPRE	CPRE						
	rw, 31						

7:0 **CPRE** I2C clock prescaler value

$F_{I2C} = F_{SYS} / (4 * CPRE)$

6.5.2 I2C:SADR - I2C Slave Address Configuration

Address: 0x0001
Reset: 0x5c

7	6	5	4	3	2	1	0
I2C:SADR	SADR						RSVD
	rw, 46						rw, 0

7:1 **SADR** Slave address

In master mode, this value serves as the remote device slave address,

In slave mode, this value is the address the I2C is accepting requests on.

6.5.3 I2C:MST - I2C Master Status

Address: 0x0002
Reset: 0x00

7	6	5	4	3	2	1	0
I2C:MST	RSVD				ACKSTAT	PBSY	BSY
	rw, 0				rw, 0	rw, 0	rw, 0

2 **ACKSTAT** Master acknowledge receive status

0: ACK Received

1: NACK Received

1 **PBSY** Master packet busy

0: Master packet idle

1: Master packet busy

0 **BSY** Master busy

0: I2C is idle

1: I2C is busy

6.5.4 I2C:CTRL - I2C General Control

Address: 0x0003
Reset: 0x01

	7	6	5	4	3	2	1	0
I2C:CTRL	RSVD				CSTREN	MMEN	MSTREN	AAINC
	rw, 0				rw, 0	rw, 0	rw, 0	rw, 1

3 **CSTREN** Clock Stretching Enable

0: Clock is controlled by the master

1: Clock line is held low to suspend the transmission

2 **MMEN** Mapping Mode enabled

0: Mapping Mode is disabled

1: Mapping Mode is enabled

1 **MSTREN** I2C Mast Mode enable

0: I2C is operating in Slave Mode

1: I2C is operating in Master Mode

0 **AAINC** Address Auto Increment enable

0: Address auto increment disabled

1: Address auto increment enabled

6.5.5 I2C:W1D - I2C Master Mode Write Buffer

Address: 0x0004
Reset: 0x5a

	7	6	5	4	3	2	1	0
I2C:W1D	W1D							
	rw, 90							

7:0 **W1D** Master mode write data buffer

6.5.6 I2C:W2D - I2C Master Mode Write Buffer

Address: 0x0005
Reset: 0xf1

	7	6	5	4	3	2	1	0
I2C:W2D	W2D							
	rw, 241							

7:0 **W2D** Master mode write data buffer

6.5.7 I2C:W3RD - I2C Master Mode Write/Read Buffer

Address: 0x0006
Reset: 0x00

	7	6	5	4	3	2	1	0
I2C:W3RD	W3RD							
	rw, 0							

7:0 **W3RD** Master mode read or write data buffer

6.5.8 I2C:CYCTRL - I2C Cycle Control

Address: 0x0007
Reset: 0x00

	7	6	5	4	3	2	1	0
I2C:CYCTRL	ACKEN	RDWR	STOPEN	STARTEN	W3RDEN	W2DEN	W1DEN	ADREN
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

7 **ACKEN** Enable ACK in read command

0: Do not acknowledge incoming data

1: Do acknowledge incoming data

6 **RDWR** Read / Write control

0: Send Write Bit (0) after Slave Address

1: Send Read Bit (1) after Slave Address

5 **STOPEN** Send Stop Condition at the end of cycle

0: Do not send Stop Bit after completion of all requested cycles

1: Send Stop Bit after completion of all requested cycles

4 **STARTEN** Send Start Condition at the beginning of cycle

0: Do not send start condition

1: Send Start Condition before requested cycles

3	**W3RDEN**	Receive data or Send data from W3RD **0:** Do not use W3RD **1:** Write Mode: Send Data from W3RD ReadMode: Read data into register W3RD
2	**W2DEN**	Send data from register W2D **0:** Don't use W2D **1:** Send Data from W2D
1	**W1DEN**	Send data from register W1D **0:** Do not use W1D **1:** Send Data from W1D
0	**ADREN**	Enable address transmission from SADR **0:** Do not send I2C address byte **1:** Send I2C address byte. The address is read from I2C:SADR, the read/write bit is taken from RDWR

6.5.9 I2C:LHADR - I2C Last Hold Address

Address: 0x00e0
Reset: 0x00

	7	6	5	4	3	2	1	0
I2C:LHADR	RSVD	ADR						
	r, 0	r, 0						

6:0	**ADR**	Contains the last called data address, which is only updated again after I2C-STOP

6.5.10 I2C:MMADR - I2C Mapping Mode Buffer Address

Address: 0x00e1
Reset: 0x80d700

	7	6	5	4	3	2	1	0
I2C:MMADR[2]	ADR							
	rw, 128							
I2C:MMADR[1]	ADR							
	rw, 215							
I2C:MMADR[0]	ADR							
	rw, 8388608							

23:0	**ADR**	Buffer address

6.5.11 I2C:HSTATE - I2C Host Status

Address: 0x00e4
Reset: 0x00

7	6	5	4	3	2	1	0
I2C:HSTATE	RSVD					RDY	INT
	rw, 0					rw, 0	rw, 0

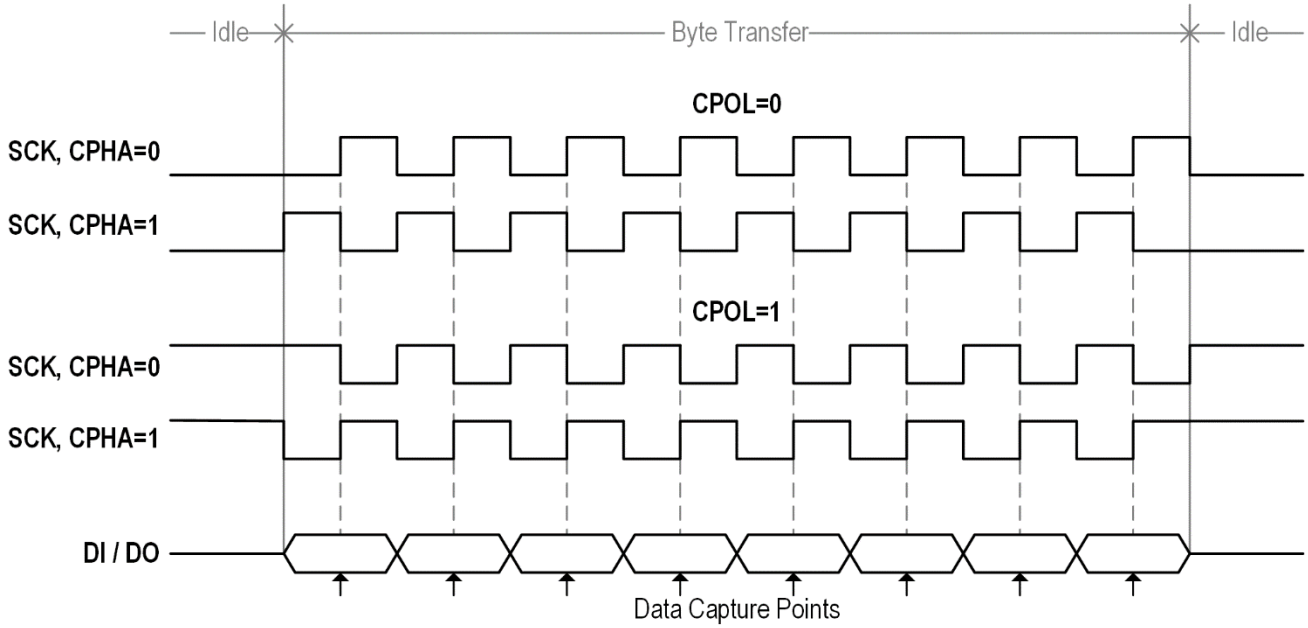
1	**RDY**	I2C ready indication **0:** The I2C host read operation is NOT complete **1:** The I2C host read operation is complete Write 1 to clear.
0	**INT**	I2C operation end indication **0:** No I2C operation end interrupt detected **1:** I2C operation end interrupt detected Write 1 to clear.

7. SPI Interface

The RYZ012 embeds a Serial Peripheral Interface (SPI)that can act as master or slave. SPI is a high-speed, full-duplex synchronous communication bus requiring four bus lines including a chip select (CS) line, a data input (DI) line, a data output (DO) line and a clock (CK) line.

The bits **CPOL** and **CPHA** in register **SPI:MODE** control SPI clock polarity and phase. The clock is low during idle periods, if **CPOL** is 0 or high otherwise. The **CPHA** bit controls whether data is sampled on the first or the second edge. A value of 0 results in sampling on the first clock edge, a value of 1 samples on the second edge. The figure below illustrates the timing behavior for all combinations of **CPOL** and **CPHA**. In Master Mode, all four combinations of **CPOL** and **CPHA** are supported. In Slave mode the two configurations where **CPOL**==**CPHA** are supported. In other words, data is always sampled on the rising clock in Slave Mode.

Figure 15. SPI Timing Diagram



7.1 SPI Master Mode

SPI for the RYZ012 supports both master mode and slave mode and acts as slave mode by default. To configure Master Mode, register **SPI:CTRL** must be set to the appropriate values. The bits **MSTREN** and **IOEN** must be set to 1 to enable master mode and activate the SPI GPIOs.

The SPI clock speed is configured in **SPI:CTRL:CPRE**. The resulting SPI clock frequency is $F_{SPI} = F_{SYS} / (2*(\text{SPI:CTRL:CPRE}+1))$.

Data transfers on the SPI bus are triggered by read or write access to the **SPI:DATA** register. Every time this register is read or written, the SPI clock pin generates 8 SPI clock cycles. Bit **SPI:CTRL:RDWR** controls whether data is read or written. On a write (**RDWR**=0), data written to the DATA register is sampled bitwise on the DO pin. On read (**RDWR**=1), data from the DI pin is sampled into the data register. **Note: SPI:CTRL:ODIS** must be cleared to enable data output.

Typically, the master controls the chip select (CS) signal to enable reception at the slave device. Bit **SPI:CTRL:CSN_EN** controls the status of the chip select signal. When this bit is set, the chip select output level is high (that is disabled).

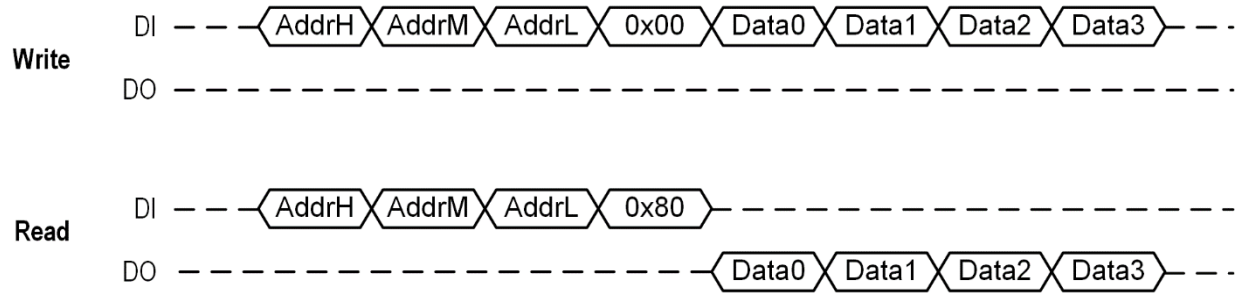
Bit **SPI:CTRL:BSY** can be used to monitor the transmission status.

7.2 SPI Slave Mode

Slave Mode SPI transfers must follow a communication scheme similar to I2C DMA mode. For each transfer, the master first sends four bytes of data. First it determines the memory address to be read or written; next a command byte, controlling read or write is sent. The address consists of three bytes AddrH, AddrM and AddrL. The address is offset by 0x800000 automatically by the SPI hardware. The command can be either 0x00 for Write or 0x80 for Read.

The bytes following the command byte are used to send or receive data from the RYZ012 SRAM or register space. Bit **SPI:CTRL:AAINC** determines whether the address received from the master is incremented automatically or not.

Figure 16. SPI Slave Mode Read and Write Transfers



7.3 Register Reference

7.3.1 SPI:DATA - SPI Data

Address: 0x0008
Reset: 0x00

	7	6	5	4	3	2	1	0
SPI:DATA	DATA							
	rw, 0							

7:0 **DATA** SPI data access

7.3.2 SPI:CTRL - SPI Control

Address: 0x0009
Reset: 0x0511

	7	6	5	4	3	2	1	0
SPI:CTRL[1]	IOEN	CPRE						
	rw, 0	rw, 5						
SPI:CTRL[0]	RSVD	BSY	SHREN	AAINC	RDWR	ODIS	MSTREN	CSN_EN
	rw, 0	rw, 0	rw, 0	rw, 1	rw, 0	rw, 0	rw, 0	rw, 1

15 **IOEN** SPI function mode, p_csn, p_scl, p_sda and p_sdo function as SPI if 1

0: No SPI functionality for specified port pins (p_csn, p_scl, p_sda and p_sdo)

1: SPI functionality for specified port pins (p_csn, p_scl, p_sda and p_sdo)

14:8	**CPRE**	SPI clock prescaler $F_{SPI} = F_{SYS} / (2 * (CPRE + 1))$
6	**BSY**	Busy status **0:** SPI is ready for next operation **1:** SPI has not completed transmission of 8 clock pulses
5	**SHREN**	DI/DO share enable **0:** SPI uses separate DI and DO pin **1:** DI and DO share one common pin
4	**AAINC**	Enable address auto increase **0:** Disables automatic address incrementing **1:** Enables automatic address incrementing
3	**RDWR**	Command direction control **0:** Write to DO pin **1:** Read from DI pin
2	**ODIS**	Data Output Disable **0:** Data in $RReg(SPI,DATA) is ignored **1:** Data in $RReg(SPI,DATA) is shifted out on DO
1	**MSTREN**	Master Mode enable **0:** SPI operates in Slave Mode **1:** SPI operates in Master Mode
0	**CSN_EN**	Chip Select signal control **0:** Chip select enabled **1:** Chip select disabled

7.3.3 SPI:MODE - SPI Mode Configuration

Address: 0x000b
Reset: 0x00

7	6	5	4	3	2	1	0
SPI:MODE	RSVD					CPHA	CPOL
	rw, 0					w, 0	rw, 0

1	**CPHA**	SPI clock phase **0:** Data is sampled on first edge of clock period **1:** Data is sampled on second edge of clock period

0	**CPOL**	SPI clock polarity **0:** Clock line is low when idle **1:** Clock line is high when idle

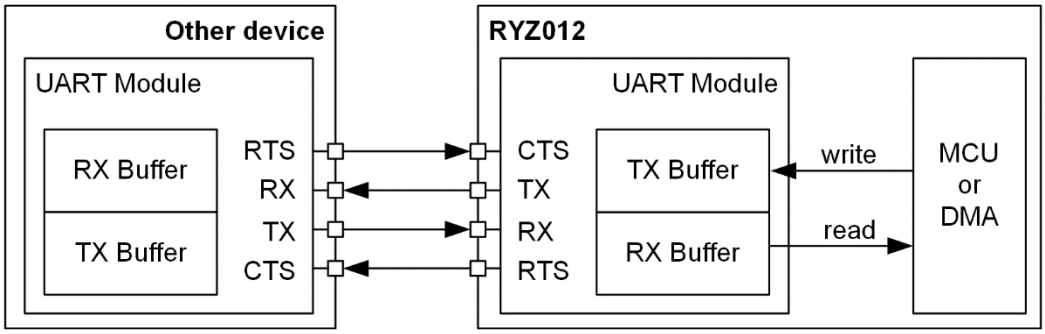
8. UART Interface

The RYZ012 embeds UART (Universal Asynchronous Receiver/Transmitter) to implement full-duplex transmission and reception through UART TX and RX interface. Both TX and RX interface are 4-layer FIFO (First In First Out) interface.

Hardware flow control is supported through RTS and CTS.

The UART module also supports ISO7816 protocol to enable communication with ISO/IEC 7816 integrated circuit card, especially smart card. In this mode, half-duplex communication (transmission or reception) is supported through the shared 7816_TRX interface.

Figure 17. UART Communication



Data sent is first written into the TX buffer by MCU or DMA; next UART module transmits the data from the TX buffer to the other device through pin TX. Data received through the pin RX is first written to the RX buffer; next the data is read by MCU or DMA.

If the RX buffer of the RYZ012 UART is close to full, the RYZ012 sends a signal (configurable high or low level) through pin RTS to inform the other device that it should stop sending data. Similarly, if the RYZ012 receives a signal from pin CTS, it indicates that the RX buffer of the other device is close to full and that the RYZ012 should stop sending data.

UART:DATA serve to write data into TX buffer or read data from RX buffer.

UART:CLKDIV serve to configure UART clock.

UART:CTRL serves to set baud rate (**BRC**), enable RX/TX DMA mode (**DMARX** / **DMATX**), and enable RX/TX interrupt (**DMARX** / **DMATX**).

UART:CTRL:CTSEN should be set to 1b'1 to enable CTS. **UART:CTRL:CTSI** serves to configure the CTS signal level. **UART:CTRL:PAREN** serves to enable parity bit, and **UART:CTRL:PARMODE** selects even/odd parity. **UART:CTRL:STOP** serve to select 1/1.5/2 bits for stop bit. **UART:CTRL:TTL** serves to configure whether RX/TX level should be inverted.

UART:CTRL:RTSEN serves to enable RTS, and **UART:CTRL:RTSTRIG** configures the RTS signal level.

UART:CTRL:RXTRIG and **UART:CTRL:TXTRIG** serves to configure the number of bytes in the RX/TX buffer to trigger interrupt.

The number of bytes in RX/TX buffer can be read from **UART:BUFCNT**.

8.1 Register Reference

8.1.1 UART:DATA - UART Data Buffer

Address: 0x0090
Reset: 0x00000000

	7	6	5	4	3	2	1	0
UART:DATA[3]	DAT3							
	rw, 0							
UART:DATA[2]	DAT2							
	rw, 0							
UART:DATA[1]	DAT1							
	rw, 0							
UART:DATA[0]	DAT0							
	rw, 0							

7:0, 15:8, 23:16, 31:24	**DATx**	UART Data Buffer Read/Write Data buffer to corresponding byte

8.1.2 UART:CLKDIV - UART Clock Divider Configuration

Address: 0x0094
Reset: 0x0fff

	7	6	5	4	3	2	1	0
UART:CLKDIV[1]	DIVEN	DIV						
	rw, 0	rw, 15						
UART:CLKDIV[0]	DIV							
	rw, 255							

15	**DIVEN**	Enable UART clock divider **0:** Disables clock divider **1:** Enables clock divider
14:0	**DIV**	Clock divider $F_{UART} = F_{SYS} / (DIV + 1)$

8.1.3 UART:CTRL - UART Control

Address: 0x0096
Reset: 0x00a50e0f

	7	6	5	4	3	2	1	0
UART:CTRL[3]	TXTRIG				RXTRIG			
	rw, 0				rw, 0			
UART:CTRL[2]	RTSEN	RTSMEN	RTSMVAL	RTSPAR	RTSTRIG			
	rw, 1	rw, 0	rw, 1	rw, 0	rw, 5			
UART:CTRL[1]	LBEN	TTL	STOP		PARMODE	PAREN	CTSEN	CTSI
	rw, 0	rw, 0	rw, 0		rw, 1	rw, 1	rw, 1	rw, 0
UART:CTRL[0]	INTTX	INTRX	DMATX	DMARX	BRC			
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 15			

31:28 **TXTRIG** TX interrupt trigger byte count

Number of occupied transmit buffer bytes that trigger an interrupt

27:24 **RXTRIG** RX interrupt trigger byte count

Number of occupied receive buffer bytes that trigger an interrupt

23 **RTSEN** Enable RTS

0: Disables RTS signal generation

1: Enables RTS signal generation

22 **RTSMEN** Enable RTS manual mode

0: Disables RTS manual configuration

1: Enables RTS manual configuration

21 **RTSMVAL** RTS manual signal level

0: Set RTS signal to LOW level

1: Set RTS signal to HIGH level

20 **RTSPAR** Enable RTS Parity

0: Disables RTS parity

1: Enables RTS parity

19:16 **RTSTRIG** RTS trigger byte count

Number of occupied receive buffer bytes that triggers an RTS signal

15 **LBEN** Enable Loopback

0: Disables RX/TX loopback routing

1: Enables RX/TX loopback routing

14 **TTL** TTL logic level configuration

0: Disables the inversion of the RX/TX logic level

1: Enables the inversion of the RX/TX logic level

13:12	**STOP**	Stop bit configuration **00:** 1 bit stop signal generation **01:** 1.5 bit stop signal generation **1x:** 2 bit stop signal generation
11	**PARMODE**	Parity mode configuration **0:** Configure Even-Parity **1:** Configure Odd-Parity
10	**PAREN**	Enable Parity **0:** Disables parity bit generation **1:** Enables parity bit generation
9	**CTSEN**	Enable CTS **0:** Disables the CTS signal processing **1:** Enables the CTS signal processing
8	**CTSI**	CTS signal inverter **0:** The CTS input will be configured as LOW-active **1:** The CTS input will be configured as HIGH-active
7	**INTTX**	Enable TX interrupt **0:** Disables TX interrupt **1:** Enables TX interrupt
6	**INTRX**	Enable RX interrupt **0:** Disables RX interrupt **1:** Enables RX interrupt
5	**DMATX**	Enable DMA data processing for sending data (TX) **0:** Disables TX-DMA data processing **1:** Enables TX-DMA data processing
4	**DMARX**	Enable DMA data processing for receiving data (RX) **0:** Disables RX-DMA data processing **1:** Enables RX-DMA data processing
3:0	**BRC**	Baudrate selection BRC should be larger than 2 Baud rate = F_{UART} / (BRC + 1)

8.1.4 UART:RXTIMEOUT - UART RX Timeout Configuration

Address: 0x009a
Reset: 0x01c0

	7	6	5	4	3	2	1	0
UART:RXTIMEOUT[1]	MASKERR	MASKDONE	7816EN	RSVD			TOV	
	rw, 0	rw, 0	rw, 0	rw, 0			rw, 1	

	7	6	5	4	3	2	1	0
UART:RXTIMEOUT[0]	TOV							
	rw, 192							

15 **MASKERR** Enable mask error indication

0: Disables mask error indication

1: Enables mask error indication

14 **MASKDONE** Enable mask done indication

0: Disables mask done indication

1: Enables mask done indication

13 **7816EN** Enable ISO7816 UART standard

0: Disables ISO7816 UART

1: Enables ISO7816 UART

9:0 **TOV** Timeout Value

Number of UART clock cycles required for one transaction.

This value should be computed as TOV=(BRC+1)*(bits per byte)*(transaction byte count).

8.1.5 UART:BUFCNT - UART Buffer Count

Address: 0x009c
Reset: 0x00

	7	6	5	4	3	2	1	0
UART:BUFCNT	TXCNT				RXCNT			
	r, 0				r, 0			

7:4 **TXCNT** Current number of bytes in TX buffer

3:0 **RXCNT** Current number of bytes in RX buffer

8.1.6 UART:STATUS - UART Status

Address: 0x009d
Reset: 0x00

	7	6	5 4	3	2 1 0
UART:STATUS	RXERR	TXERR	RSVD	IRQ	RSVD
	r, 0	r, 0	r, 0	r, 0	r, 0

7 **RXERR** RX mask error indication

0: No RX mask error detected

1: RX mask error detected

Write 1 to clear.

6 **TXERR** TX mask error indication

0: No TX mask error detected

1: TX mask error detected

Write 1 to clear.

3 **IRQ** RX/TX interrupt indication

0: No RX/TX interrupt detected

1: RX/TX buffer interrupt detected

8.1.7 UART:TXRX_STATUS - UART RX/TX Status

Address: 0x009e
Reset: 0x00

	7 6 5 4	3	2	1	0
UART:TXRX_STATUS	RSVD	RXBUFIRQ	RXDONE	TXBUFIRQ	TXDONE
	r, 0	r, 0	r, 0	r, 0	r, 0

3 **RXBUFIRQ** RX buffer interrupt indication

0: No RX buffer interrupt detected

1: RX buffer interrupt detected

2 **RXDONE** RX mask done indication

0: No RX mask done detected

1: RX mask done detected

1 **TXBUFIRQ** TX buffer interrupt indication

0: No TX buffer interrupt detected

1: TX buffer interrupt detected

0	**TXDONE**	TX mask done indication **0:** No TX mask done detected **1:** TX mask done detected

8.1.8 UART:STATE - UART State

Address: 0x009f
Reset: 0x00

7	6	5	4	3	2	1	0
UART:STATE	RSTATE			RSVD	TSTATE		
	r, 0			r, 0	r, 0		

7:4	**RSTATE**	[7:4] rstate_i
2:0	**TSTATE**	[2:0] tstate_i

9. Single Wire Interface

The RYZ012 supports Single Wire interface. SWM (Single Wire Master) and SWS (Single Wire Slave) represent the master and slave device of the single wire communication system. The maximum data rate can be up to 2Mbps.

The SWIRE interface is used for device programming and debugging.

10. Timers

10.1 General-Purpose Timers Timer 0 - Timer 2

The RYZ012 supports three timers: Timer 0 – Timer 2. The three timers all support four modes: Mode 0 (System Clock Mode), Mode 1 (GPIO Trigger Mode), Mode 2 (GPIO Pulse Width Mode) and Mode 3 (Tick Mode), which are selectable through **TIMER:CTRL:MODE0** to **TIMER:CTRL:MODE2** to the corresponding Timer.

Timer2 can also be configured as watchdog to monitor proper firmware execution.

10.1.1 Mode 0 (System Clock Mode)

In Mode 0, the system clock is employed as clock source.
After the timer is enabled, Timer Tick (that is counting value) is increased by 1 on each positive edge of system clock. Generally, the initial Tick value should be set to 0.

When the current Timer Tick value matches the preset Timer Capture, an interrupt is generated, the timer stops counting, and the timer status is updated.

10.1.1.1 Timer 0 Mode 0 Configuration Example

1. Set the initial Tick Value of Timer 0 through **TIMER:TICK0**. It is recommended to clear initial Timer Tick value to 0.
2. Set the Capture Value of Timer 0 through **TIMER:CAPT0**.
3. Set TIMER:CTRL:MODE0 to 2b'00 to select Mode 0. Meanwhile set TIMER:CTRL:EN0 to 1b'1 to enable Timer0.

Timer 0 starts counting upward, and Tick value is increased by 1 on each positive edge of system clock until it reaches Timer0 Capture value.

10.1.2 Mode 1 (GPIO Trigger Mode)

In Mode 1, GPIO is employed as clock source. The registers **GPIOx:T0G2R**, **GPIOx:T1G2R** or **GPIOx:T2** specify the GPIO that generates the counting signal for Timer 0, Timer 1 and Timer2, respectively.

When the timer is enabled, Timer Tick (that is counting value) is increased by 1 on each positive/negative (configurable) edge of GPIO. Generally, the initial Tick value should be set to 0. The **GPIOx:INTPOL** register specifies the GPIO edge when Timer Tick counting increases. See **GPIO to Timer and Interrupt Mapping** for GPIO to timer mapping.

Once current Timer Tick value matches the preset Timer Capture (that is timing value), an interrupt is generated and timer stops counting.

10.1.2.1 Timer 1 Mode 1 Configuration Example

1. Set initial Tick value of Timer1 through **TIMER:TICK1**. It is recommended to clear initial Timer Tick value to 0.
2. Set the Capture Value of Timer 1 through **TIMER:CAPT1**.
3. Select GPIO source and edge for Timer1 through registers **GPIOx:T1G2R** and **GPIOx:INTPOL**.
4. Set Timer 1 to Mode 1 and enable Timer 1 by setting **TIMER:CTRL:MODE1** to 2b'01 and **TIMER:CTRL:EN1** to 1b'1.

Timer 1 starts counting upward, and Timer1 Tick value is increased by 1 on each positive/negative (specified during the 3rd step) edge of GPIO until it reaches Timer1 Capture value.

10.1.3 Mode 2 (GPIO Pulse Width Mode)

In Mode 2, system clock is employed as clock source to measure the width of GPIO pulse. The registers **GPIOx:T0G2R**, **GPIOx:T1G2R** or **GPIOx:T2** specify the GPIO that generates the control signals for Timer 0, Timer 1 and Timer 2, respectively.

When the Timer is enabled, Timer Tick is triggered by a positive/negative (configurable) edge of GPIO pulse. Then Timer Tick (that is counting value) is increased by 1 on each positive edge of system clock. Generally, the initial Tick value should be set to 0. The **GPIOx:INTPOL** register specifies the GPIO edge when Timer Tick starts counting. See **GPIO to Timer and Interrupt Mapping** for GPIO to timer mapping.

When a negative/positive edge of GPIO pulse is detected, an interrupt is generated and timer stops counting. The GPIO pulse width could be calculated in terms of tick count and period of system clock.

10.1.3.1 Timer 2 Mode 2 Configuration Example

1. Set initial Timer 2 Tick value through **TIMER:TICK2**. It is recommended to clear initial Timer Tick value to 0.
2. Select GPIO source and edge for Timer 2 through registers **GPIOx:T2** and **GPIOx:INTPOL**.
3. Set Timer 2 to Mode 2 and enable Timer 2 by setting **TIMER:CTRL:MODE2** to 2b'10 and **TIMER:CTRL:EN2** to 1b'1.

Timer 2 Tick is triggered by a positive/negative (specified during the 2nd step) edge of GPIO pulse. Timer 2 starts counting upward and its Tick value is increased by 1 on each positive edge of system clock.

When a negative/positive edge of GPIO pulse is detected, an interrupt is generated and Timer 2 stops counting.

The length of the GPIO pulse is determined as the system clock period time multiplied with the value read from register **TIMER:TICK2**.

10.1.4 Mode 3 (Tick Mode)

In Mode 3, the system clock is employed as clock source. When the Timer is enabled, Timer Tick starts counting upward, and Timer Tick value is increased by 1 on each positive edge of system clock.

This mode can be used as time indicator. There will be no interrupt generated. Timer Tick keeps rolling from 0 to 0xffffffff. When Timer tick overflows, it returns to 0 and starts counting upward again.

10.1.4.1 Timer 0 Mode 3 Configuration Example

1. Set initial Timer 0 Tick value through **TIMER:TICK0**. It is recommended to clear initial Timer Tick value to 0.
2. Set Timer 0 to Mode 3 and enable Timer 0 by setting **TIMER:CTRL:MODE0** to 2b'11 and **TIMER:CTRL:EN0** to 1b'1.

Timer0 Tick starts to roll. The Timer 0 Tick Value can be read any time from **TIMER:TICK0**.

10.1.5 Watchdog

The programmable watchdog can reset the module from unexpected hang up or malfunction. The watchdog functionality is only supported by Timer 2.

The watchdog is triggered when the 14 bit Watchdog Capture Value **TIMER:CTRL:WDCAPT** match the upper 14 bits (that is bits 31:18) of the Timer 2 Tick Value. When the watchdog is triggered, the chip is reset.

10.1.5.1 Watchdog Timer Configuration Example

1. Clear Timer 2 Tick value by setting **TIMER:TICK2** to zero.
2. Configure the Watchdog Capture value **TIMER:CTRL:WDCAPT** to the appropriate timeout value and enable the watchdog by setting **TIMER:CTRL:WDEN** to 1b'1.
3. Enable Timer 2 by setting **TIMER:CTRL:EN2** to 1b'1.
4. Periodically reset Timer 2 Tick value before reaching the Watchdog Capture value.

When enabled, Timer 2 starts counting. The periodical reset of the Tick Value prevents the timer from reaching the Watchdog Capture value. If the reset is not executed due to an application malfunction or deadlock, the counter reaches the Watchdog Capture value and the module resets. The user can read the watchdog status bit **SCTL:SSTATUS:WD_STATE** to check whether the reset was due to a watchdog reset or not.

10.2 32K LTIMER

The RYZ012 also supports a low frequency (32kHz) LTIMER in Suspend, Deep Sleep or Standby Mode. This timer can be used as one kind of wakeup source.

10.3 Register Reference

10.3.1 TIMER:CTRL - Timer Control

Address: 0x0620
Reset: 0x000000

	7	6	5	4	3	2	1	0
TIMER:CTRL[2]	WDEN	WDCAPT						
	rw1, 0	rw, 0						
TIMER:CTRL[1]	WDCAPT							MODE2
	rw, 0							rw, 0
TIMER:CTRL[0]	MODE2	EN2	MODE1		EN1	MODE0		EN0
	rw, 0	rw, 0	rw, 0		rw, 0	rw, 0		rw, 0

23	**WDEN**	Watchdog enable **0:** Disables Watchdog capture **1:** Enables Watchdog capture
22:9	**WDCAPT**	Watchdog capture value
8:7	**MODE2**	Timer 2 mode selection Last significant bit of MODE2 **00:** Using SCLK **01:** Using GPIO **10:** Count width of GPI **11:** Timer ticks
6	**EN2**	Timer 2 enable **0:** Disables Timer 2 **1:** Enables Timer 2
5:4	**MODE1**	Timer 1 mode selection **00:** Using SCLK **01:** Using GPIO **10:** Count width of GPI **11:** Timer ticks
3	**EN1**	Timer 1 enable **0:** Disables Timer 1 **1:** Enables Timer 1

2:1	**MODE0**	Timer 0 mode selection **00:** Using SCLK **01:** Using GPIO **10:** Count width of GPI **11:** Timer ticks
0	**EN0**	Timer 0 enable **0:** Disables Timer 0 **1:** Enables Timer 0

10.3.2 TIMER:STATUS - Timer Status

Address: 0x0623
Reset: 0x00

	7	6	5	4	3	2	1	0
TIMER:STATUS	RSVD				TS2	TS1	TS0	RSVD
	rw, 0				rw1, 0	rw1, 0	rw1, 0	rw, 0

3	**TS2**	Timer 2 status **0:** Timer 2 did not trigger **1:** Timer 2 triggered Write 1 to clear.
2	**TS1**	Timer 1 status **0:** Timer 1 did not trigger **1:** Timer 1 triggered Write 1 to clear.
1	**TS0**	Timer 0 status **0:** Timer 0 did not trigger **1:** Timer 0 triggered Write 1 to clear.

10.3.3 TIMER:CAPT0 - Timer 0 Capture

Address: 0x0624
Reset: 0x00000000

	7	6	5	4	3	2	1	0
TIMER:CAPT0[3]	CAPT0							
	rw, 0							
TIMER:CAPT0[2]	CAPT0							
	rw, 0							
TIMER:CAPT0[1]	CAPT0							
	rw, 0							
TIMER:CAPT0[0]	CAPT0							
	rw, 0							

31:0 **CAPT0** Timer 0 Capture Value

10.3.4 TIMER:CAPT1 - Timer 1 Capture

Address: 0x0628
Reset: 0x00000000

	7	6	5	4	3	2	1	0
TIMER:CAPT1[3]	CAPT1							
	rw, 0							
TIMER:CAPT1[2]	CAPT1							
	rw, 0							
TIMER:CAPT1[1]	CAPT1							
	rw, 0							
TIMER:CAPT1[0]	CAPT1							
	rw, 0							

31:0 **CAPT1** Timer 1 Capture Value

10.3.5 TIMER:CAPT2 - Timer 2 Capture

Address: 0x062c
Reset: 0x00000000

	7	6	5	4	3	2	1	0
TIMER:CAPT2[3]	CAPT2							
	rw, 0							
TIMER:CAPT2[2]	CAPT2							
	rw, 0							
TIMER:CAPT2[1]	CAPT2							
	rw, 0							
TIMER:CAPT2[0]	CAPT2							
	rw, 0							

31:0 **CAPT2** Timer 2 Capture Value

10.3.6 TIMER:TICK0 - Timer 0 Tick Counter

Address: 0x0630
Reset: 0x00000000

	7	6	5	4	3	2	1	0
TIMER:TICK0[3]	TICK0							
	rw, 0							
TIMER:TICK0[2]	TICK0							
	rw, 0							
TIMER:TICK0[1]	TICK0							
	rw, 0							
TIMER:TICK0[0]	TICK0							
	rw, 0							

31:0 **TICK0** Timer 0 Counter Value

10.3.7 TIMER:TICK1 - Timer 1 Tick Counter

Address: 0x0634
Reset: 0x00000000

7	6	5	4	3	2	1	0
TIMER:TICK1[3]	TICK1						
	rw, 0						
TIMER:TICK1[2]	TICK1						
	rw, 0						
TIMER:TICK1[1]	TICK1						
	rw, 0						
TIMER:TICK1[0]	TICK1						
	rw, 0						

31:0 **TICK1** Timer 1 Counter Value

10.3.8 TIMER:TICK2 - Timer 2 Tick Counter

Address: 0x0638
Reset: 0x00000000

7	6	5	4	3	2	1	0
TIMER:TICK2[3]	TICK2						
	rw, 0						
TIMER:TICK2[2]	TICK2						
	rw, 0						
TIMER:TICK2[1]	TICK2						
	rw, 0						
TIMER:TICK2[0]	TICK2						
	rw, 0						

31:0 **TICK2** Timer 2 Counter Value

10.4 System Timer

The RYZ012 also supports a System Timer.
As introduced in **System Timer Clock** the clock frequency for System Timer is fixed as 16MHz irrespective of system clock.
In suspend mode, both System Timer and Timer 0–Timer 2 stop counting, and 32K Timer starts counting. When the chip restores to active mode, Timer 0–Timer 2 continue counting from the number at which they stopped; In contrast, System Timer continues counting from an adjusted number which is a sum of the number when it stops and an offset calculated from the counting value of 32K Timer during Suspend Mode.

10.5 Register Reference

10.5.1 SYSTIM:CNT - System Timer Counter Value

Address: 0x0740
Reset: 0x00

	7	6	5	4	3	2	1	0
SYSTIM:CNT[3]	CNT							
	rw, 0							
SYSTIM:CNT[2]	CNT							
	rw, 0							
SYSTIM:CNT[1]	CNT							
	rw, 0							
SYSTIM:CNT[0]	CNT						RSVD	
	rw, 0						rw, 0	

31:3 **CNT** This is the System Timer counter value. Write to set initial value.

10.5.2 SYSTIM:CTRL - System Timer Control

Address: 0x074c
Reset: 0x0090

	7	6	5	4	3	2	1	0
SYSTIM:CTRL[1]	RSVD							
	rw, 0							
SYSTIM:CTRL[0]	RSVD						IRQEN	RSVD
	rw, 36						rw, 0	rw, 0

1 **IRQEN** System Timer Interrupt Enable

0: Disables System timer interrupt.

1: Enables System timer interrupt.

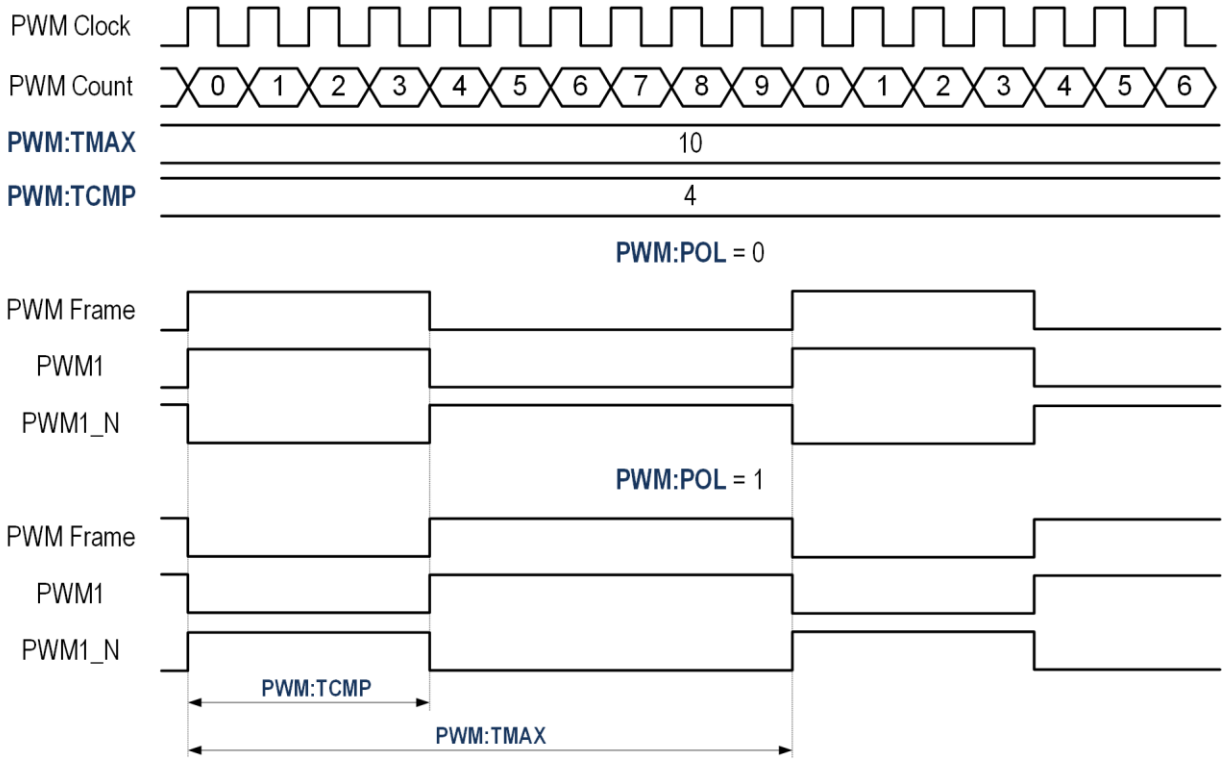
11. PWM

The RYZ012 has six Pulse-Width-Modulation (PWM) channels. Each PWM has separate direct (non-inverted) outputs named PWMx. In addition, for channels 0-2 and 4, inverted outputs named PWMxN are available.

The PWM clock derives from the system clock. **PWM:CLKDIV** serves as frequency divider for the PWM clock, such that $F_{PWM} = F_{SYS} / (\text{PWM:CLKDIV}+1)$.

Each PWM channel has an independent counter which counts from 0 to **PWM:TMAXx**. As long as the counter value is below **PWM:TCMPx**, a high level output is generated; afterwards, a low level output is generated on the corresponding direct pin until the counter reaches **PWM:TMAXx**. The polarity of the generated signal can be inverted through register **PWM:POL** independently for each channel. In addition, the polarity of the direct output and the inverted output can be controlled through registers **PWM:DPOL** and **PWM:IPOL**, respectively.

Figure 18. PWM, PWM Output Generation



The individual PWM channels are enabled through register **PWM:EN**. When the PWM is disabled, the corresponding output turns low immediately. An interruption will be generated at the end of each signal frame if enabled through bit 2 to 7 of **PWM:MASK0**.

11.1 PWM Modes

PWM0 supports three modes, including Continuous, Counting, and IR Mode. PWM1–PWM5 only support Continuous Mode. The register **PWM:MODE** serves to select PWM0 mode.

11.1.1 Continuous Mode

Continuous Mode is supported by all PWM channels. In this mode, the PWM continuously sends out signal frames. The frequency and duty cycle of the generated waveform can be changed freely through registers **PWM:TMAXx** and **PWM:TCMPx**. Changes to these registers will take effect in the next signal frame.

After completion of a signal frame, the corresponding PWM cycle done interrupt flag **PWM:INT0:FRx** is set. If the interrupt is enabled in register **PWM:MASK0**, an interrupt request is sent to the interrupt controller. The user needs to write 1b'1 to the flag bit to manually clear it.

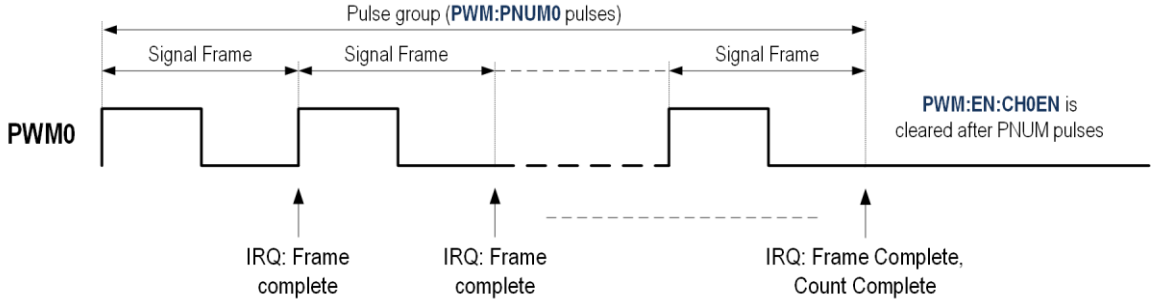
11.1.2 Counting Mode

Only PWM0 supports Counting mode. **PWM:MODE:MODE** should be set as 4b'0001 to select PWM0 counting mode. In this mode, PWM0 sends out specified number of signal frames which are defined as a pulse group. The number is configured through register **PWM:PNUM0**.

After completion of each signal frame, the cycle done interrupt flag (**PWM:INT0:FR0**) is set. If the interrupt is enabled in register **PWM:MASK0:FR0**, an interrupt request is sent to the interrupt controller. The interrupt flag is cleared by writing 1b'1 to it.

After completion of the pulse group, PWM0 is disabled automatically, and the interrupt flag **PWM:INT0:CNT0** is set. If the interrupt is enabled in register **PWM:MASK0:CNT0**, an interrupt request is sent to the interrupt controller. The interrupt flag is cleared by writing 1b'1 to it.

Figure 19. Counting Mode



Counting mode also serves to stop IR mode gracefully. See **IR Mode** for details.

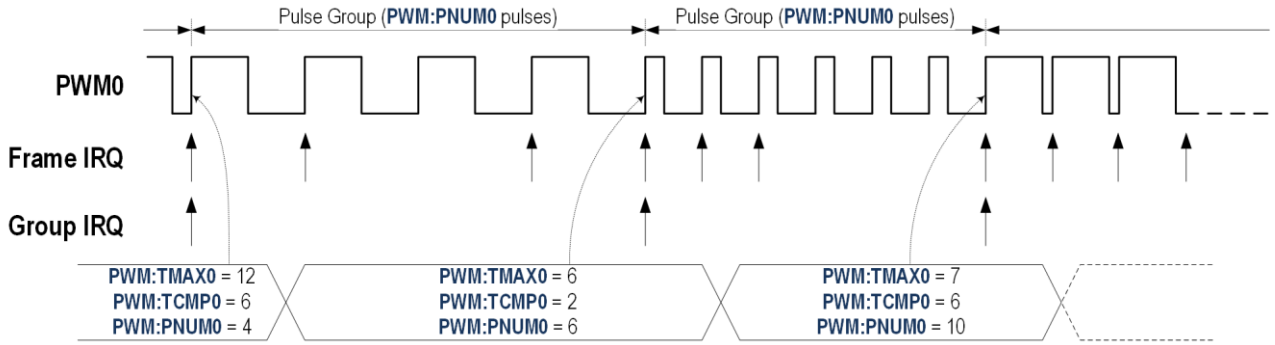
11.1.3 IR Mode

Only PWM0 supports IR mode. **PWM:MODE:MODE** should be set as 4b'0011 to select PWM0 IR mode. IR Mode is similar to Counting Mode with the difference that pulse groups are sent continuously.

During IR mode, PWM0 output waveform can be changed freely through **PWM:TCMP0**, **PWM:TMAX0**, and **PWM:PNUM0**. The new configuration of these registers takes effect in the next pulse group.

To stop IR mode and complete the current pulse group, the user can switch PWM0 from IR mode to Counting mode so that PWM0 stops after the current pulse group is finished. If PWM0 is disabled directly through **PWM:EN:CH0EN**, PWM0 output turns Low immediately despite of the current pulse group. After completion of each frame and pulse group, the corresponding interrupt flags **PWM:INT0:FR0** and **PWM:INT0:CNT0** are set. If the corresponding interrupt is enabled in register **PWM:MASK0**, an interrupt request is sent to the interrupt controller. The interrupt flags are cleared by writing 1b'1 to them.

Figure 20. IR Mode



11.2 Register Reference

11.2.1 PWM:EN - PWM Enable

Address: 0x0780
Reset: 0x0000

	7	6	5	4	3	2	1	0
PWM:EN[1]	RSVD							CH0EN
	rw, 0							rw, 0
PWM:EN[0]	RSVD		CH5EN	CH4EN	CH3EN	CH2EN	CH1EN	RSVD
	rw, 0		rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

8 **CH0EN** Enable PWM0

0: Disables PWM0

1: Enables PWM0

5 **CH5EN** Enable PWM5

0: Disables PWM5

1: Enables PWM5

4 **CH4EN** Enable PWM4

0: Disables PWM4

1: Enables PWM4

3 **CH3EN** Enable PWM3

0: Disables PWM3

1: Enables PWM3

2 **CH2EN** Enable PWM2

0: Disables PWM2

1: Enables PWM2

1 **CH1EN** Enable PWM1

0: Disables PWM1

1: Enables PWM1

11.2.2 PWM:CLKDIV - PWM Clock Divider Configuration

Address: 0x0782
Reset: 0x00

	7	6	5	4	3	2	1	0
PWM:CLKDIV	DIV							
	rw, 0							

7:0 **DIV** Select PWM Clock divider

$F_{PWM} = F_{SYS} / (CLKDIV + 1)$

11.2.3 PWM:MODE - PWM Mode

Address: 0x0783
Reset: 0x00

	7	6	5	4	3	2	1	0
PWM:MODE	RSVD				MODE			
	rw, 0				rw, 0			

3:0 **MODE** PWM0 mode selection

0000: Select PWM0 Continuous Mode

0001: Select PWM0 Counting Mode

0011: Select PWM0 IR Mode

0111: Select PWM0 IR FIFO Mode

1111: Select PWM0 IR DMA FIFO Mode

11.2.4 PWM:DPOL - PWMx Pin Output Inversion

Address: 0x0784
Reset: 0x00

	7	6	5	4	3	2	1	0
PWM:DPOL	RSVD		DPOL5	DPOL4	DPOL3	DPOL2	DPOL1	DPOL0
	rw, 0		rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5 **DPOLx** Configures the output polarity of the corresponding direct PWM output pin (PWMx)

0: PWMx is not inverted

1: PWMx is inverted

11.2.5 PWM:IPOL - PWMx_N Pin Output Inversion

Address: 0x0785
Reset: 0x00

	7	6	5	4	3	2	1	0
PWM:IPOL	RSVD		IPOL5	IPOL4	IPOL3	IPOL2	IPOL1	IPOL0
	rw, 0		rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5	**IPOLx**	Configures the output polarity of the corresponding inverted PWM output pin (PWMx_N) **0:** PWMx_N is not inverted **1:** PWMx_N is inverted

11.2.6 PWM:POL - PWM Polarity

Address: 0x0786
Reset: 0x00

	7	6	5	4	3	2	1	0
PWM:POL	RSVD		POL5	POL4	POL3	POL2	POL1	POL0
	rw, 0		rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

0, 1, 2, 3, 4, 5	**POLx**	Configures the PWM frame polarity **0:** Frame starts with high level **1:** Frame starts with low level

11.2.7 PWM:TCMP0 - PWM0 Capture Mode Time

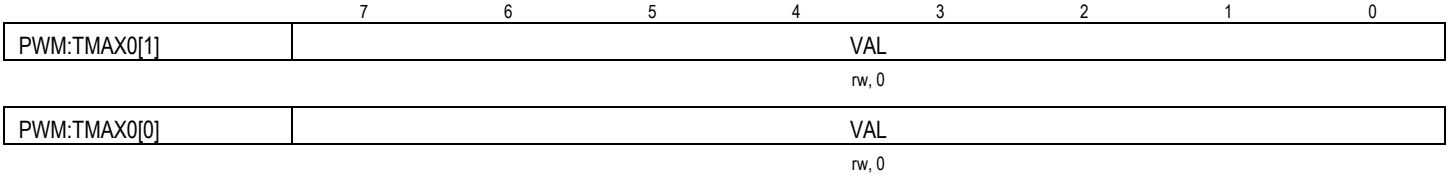
Address: 0x0794
Reset: 0x0000

	7	6	5	4	3	2	1	0
PWM:TCMP0[1]	VAL							
	rw, 0							
PWM:TCMP0[0]	VAL							
	rw, 0							

15:0	**VAL**	PWM0 high time or low time value

11.2.8 PWM:TMAX0 - PWM0 Maximum Cycle Time

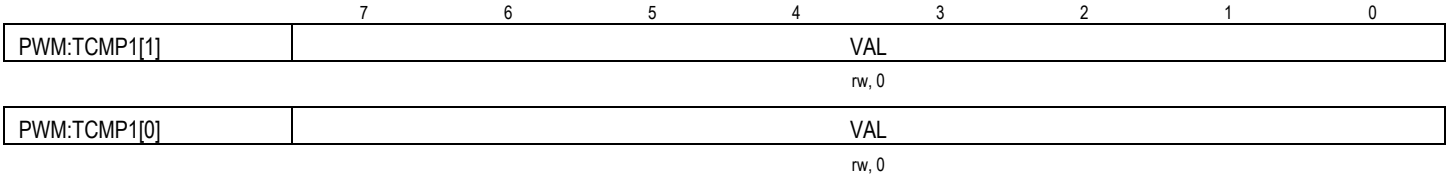
Address: 0x0796
Reset: 0x0000



15:0 **VAL** PWM0 cycle time value

11.2.9 PWM:TCMP1 - PWM1 Capture Mode Time

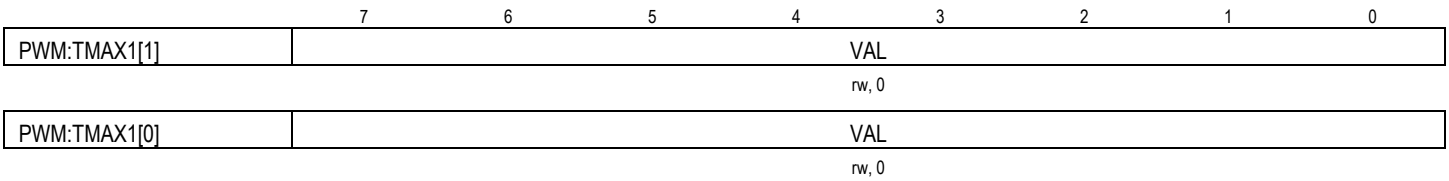
Address: 0x0798
Reset: 0x0000



15:0 **VAL** PWM1 high time or low time value

11.2.10 PWM:TMAX1 - PWM1 Maximum Cycle Time

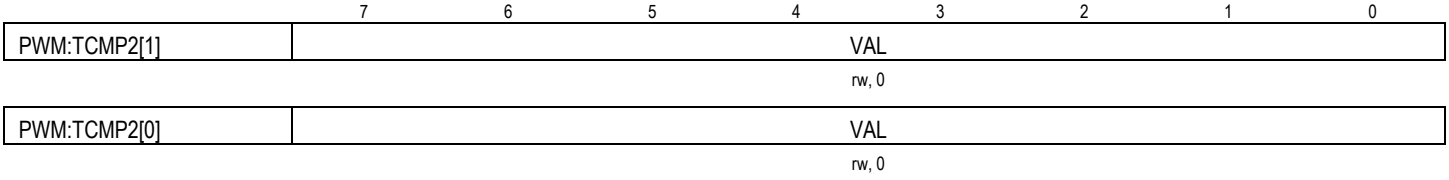
Address: 0x079a
Reset: 0x0000



15:0 **VAL** PWM1 cycle time value

11.2.11 PWM:TCMP2 - PWM2 Capture Mode Time

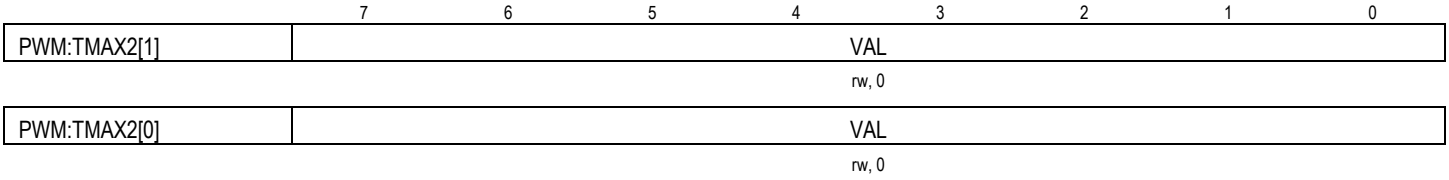
Address: 0x079c
Reset: 0x0000



15:0 **VAL** PWM2 high time or low time value

11.2.12 PWM:TMAX2 - PWM2 Maximum Cycle Time

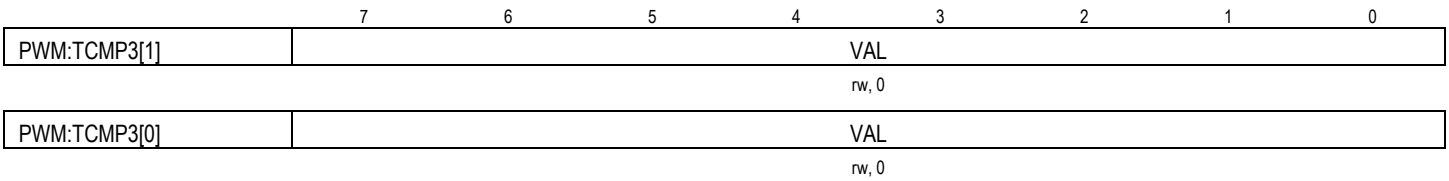
Address: 0x079e
Reset: 0x0000



15:0 **VAL** PWM2 cycle time value

11.2.13 PWM:TCMP3 - PWM3 Capture Mode Time

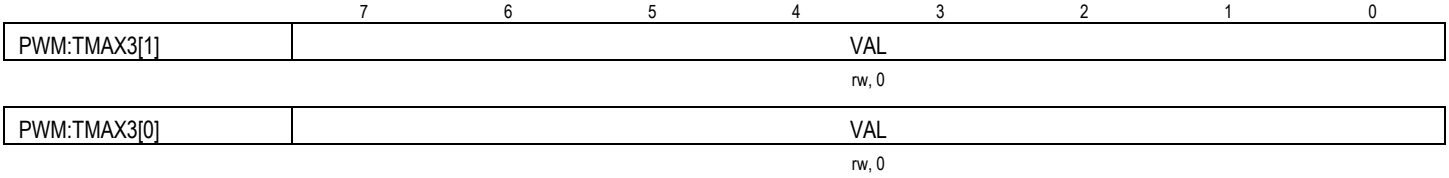
Address: 0x07a0
Reset: 0x0000



15:0 **VAL** PWM3 high time or low time value

11.2.14 PWM:TMAX3 - PWM3 Maximum Cycle Time

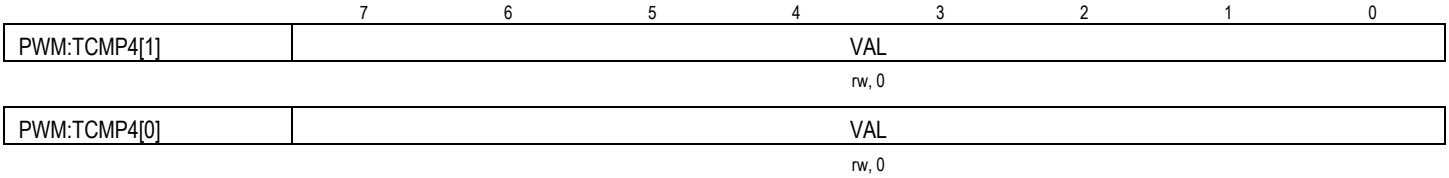
Address: 0x07a2
Reset: 0x0000



15:0 **VAL** PWM3 cycle time value

11.2.15 PWM:TCMP4 - PWM4 Capture Mode Time

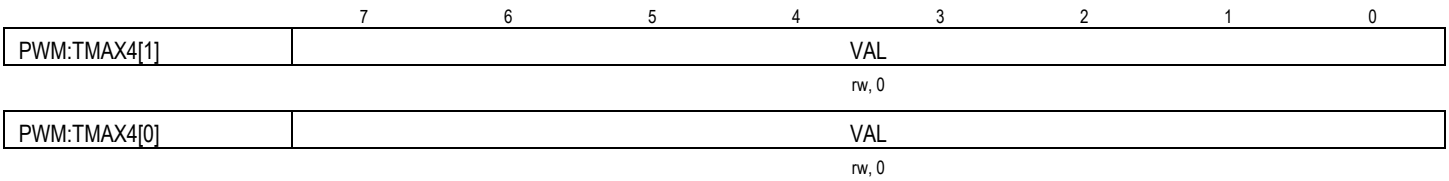
Address: 0x07a4
Reset: 0x0000



15:0 **VAL** PWM4 high time or low time value

11.2.16 PWM:TMAX4 - PWM4 Maximum Cycle Time

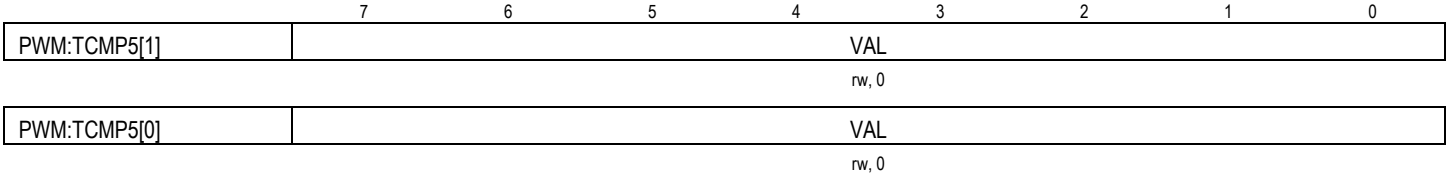
Address: 0x07a6
Reset: 0x0000



15:0 **VAL** PWM4 cycle time value

11.2.17 PWM:TCMP5 - PWM5 Capture Mode Time

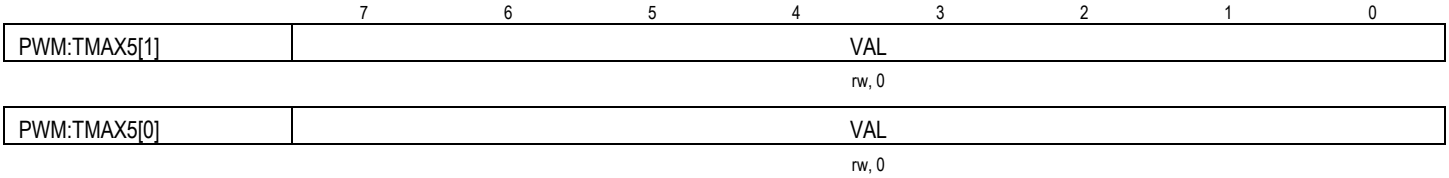
Address: 0x07a8
Reset: 0x0000



15:0 **VAL** PWM5 high time or low time value

11.2.18 PWM:TMAX5 - PWM5 Maximum Cycle Time

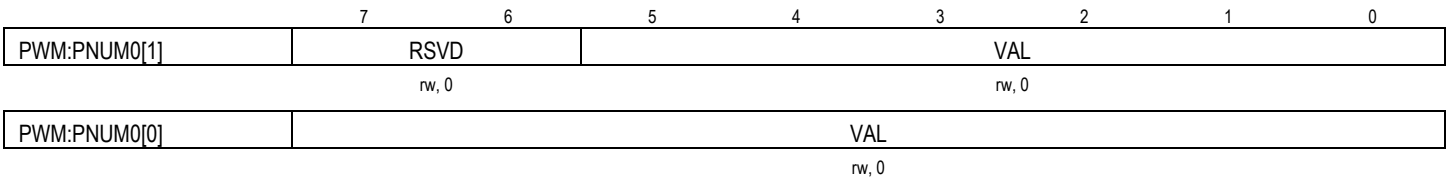
Address: 0x07aa
Reset: 0x0000



15:0 **VAL** PWM5 cycle time value

11.2.19 PWM:PNUM0 - PWM0 Pulse Number

Address: 0x07ac
Reset: 0x0000



13:0 **VAL** PWM0 Pulse number in count mode and IR mode

11.2.20 PWM:MASK0 - PWM Interrupt Mask

Address: 0x07b0
Reset: 0x00

	7	6	5	4	3	2	1	0
PWM:MASK0	FR5	FR4	FR3	FR2	FR1	FR0	DMA0	CNT0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

7 **FR5** Enable PWM5 frame interrupt
0: Disables interrupt
1: Enables interrupt

6 **FR4** Enable PWM4 frame interrupt
0: Disables interrupt
1: Enables interrupt

5 **FR3** Enable PWM3 frame interrupt
0: Disables interrupt
1: Enables interrupt

4 **FR2** Enable PWM2 frame interrupt
0: Disables interrupt
1: Enables interrupt

3 **FR1** Enable PWM1 frame interrupt
0: Disables interrupt
1: Enables interrupt

2 **FR0** Enable PWM0 frame interrupt
0: Disables interrupt
1: Enables interrupt

1 **DMA0** Enable PWM0 IR DMA FIFO mode interrupt
0: Disables interrupt
1: Enables interrupt

0 **CNT0** Enable PWM0 count interrupt
0: Disables interrupt
1: Enables interrupt

11.2.21 PWM:INT0 - PWM Interrupt Status

Address: 0x07b1
Reset: 0x00

	7	6	5	4	3	2	1	0
PWM:INT0	FR5	FR4	FR3	FR2	FR1	FR0	DMA0	CNT0
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0

7 **FR5** PWM5 cycle done interrupt indication (CNT5 – TMAX5)

0: No interrupt detected

1: Interrupt detected

Write 1 to clear.

6 **FR4** PWM4 cycle done interrupt indication (CNT4 – TMAX4)

0: No interrupt detected

1: Interrupt detected

Write 1 to clear.

5 **FR3** PWM3 cycle done interrupt indication (CNT3 – TMAX3)

0: No interrupt detected

1: Interrupt detected

Write 1 to clear.

4 **FR2** PWM2 cycle done interrupt indication (CNT2 – TMAX2)

0: No interrupt detected

1: Interrupt detected

Write 1 to clear.

3 **FR1** PWM1 cycle done interrupt indication (CNT1 – TMAX1)

0: No interrupt detected

1: Interrupt detected

Write 1 to clear.

2 **FR0** PWM0 cycle done interrupt indication (CNT0 – TMAX0)

0: No interrupt detected

1: Interrupt detected

Write 1 to clear.

1 **DMA0** PWM0 IR DMA FIFO mode interrupt indication (CNT0 & EMPTY)

0: No interrupt detected

1: Interrupt detected

Write 1 to clear.

0 **CNT0** PWM0 count interrupt indication (NCNT0 == PNUM0)

0: No interrupt detected

1: Interrupt detected

Write 1 to clear.

11.2.22 PWM:MASK1 - PWM Interrupt Mask

Address: 0x07b2
Reset: 0x00

7	6	5	4	3	2	1	0
PWM:MASK1			RSVD				FIFOCNT
			rw, 0				rw, 0

0 **FIFOCNT** Enable PWM0 FIFO count interrupt (FIFO mode)

0: Disables interrupt

1: Enables interrupt

11.2.23 PWM:INT1 - PWM Interrupt Status

Address: 0x07b3
Reset: 0x00

7	6	5	4	3	2	1	0
PWM:INT1			RSVD				FIFOCNT
			rw, 0				rw, 0

0 **FIFOCNT** PWM0 FIFO count interrupt (FIFO mode) indication (FIFO_NUM < FIFO_NUM_LVL)

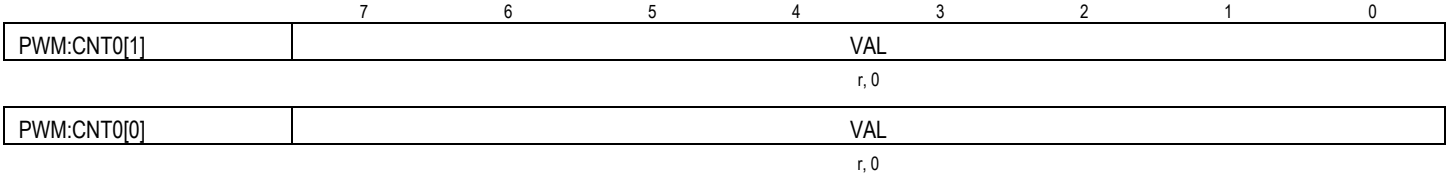
0: No interrupt detected

1: Interrupt detected

Write 1 to clear.

11.2.24 PWM:CNT0 - PWM0 Counter Value

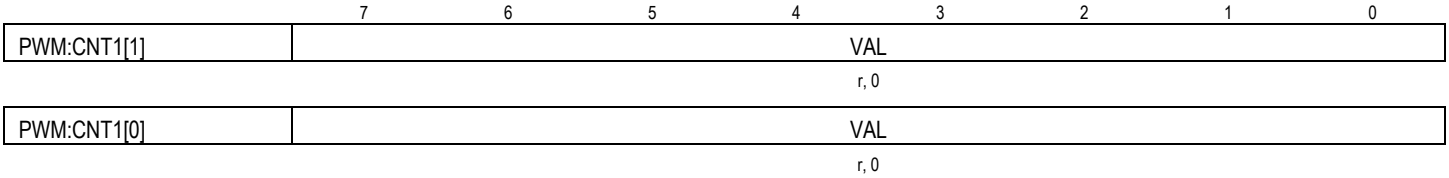
Address: 0x07b4
Reset: 0x0000



15:0 **VAL** PWM0 counter value

11.2.25 PWM:CNT1 - PWM1 Counter Value

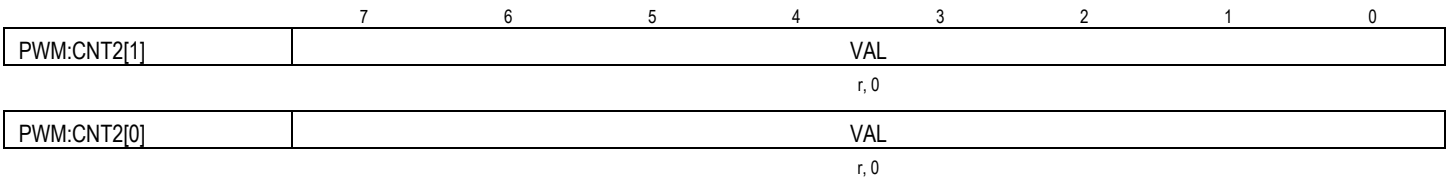
Address: 0x07b6
Reset: 0x0000



15:0 **VAL** PWM1 counter value

11.2.26 PWM:CNT2 - PWM2 Counter Value

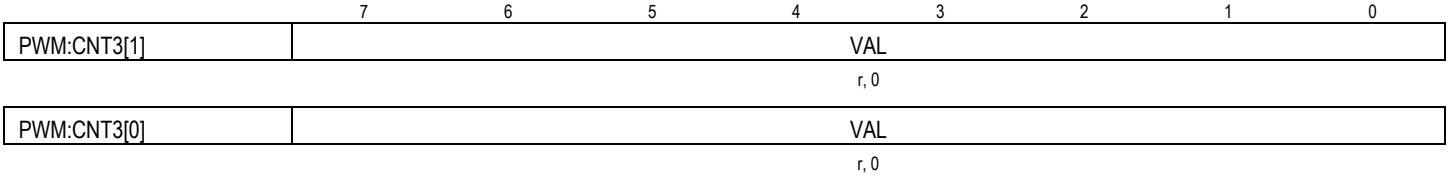
Address: 0x07b8
Reset: 0x0000



15:0 **VAL** PWM2 counter value

11.2.27 PWM:CNT3 - PWM3 Counter Value

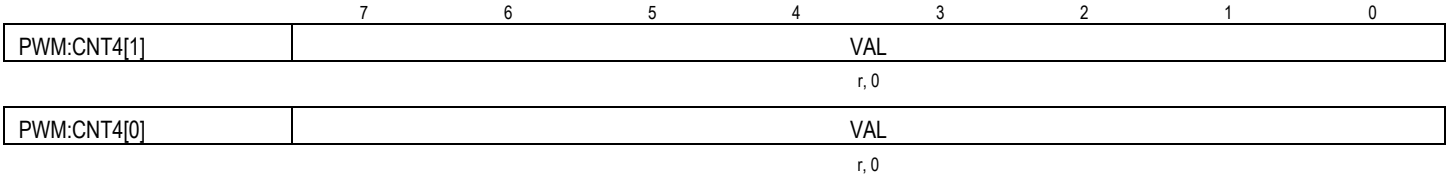
Address: 0x07ba
Reset: 0x0000



15:0 **VAL** PWM3 counter value

11.2.28 PWM:CNT4 - PWM4 Counter Value

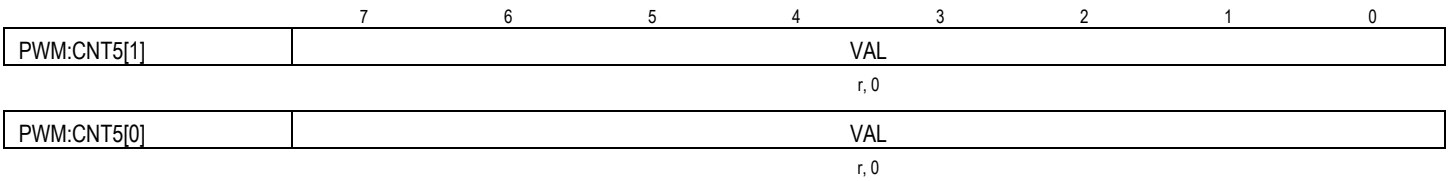
Address: 0x07bc
Reset: 0x0000



15:0 **VAL** PWM4 counter value

11.2.29 PWM:CNT5 - PWM5 Counter Value

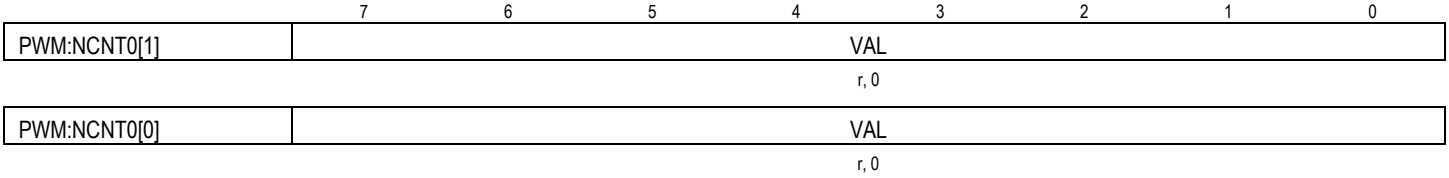
Address: 0x07be
Reset: 0x0000



15:0 **VAL** PWM5 counter value

11.2.30 PWM:NCNT0 - PWM0 Pulse Count Value

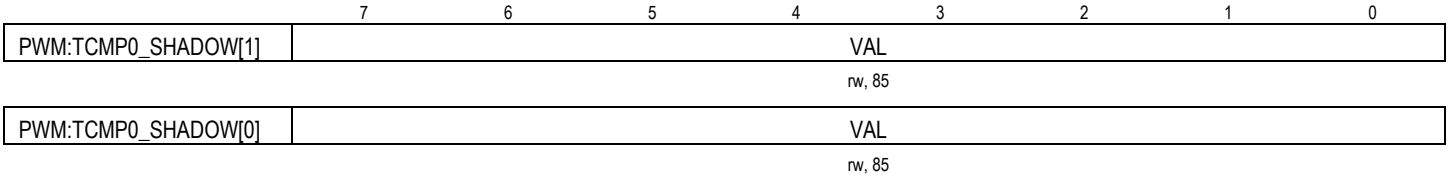
Address: 0x07c0
Reset: 0x0000



15:0 **VAL** PWM0 pulse count value

11.2.31 PWM:TCMP0_SHADOW - PWM0 Shadow Capture Mode Time

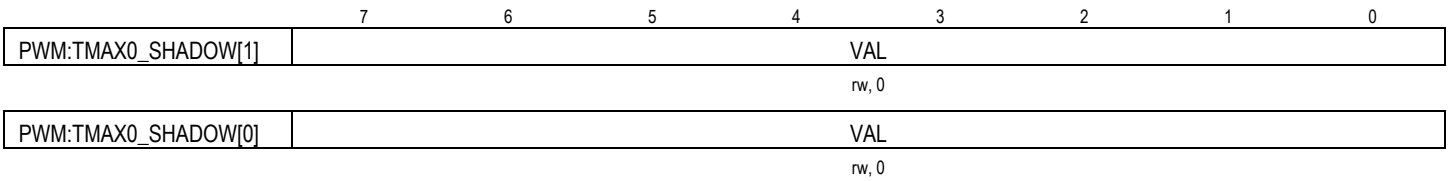
Address: 0x07c4
Reset: 0x5555



15:0 **VAL** PWM0 high or low time in IR FIFO or DMA FIFO mode

11.2.32 PWM:TMAX0_SHADOW - PWM0 Maximum Shadow Cycle Time

Address: 0x07c6
Reset: 0x0000



15:0 **VAL** PWM0 cycle time in IR FIFO or DMA FIFO mode

11.2.33 PWM:FIFO_DAT_ENTRY - FIFO Data Entry

Address: 0x07c8
Reset: 0x00

	7	6	5	4	3	2	1	0
PWM:FIFO_DAT_ENTRY[3]	VAL							
	rw, 0							
PWM:FIFO_DAT_ENTRY[2]	VAL							
	rw, 0							
PWM:FIFO_DAT_ENTRY[1]	VAL							
	rw, 0							
PWM:FIFO_DAT_ENTRY[0]	VAL							
	rw, 0							

31:0 **VAL** FIFO data entry byte 0 in IR FIFO mode

11.2.34 PWM:FIFO_NUM_LVL - FIFO Interrupt Trigger Entry

Address: 0x07cc
Reset: 0x00

	7	6	5	4	3	2	1	0
PWM:FIFO_NUM_LVL	VAL							
	rw, 0							

7:0 **VAL** FIFO interrupt trigger byte count

11.2.35 PWM:FIFO_SR - PWM FIFO Status

Address: 0x07cd
Reset: 0x00

	7	6	5	4	3	2	1	0
PWM:FIFO_SR	RSVD		FULL	EMPTY	DAT			
	r, 0		r, 0	r, 0	r, 0			

5 **FULL** FIFO full indication

0: FIFO data buffer is NOT full

1: FIFO data buffer is full

4 **EMPTY** FIFO empty indication

0: FIFO data buffer is NOT empty

1: FIFO data buffer is empty

3:0	**DAT**	FIFO data count Current number of bytes in the FIFO

11.2.36 PWM:FIFO_CLR - PWM FIFO Clear

Address: 0x07ce
Reset: 0x00

7	6	5	4	3	2	1	0
PWM:FIFO_CLR			RSVD				CLR
			w1, 0				w1, 0

0	**CLR**	Clear data FIFO **0:** Not used **1:** FIFO data buffer is cleared

12. Audio

12.1 Audio Input Path

There are three types of audio input path: digital microphone (DMIC), Codec (I2S) and analog input channel (AMIC), which is selectable through **AUDIO_IN:DFIFOAIN:AISEL**. Stereo or mono input processing can be selected through **AUDIO_IN:DFIFOAIN:AIMODE**.

Figure 21. Audio Input Path

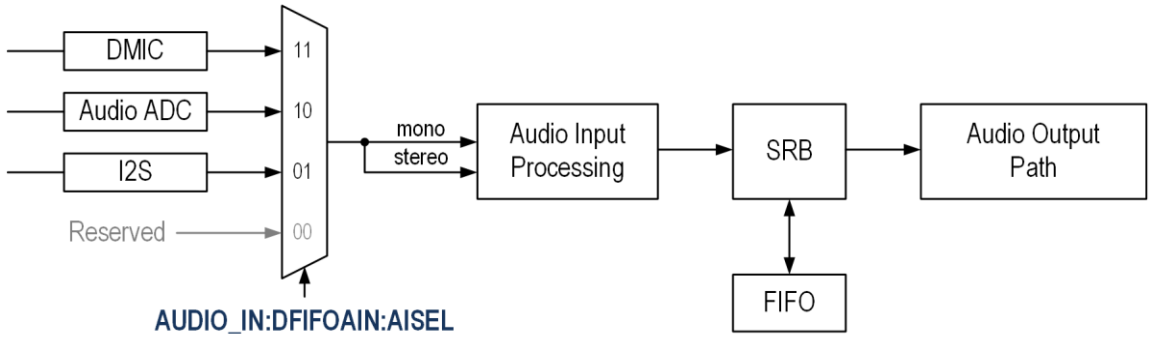


Table 11. Audio Data Flow Direction

Data Path		Target SRAM		
		FIFO0	FIFO1	FIFO2
DMIC	Decimation filter/LPF/Down Sample/HPF/ALC	√	√	×
I2S		√	√	×
ANALOG Channel 0		√	√	×
ANALOG Channel 1		√	√	×
ANALOG Channel 2		×	×	√

12.1.1 AMIC Input

AUDIO_IN:DFIFOAIN:AISEL should be set as 2b'10 to select AMIC as audio input.
A programmable stereo PGA (Programmable Gain Amplifier) with adjustable gain is built in for AMIC. AMIC input channel can carry out signal amplification through the PGA.

After implementing AD conversion for selected AMIC input signal, data of 3 analog channels (CH0–CH2) is generated. Data of CH0/CH1 is sent to the audio input processing module, while data of CH2 is directly written into the FIFO.

12.1.2 DMIC Input

Stereo digital microphone (DMIC) interface is also supported in the RYZ012. **AUDIO_IN:DFIFOAIN:AISEL** should be set as 2b'11 to select DMIC as audio input.

The DMIC interface includes one configurable clock line and one data line. **AUDIO_IN:DFIFOAIN:ESEL0** and **AUDIO_IN:DFIFOAIN:ESEL1** serves to set the rising/falling edge of clock signal at which to sample data of DMIC, and it should not be set as 2b'11. **AUDIO_IN:DFIFOAIN:EEN0** and **AUDIO_IN:DFIFOAIN:EEN1** serves to enable/mask the DMIC channel which samples data at rising/falling edge. Generally, **AUDIO_IN:DFIFOAIN:ESEL0** is set as 1b'0, **AUDIO_IN:DFIFOAIN:EEN0** is set as 1b'0 and **AUDIO_IN:DFIFOAIN:EEN1** is set as 1b'1 to enable DMIC0 sampling at rising edge of clock.

After data sampling of DMIC interface, sign extension and audio input processing, the signal can be written into the FIFO.

12.1.3 I2S Input

AUDIO_IN:DFIFOAIN:AISEL should be set as 2b'01 to select I2S as audio input.

Digital I2S audio interface supports Master mode only, 16-bit data width, and variable sampling rate: 8K/16K/22.05K/24K/32K/44.1K/48K. The sampling rate is determined by I2S clock. For I2S clock configuration details, see section **I2S Clock**.

The registers **AUDIO_OUT:CTRL:I2S_PLY**, **AUDIO_OUT:CTRL:I2S_REC** and **AUDIO_OUT:CTRL:I2S_EN** should be set to 1b'1 to enable I2S interface, I2S recorder and I2S player, respectively. The I2S interface includes one configurable clock line, one data line and one channel selection line. Data generated by the audio codec is written into FIFO after implementing conversion through the I2S Recorder and audio input processing.

12.1.4 DFIFO

As shown in Table 11, for any type of audio input path, the data will be finally written into DFIFO (DMA FIFO) 0, 1 or 2.

AUDIO_IN:DFIFOMODE:AI0, **AUDIO_IN:DFIFOMODE:AI1** and **AUDIO_IN:DFIFOMODE:AI2** should be set as 1b'1 to enable audio input of DFIFO 0–2.

DFIFO supports auto mode and manual mode. It is highly recommended to clear **AUDIO_IN:DFIFO_MANUAL:EN** to select auto mode.

Take DFIFO0 as an example:

- **AUDIO_IN:DFIFO0_BADR0**, **AUDIO_IN:DFIFO0_BADR1** and **AUDIO_IN:DFIFO0_BADR2** serve to set base address for DFIFO0, that is the starting address to write/read data into/from DFIFO0.
- **AUDIO_IN:DFIFO0_DEPTH** serves to set depth (that is the maximum data number) for DFIFO0. Suppose **AUDIO_IN:DFIFO0_DEPTH** is set as 0x01, then the DFIFO0 depth is 4 words, that is 16 bytes.
- Current data number (the difference value of write-pointer and read-pointer) in DFIFO0 can be read from **AUDIO_IN:DFIFO0_NUM**.
- The user can check current DFIFO0 read pointer/write pointer location by reading **AUDIO_IN:DFIFO0_RPTR** or **AUDIO_IN:DFIFO1_RPTR**.
- When current data number in DFIFO0 is less than the underflow threshold set in **AUDIO_IN:DFIFO0_LLEV**, **AUDIO_IN:DFIFOIRQST:LOW0A** and **AUDIO_IN:DFIFOIRQST:LOW0M** will be set as 1b'1 successively, and a FIFO0 low interrupt is generated if enabled through **AUDIO_IN:DFIFOMODE:LOW0**.

AUDIO_IN:DFIFOIRQST:LOW0A is automatically cleared when the data number in DFIFO0 is not less than the threshold. **AUDIO_IN:DFIFOIRQST:LOW0M** needs to be cleared manually.

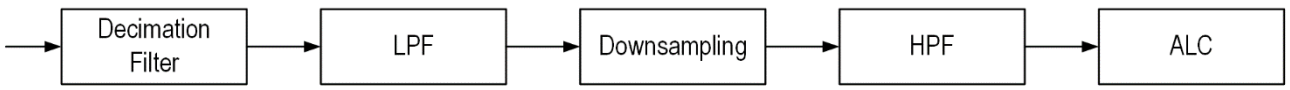
When current data number in DFIFO0 is more than the overflow threshold set in **AUDIO_IN:DFIFO0_HLEV**, **AUDIO_IN:DFIFOIRQST:HIGH0A** and **AUDIO_IN:DFIFOIRQST:HIGH0M** is set as 1b'1 successively, and a FIFO0 high interrupt is generated if enabled through **AUDIO_IN:DFIFOMODE:HIGH0**.

AUDIO_IN:DFIFOIRQST:HIGH0A is automatically cleared when the data number in DFIFO0 is no more than the threshold. **AUDIO_IN:DFIFOIRQST:HIGH0M** needs to be cleared manually.

12.2 Audio Input Processing

Audio input processing mainly includes configurable decimation filter, LPF (Low Pass Filter), Down-sample module, HPF (High Pass Filter) and ALC (Automatic Level Control). The decimation filter, LPF, Down-sample module, HPF and ALC can be enabled or bypassed through **AUDIO_IN:DFIFOAIN:DECFEN**, **AUDIO_IN:ALC_FLT_CTRL:HPFBYP**, **AUDIO_IN:ALC_FLT_CTRL:ALCBYP**, **AUDIO_IN:ALC_FLT_CTRL:LPFBYP** and **AUDIO_IN:ALC_FLT_CTRL:DSEN**.

Figure 22. Audio Input Processing



12.2.1 Decimation Filter

AUDIO_IN:DFIFOAIN:DECFEN should be cleared to enable decimation filter.
The decimation filter serves to down-sample the mono or stereo input data to required audio data playback rate (for example 48K or 32K).

Down-sampling rate is configurable as 1–8, 16, 32, 64, 128 or 256 by writing **AUDIO_IN:DFIFODEC:RATIO**.

AUDIO_IN:DFIFODEC:SHIFT serves to adjust decimation filter output by right shift, so that the data after down-sampling will not exceed data bit width.

12.2.2 Low Pass Filter (LPF)

AUDIO_IN:ALC_FLT_CTRL:LPFBYP should be cleared to enable the LPF. The LPF serves to conduct frequency compensation.

12.2.3 Down-sampling

If the Down-sample module is enabled by setting **AUDIO_IN:ALC_FLT_CTRL:DSEN** to 1b'1, it does down-sample the data from the LPF with a fixed ratio of 2.

12.2.4 High Pass Filter (HPF)

The HPF serves to eliminate internal DC offset to ensure audio amplification range. **AUDIO_IN:ALC_FLT_CTRL:HPFBYP** should be cleared to enable the HPF.
The HPF output is adjustable through setting the parameter in **AUDIO_IN:ALC_FLT_CTRL:HPFADJ**.

12.2.5 Adaptive Level Control (ALC)

The Adaptive Level Control supports analog mode and digital mode, and it mainly serves to regulate input volume level automatically or manually in each mode. The analog mode is designed only for AMIC input, while the digital mode applies to all audio input types. In analog mode, input volume level is regulated via PGA; while in digital mode, input volume level is regulated via Multiplier/Divider.

12.2.5.1 Automatic Regulation in Analog Mode

For automatic regulation in Analog Mode, **AUDIO_IN:ALC_CFG:ANSEL** should be set as 1b'1 and **AUDIO_IN:ALC_VOL_L:MODE** and **AUDIO_IN:ALC_VOL_R:MODE** should be set as 1b'1 to enable auto regulation mode for the left and right channel.

The result of (AMIC input × current PGA gain) is compared with the high volume target (**AUDIO_IN:ALC_VOL_THH**) and the low volume target (**AUDIO_IN:ALC_VOL_THL**). Meanwhile, it is compared with the volume noise level (**AUDIO_IN:ALC_VOL_THN**) to judge the noise signal and help regulate the PGA gain. The PGA gain automatically adjusts according to the comparison results, and it should be in the range of the minimum PGA gain (**AUDIO_IN:ALC_VOL_L**/**AUDIO_IN:ALC_VOL_R**) to the maximum the PGA gain (**AUDIO_IN:ALC_VOL_H**).

- **AUDIO_IN:ALC_VOL_THH:INT** and **AUDIO_IN:ALC_VOL_THH:FRAC** control the integer and the fractional part of the high volume target in units of dB.
- **AUDIO_IN:ALC_VOL_THL:INT** and **AUDIO_IN:ALC_VOL_THL:FRAC** control the integer and the fractional part of low volume target in units of dB.
- **AUDIO_IN:ALC_VOL_THN:INT** and **AUDIO_IN:ALC_VOL_THN:FRAC** control the integer and the fractional part of the volume noise level in units of dB.
- **AUDIO_IN:ALC_VOL_H** sets the maximum PGA gain, while **AUDIO_IN:ALC_VOL_L** and **AUDIO_IN:ALC_VOL_R** set the minimum PGA gain in the left and right channel.
- The user can check the current PGA gain in the left and right channel by reading **AUDIO_IN:CUR_PGA_GAIN_L** and **AUDIO_IN:CUR_PGA_GAIN_R**, respectively.

12.2.5.2 Manual Regulation in Analog Mode

For manual regulation, the PGA gain can be adjusted by either of the following two manual modes. Manual Mode 1

AUDIO_IN:PGA_FIX_VALUE:FGEN should be set as 1b'1 to select manual mode 1. In this mode, the PGA consists of two stages of amplifiers including pre-amplifier and post-amplifier and each stage has configurable gain. Bit 6 of **AUDIO_IN:PGA_FIX_VALUE:FGAIN** serves to set gain for the pre-amplifier (Boost-stage) as 18dB (1b'0, default) or 38dB (1b'1). While bit 0 to 5 of **AUDIO_IN:PGA_FIX_VALUE:FGAIN** serves to set gain for the post-amplifier (Gain-stage) as -10dB (0x0, default) to 14dB (0x30) with step of 0.5dB.

Manual Mode 2

AUDIO_IN:PGA_FIX_VALUE:FGEN and **AUDIO_IN:ALC_CFG:ANSEL** should be cleared to select manual mode 2. In this mode, **AUDIO_IN:PGA_MAN_TARGET_L:TGAIN** and **AUDIO_IN:PGA_MAN_TARGET_R:TGAIN** serve to set target gain value for left/right channel, while **AUDIO_IN:PGA_MAN_SPD** serves to set the speed for PGA gain to reach the target gain value. Current PGA gain can be read from **AUDIO_IN:PGA_VALUE_L:VAL** and **AUDIO_IN:PGA_VALUE_R:VAL** which changes until the target gain value is reached. When PGA gain reaches the target value, **AUDIO_IN:PGA_MAN_TARGET_L:TACC** and **AUDIO_IN:PGA_MAN_TARGET_R:TACC** are set as 1b'1.

12.2.5.3 Automatic Regulation in Digital Mode

For automatic regulation in Digital Mode, **AUDIO_IN:ALC_CFG:ANSEL** should be set as 1b'0 and **AUDIO_IN:ALC_VOL_L:MODE** and **AUDIO_IN:ALC_VOL_R:MODE** should be set as 1b'1 to enable auto regulation mode for the left and right channel.

The result of (Audio input × current digital gain) is compared with the high volume target (**AUDIO_IN:ALC_VOL_THH**) and the low volume target (**AUDIO_IN:ALC_VOL_THL**). Meanwhile, it is compared with the volume noise level (**AUDIO_IN:ALC_VOL_THN**) to judge the noise signal and help regulate the digital gain. The digital gain automatically adjusts according to the comparison results, and it should be in the range from minimum digital gain (**AUDIO_IN:ALC_VOL_L**/**AUDIO_IN:ALC_VOL_R**) to maximum digital gain (**AUDIO_IN:ALC_VOL_H**).

- **AUDIO_IN:ALC_VOL_THH:INT** and **AUDIO_IN:ALC_VOL_THH:FRAC** control the integer and the fractional part of the high volume target in units of dB.
- **AUDIO_IN:ALC_VOL_THL:INT** and **AUDIO_IN:ALC_VOL_THL:FRAC** control the integer and the fractional part of low volume target in units of dB.
- **AUDIO_IN:ALC_VOL_THN:INT** and **AUDIO_IN:ALC_VOL_THN:FRAC** control the integer and the fractional part of the volume noise level in units of dB.
- **AUDIO_IN:ALC_VOL_H** sets the maximum digital gain, while **AUDIO_IN:ALC_VOL_L** and **AUDIO_IN:ALC_VOL_R** set the minimum digital gain in the left and right channel.
- The user can check the current PGA gain in the left and right channel by reading **AUDIO_IN:ALC_VOL_L_R** and **AUDIO_IN:ALC_VOL_R_R**, respectively.

User can check current digital gain in left/right channel by reading **AUDIO_IN:ALC_VOL_L_R:GAIN** and **AUDIO_IN:ALC_VOL_R_R:GAIN**.

12.2.5.4 Manual Regulation in Digital Mode

For manual regulation in Digital Mode, **AUDIO_IN:ALC_CFG:ANSEL** should be set as 1b'0, and **AUDIO_IN:ALC_VOL_L:MODE** and **AUDIO_IN:ALC_VOL_R:MODE** should be set as 1b'0 to select manual regulation of the left and right channel.

The coefficient of multiplier/divider is configurable through registers **AUDIO_IN:ALC_VOL_L:GAIN** and **AUDIO_IN:ALC_VOL_R:GAIN** for left and right channel.

In manual mode (either analog mode or digital mode), the volume of the signal sent to the ALC module can be read through registers **AUDIO_IN:ALC_VOL_L_R:GAIN** and **AUDIO_IN:ALC_VOL_R_R:GAIN**.

12.3 Audio Input Path Register Reference

12.3.1 AUDIO_IN:DFIFO0_BADR0 - DFIFO0 Base Address

Address: 0x0b00
Reset: 0x00

	7	6	5	4	3	2	1	0
AUDIO_IN:DFIFO0_BADR0	VAL							
	rw, 0							

7:0 **VAL** FIFO0 base address byte 0

12.3.2 AUDIO_IN:DFIFO0_BADR1 - DFIFO0 Base Address

Address: 0x0b01
Reset: 0x40

	7	6	5	4	3	2	1	0
AUDIO_IN:DFIFO0_BADR1	VAL							
	rw, 64							

7:0 **VAL** FIFO0 base address byte 1

12.3.3 AUDIO_IN:DFIFO0_DEPTH - DFIFO0 Depth

Address: 0x0b02
Reset: 0x7f

	7	6	5	4	3	2	1	0
AUDIO_IN:DFIFO0_DEPTH	VAL							
	rw, 127							

7:0 **VAL** $FIFO0_{DEPTH}$ = FIFO0_DEPTH * (4 words)

12.3.4 AUDIO_IN:DFIFO0_BADR2 - DFIFO0 Base Address

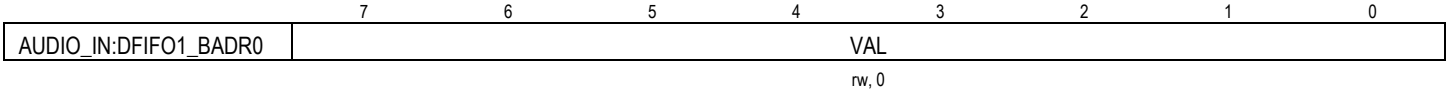
Address: 0x0b03
Reset: 0x04

	7	6	5	4	3	2	1	0
AUDIO_IN:DFIFO0_BADR2	RSVD				VAL			
	rw, 0				rw, 4			

3:0 **VAL** FIFO0 base address byte 2

12.3.5 AUDIO_IN:DFIFO1_BADR0 - DFIFO1 Base Address

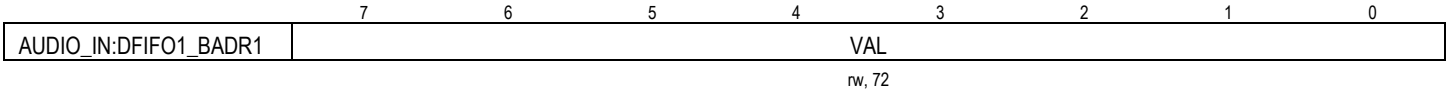
Address: 0x0b04
Reset: 0x00



7:0 **VAL** FIFO1 base address byte 0

12.3.6 AUDIO_IN:DFIFO1_BADR1 - DFIFO1 Base Address

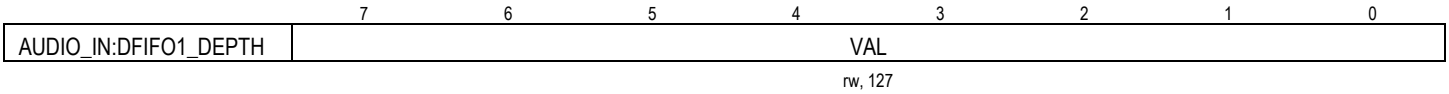
Address: 0x0b05
Reset: 0x48



7:0 **VAL** FIFO1 base address byte 1

12.3.7 AUDIO_IN:DFIFO1_DEPTH - DFIFO1 Depth

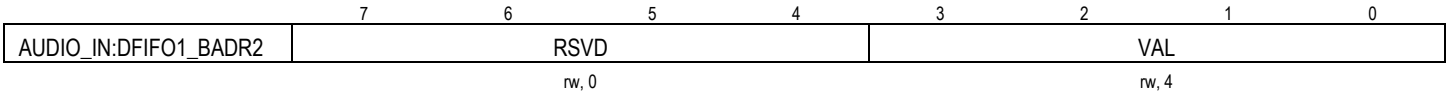
Address: 0x0b06
Reset: 0x7f



7:0 **VAL** $FIFO1_{DEPTH}$ = FIFO1_DEPTH * (4 words)

12.3.8 AUDIO_IN:DFIFO1_BADR2 - DFIFO1 Base Address

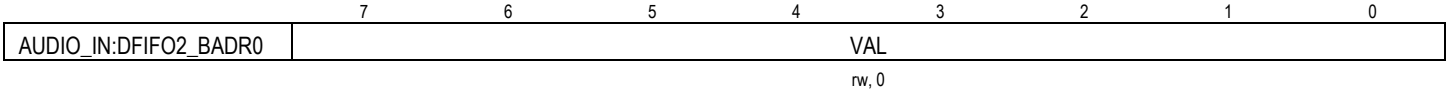
Address: 0x0b07
Reset: 0x04



3:0 **VAL** FIFO1 base address byte 2

12.3.9 AUDIO_IN:DFIFO2_BADR0 - DFIFO2 Base Address

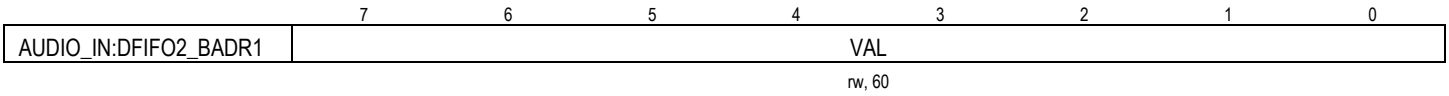
Address: 0x0b08
Reset: 0x00



7:0 **VAL** FIFO2 base address byte 0

12.3.10 AUDIO_IN:DFIFO2_BADR1 - DFIFO2 Base Address

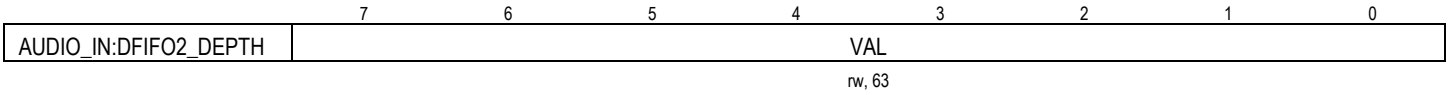
Address: 0x0b09
Reset: 0x3c



7:0 **VAL** FIFO2 base address byte 1

12.3.11 AUDIO_IN:DFIFO2_DEPTH - DFIFO2 Depth

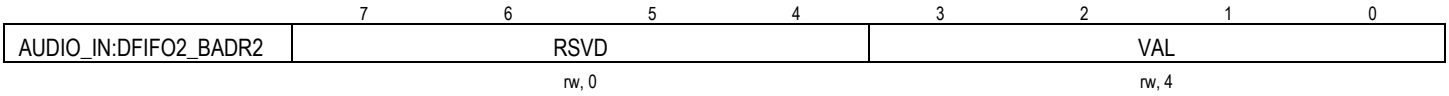
Address: 0x0b0a
Reset: 0x3f



7:0 **VAL** $FIFO2_{DEPTH}$ = FIFO2_DEPTH * (4 words)

12.3.12 AUDIO_IN:DFIFO2_BADR2 - DFIFO2 Base Address

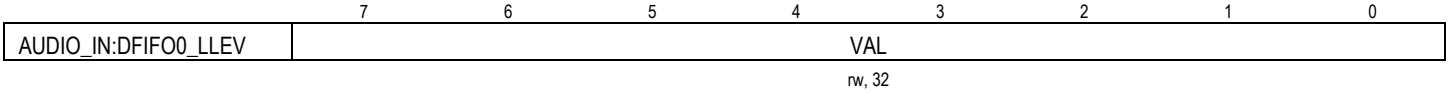
Address: 0x0b0b
Reset: 0x04



3:0 **VAL** FIFO2 base address byte 2

12.3.13 AUDIO_IN:DFIFO0_LLEV – DFIFO0 Interrupt Level

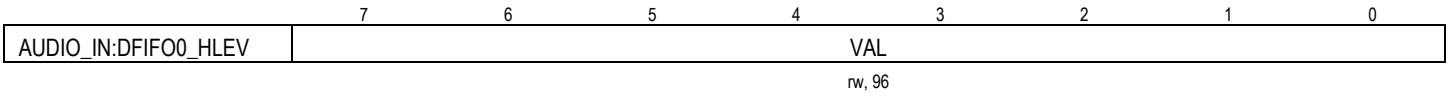
Address: 0x0b0c
Reset: 0x20



7:0 **VAL** FIFO0 interrupt trigger low level byte count

12.3.14 AUDIO_IN:DFIFO0_HLEV - DFIFO0 Interrupt Level

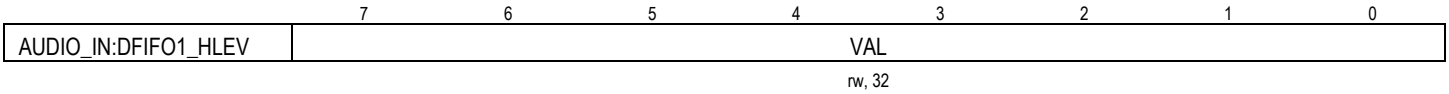
Address: 0x0b0d
Reset: 0x60



7:0 **VAL** FIFO0 interrupt trigger high level byte count

12.3.15 AUDIO_IN:DFIFO1_HLEV - DFIFO1 Interrupt Level

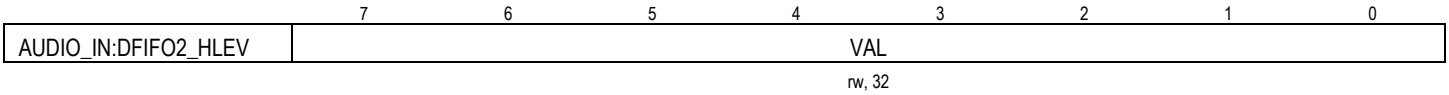
Address: 0x0b0e
Reset: 0x20



7:0 **VAL** FIFO1 interrupt trigger high level byte count

12.3.16 AUDIO_IN:DFIFO2_HLEV - DFIFO2 Interrupt Level

Address: 0x0b0f
Reset: 0x20



7:0 **VAL** FIFO2 interrupt trigger high level byte count

12.3.17 AUDIO_IN:DFIFOMODE - DFIFO Mode

Address: 0x0b10
Reset: 0xF9

	7	6	5	4	3	2	1	0
AUDIO_IN:DFIFOMODE	HIGH	HIGH1	HIGH0	LOW0	AO0	AI2	AI1	AI0
	rw, 1	rw, 1	rw, 1	rw, 1	rw, 1	rw, 0	rw, 0	rw, 1

7 **HIGH** FIFO2 high interrupt enable
14: Disables FIFOx interrupt
15: Enables FIFOx interrupt

6 **HIGH1** FIFO1 high interrupt enable
12: Disables FIFOx interrupt
13: Enables FIFOx interrupt

5 **HIGH0** FIFO0 high interrupt enable
10: Disables FIFOx interrupt
11: Enables FIFOx interrupt

4 **LOW0** FIFO0 low interrupt enable
8: Disables FIFOx interrupt
9: Enables FIFOx interrupt

3 **AO0** Enable audio output of FIFO0
6: Disables FIFOx output
7: Enables FIFOx output

2 **AI2** Enable audio input of FIFO2
4: Disables FIFOx input
5: Enables FIFOx input

1 **AI1** Enable audio input of FIFO1
2: Disables FIFOx input
3: Enables FIFOx input

0 **AI0** Enable audio input of FIFO0
0: Disables FIFOx input
1: Enables FIFOx input

12.3.18 AUDIO_IN:DFIFOAIN - DFIFO Analog Input Configuration

Address: 0x0b11
Reset: 0x21

	7	6	5	4	3	2	1	0
AUDIO_IN:DFIFOAIN	EEN1	EEN0	DECFEN	AIMODE	AISEL		ESEL1	ESEL0
	rw, 0	rw, 0	rw, 1	rw, 0	rw, 0		rw, 0	rw, 1

7 **EEN1** dmic_fall_chn_not_en (generally disabled)

0: Disables DMICx sampling at falling edge of clock

1: Enables DMICx sampling at falling edge of clock

6 **EEN0** dmic_raise_chn_not_en

0: Disables DMICx sampling at rising edge of clock

1: Enables DMICx sampling at rising edge of clock

5 **DECFEN** Enable input decimation filter (low active)

0: Enables input filter

1: Disables input filter

4 **AIMODE** Audio input mode selection

0: Select audio stereo input

1: Select audio mono input

3:2 **AISEL** Audio input selection

00: no available

01: Select I2S input

10: Select ADC input

11: Select D-MIC input

1 **ESEL1** D-MIC1 edge selection

0: Select data usage at rising edge of clock

1: Select data usage at falling edge of clock

0 **ESEL0** D-MIC0 edge selection

0: Select data usage at rising edge of clock

1: Select data usage at falling edge of clock

12.3.19 AUDIO_IN:DFIFODEC - DFIFO QDEC Configuration

Address: 0x0b12
Reset: 0x5b

	7	6	5	4	3	2	1	0
AUDIO_IN:DFIFODEC	SHIFT				RATIO			
	rw, 5				rw, 11			

7:4 **SHIFT** CIC shift select (0 – 7)

3:0 **RATIO** CIC down conversion ratio

12.3.20 AUDIO_IN:DFIFOIRQST - DFIFOx Interrupt Status

Address: 0x0b13
Reset: 0x00

	7	6	5	4	3	2	1	0
AUDIO_IN:DFIFOIRQST	HIGH2M	HIGH1M	HIGH0M	LOW0M	HIGH2A	HIGH1A	HIGH0A	LOW0A
	rw1c, 0	rw1c, 0	rw1c, 0	rw1c, 0	r, 0	r, 0	r, 0	r, 0

7 **HIGH2M** FIFO2 high level interrupt indication

0: No interrupt detected

1: Interrupt detected

Write 1 to clear.

6 **HIGH1M** FIFO1 high level interrupt indication

0: No interrupt detected

1: Interrupt detected

Write 1 to clear.

5 **HIGH0M** FIFO0 high level interrupt indication

0: No interrupt detected

1: Interrupt detected

Write 1 to clear.

4 **LOW0M** FIFO0 low level interrupt indication

0: No interrupt detected

1: Interrupt detected

Write 1 to clear.

3 **HIGH2A** FIFO2 high level interrupt indication

0: No interrupt detected

1: Interrupt detected

Cleared by hardware when number of items in FIFO0 is below DFIFO2_HLEV.

2	**HIGH1A**	FIFO1 high level interrupt indication **0:** No interrupt detected **1:** Interrupt detected Cleared by hardware when number of items in FIFO0 is below DFIFO1_HLEV.
1	**HIGH0A**	FIFO0 high level interrupt indication **0:** No interrupt detected **1:** Interrupt detected Cleared by hardware when number of items in FIFO0 is below DFIFO0_HLEV.
0	**LOW0A**	FIFO0 low level interrupt indication **0:** No interrupt detected **1:** Interrupt detected Cleared by hardware when number of items in FIFO0 is above DFIFO0_LLEV.

12.3.21 AUDIO_IN:DFIFO0_RPTR - Read FIFO0 PTR

Address: 0x0b14
Reset: 0x0000

	7	6	5	4	3	2	1	0
AUDIO_IN:DFIFO0_RPTR[1]	RSVD				VAL			
	ro, 0				ro, 0			
AUDIO_IN:DFIFO0_RPTR[0]	VAL							
	ro, 0							

11:0	**VAL**	Read FIFO0 PTR value

12.3.22 AUDIO_IN:DFIFO0_WPTR - Write FIFO0 PTR

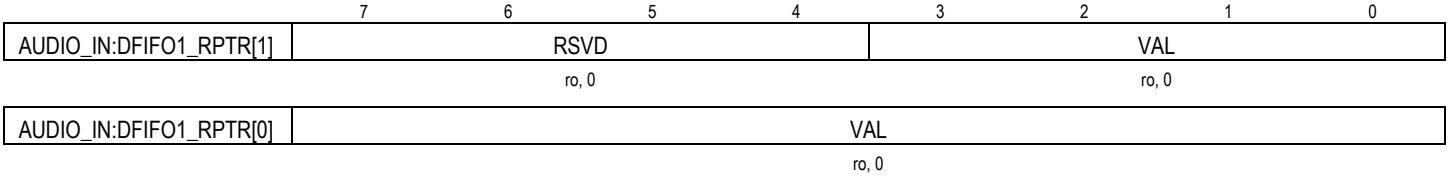
Address: 0x0b16
Reset: 0x0000

	7	6	5	4	3	2	1	0
AUDIO_IN:DFIFO0_WPTR[1]	RSVD				VAL			
	ro, 0				ro, 0			
AUDIO_IN:DFIFO0_WPTR[0]	VAL							
	ro, 0							

11:0	**VAL**	Write FIFO0 PTR value

12.3.23 AUDIO_IN:DFIFO1_RPTR - Read FIFO1 PTR

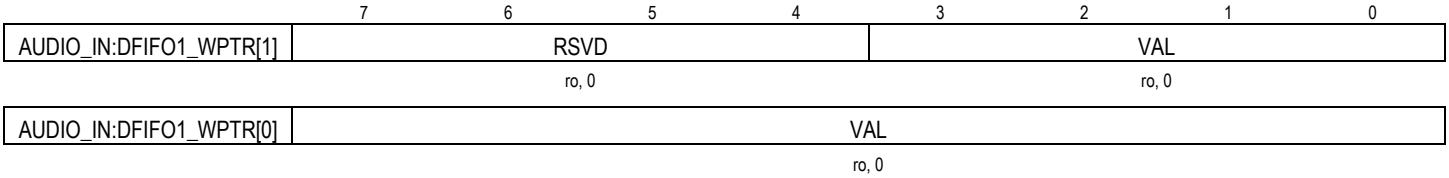
Address: 0x0b18
Reset: 0x0000



11:0 **VAL** Read FIFO1 PTR value

12.3.24 AUDIO_IN:DFIFO1_WPTR - Write FIFO1 PTR

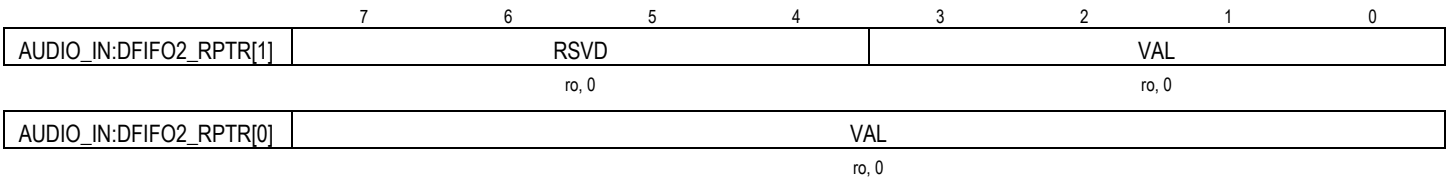
Address: 0x0b1a
Reset: 0x0000



11:0 **VAL** Write FIFO1 PTR value

12.3.25 AUDIO_IN:DFIFO2_RPTR - Read FIFO2

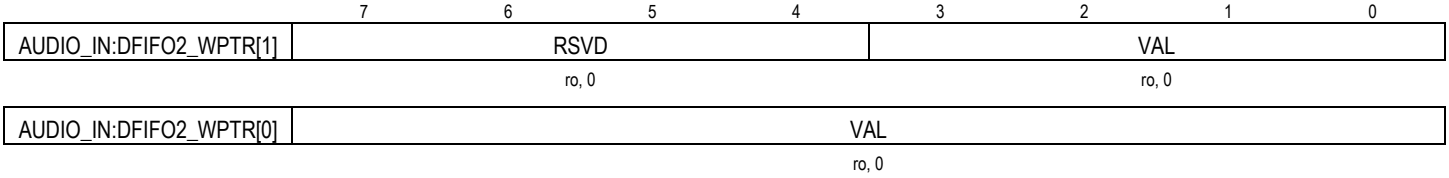
Address: 0x0b1c
Reset: 0x0000



11:0 **VAL** Read FIFO2 PTR value

12.3.26 AUDIO_IN:DFIFO2_WPTR - Write FIFO2 PTR

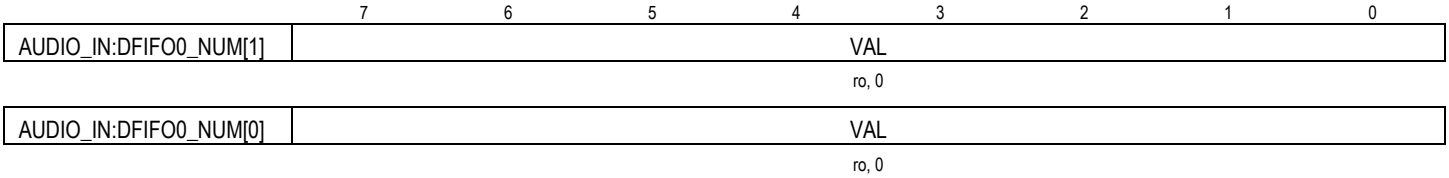
Address: 0x0b1e
Reset: 0x0000



11:0 **VAL** Write FIFO2 PTR value

12.3.27 AUDIO_IN:DFIFO0_NUM - Number FIFO0

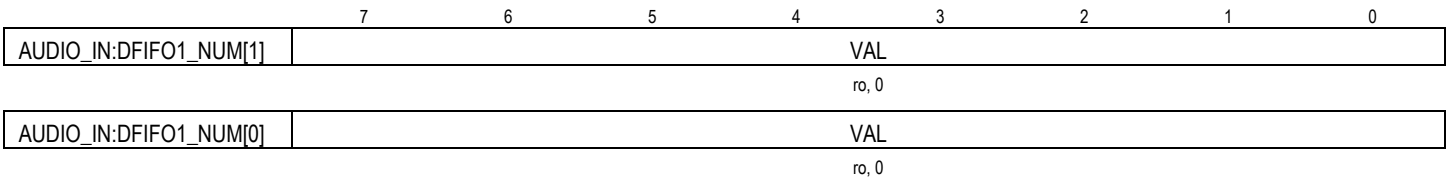
Address: 0x0b20
Reset: 0x0000



15:0 **VAL** Current number of bytes FIFO0

12.3.28 AUDIO_IN:DFIFO1_NUM - Number FIFO1

Address: 0x0b24
Reset: 0x0000



15:0 **VAL** Current number of bytes FIFO1

12.3.29 AUDIO_IN:DFIFO2_NUM - Number FIFO2

Address: 0x0b28
Reset: 0x0000

	7	6	5	4	3	2	1	0
AUDIO_IN:DFIFO2_NUM[1]	VAL							
	ro, 0							
AUDIO_IN:DFIFO2_NUM[0]	VAL							
	ro, 0							

15:0 **VAL** Current number of bytes FIFO2

12.3.30 AUDIO_IN:DFIFO_MANUAL - DFIFO Manual Mode

Address: 0x0b2c
Reset: 0x00

	7	6	5	4	3	2	1	0
AUDIO_IN:DFIFO_MANUAL	RSVD							EN
	rw, 0							rw, 0

0 **EN** DFIFO Manual Mode

0: FIFO automatic mode

1: FIFO manual mode

12.3.31 AUDIO_IN:DFIFO_MAN_DAT0 - DFIFO Manual Mode Data

Address: 0x0b30
Reset: 0x00

	7	6	5	4	3	2	1	0
AUDIO_IN:DFIFO_MAN_DAT0	VAL							
	w, 0							

7:0 **VAL** FIFO manual mode data input (byte 0)

12.3.32 AUDIO_IN:DFIFO_MAN_DAT1 - DFIFO Manual Mode Data

Address: 0x0b31
Reset: 0x00

7	6	5	4	3	2	1	0
AUDIO_IN:DFIFO_MAN_DAT1				VAL			
				w, 0			

7:0 **VAL** FIFO manual mode data input (byte 1)

12.3.33 AUDIO_IN:DFIFO_MAN_DAT2 - DFIFO Manual Mode Data

Address: 0x0b32
Reset: 0x00

7	6	5	4	3	2	1	0
AUDIO_IN:DFIFO_MAN_DAT2				VAL			
				w, 0			

7:0 **VAL** FIFO manual mode data input (byte 2)

12.3.34 AUDIO_IN:DFIFO_MAN_DAT3 - DFIFO Manual Mode Data

Address: 0x0b33
Reset: 0x00

7	6	5	4	3	2	1	0
AUDIO_IN:DFIFO_MAN_DAT3				VAL			
				w, 0			

7:0 **VAL** FIFO manual mode data input (byte 3)

12.3.35 AUDIO_IN:AUDIO_CFG - Audio Configuration

Address: 0x0b35
Reset: 0x09

	7	6	5	4	3	2	1	0
AUDIO_IN:AUDIO_CFG	RSVD			INSWAP	ADCTRIM	ADCSIGN	ADCOPT	VALIDEN
	rw, 0			rw, 0	rw, 1	rw, 0	rw, 0	rw, 1

4 **INSWAP** Enable audio input left/right channel swap (AMIC/DMIC/I2S)

0: Disables audio input channel swap

1: Enables audio input channel swap

3 **ADCTRIM** Enable bypass ADC trim

0: Disables bypass ADC trim

1: Enables bypass ADC trim

2 **ADCSIGN** Enable ADC signed byte

0: Disables ADC signed byte

1: Enables ADC signed byte

1 **ADCOPT** Enable ADC 64/63 option

0: Disables ADC 64/63 option

1: Enables ADC 64/63 option

0 **VALIDEN** Enable ADC valid indication

0: Disables ADC valid indication

1: Enables ADC valid indication

12.3.36 AUDIO_IN:ADC_MUL - ADC calibration multiplicator

Address: 0x0b36
Reset: 0x00

	7	6	5	4	3	2	1	0
AUDIO_IN:ADC_MUL	MUL							
	rw, 0							

7:0 **MUL** ADC calibration multiplicator

12.3.37 AUDIO_IN:ADC_BIAS - ADC calibration bias

Address: 0x0b37
Reset: 0x00

	7	6	5	4	3	2	1	0
AUDIO_IN:ADC_BIAS	BIAS							
	rw, 0							

7:0 **BIAS** ADC calibration bias

12.3.38 AUDIO_IN:ALC_FLT_CTRL - ALC Filter Control

Address: 0x0b40
Reset: 0xfb

	7	6	5	4	3	2	1	0
AUDIO_IN:ALC_FLT_CTRL	DSEN	LPFBYP	ALCBYP	HPFBYP	HPFADJ			
	rw, 1	rw, 1	rw, 1	rw, 1	rw, 11			

7 **DSEN** Enable double down sampling
0: Disables double down sampling
1: Enables double down sampling

6 **LPFBYP** LPF Bypass
0: LPF is enabled
1: LPF is bypassed

5 **ALCBYP** ALC Bypass Control
0: ALC is enabled
1: ALC is bypassed

4 **HPFBYP** HPF Bypass
0: HPF is enabled
1: HPF is bypassed

3:0 **HPFADJ** Parameter to adjust HPF output.

12.3.39 AUDIO_IN:ALC_VOL_L - ALC Left Channel Setting

Address: 0x0b41
Reset: 0x20

	7	6	5	4	3	2	1	0
AUDIO_IN:ALC_VOL_L	MODE	GAIN						
	rw, 0	rw, 32						

7 **MODE** Mode selection

0: Select automatic mode

1: Select manual mode

6:0 **GAIN** [6:0] Minimum gain limit in automatic mode

[5:0] Digital gain in manual mode

12.3.40 AUDIO_IN:ALC_VOL_R - ALC Right Channel Setting

Address: 0x0b42
Reset: 0x20

	7	6	5	4	3	2	1	0
AUDIO_IN:ALC_VOL_R	MODE	GAIN						
	rw, 0	rw, 32						

7 **MODE** Mode selection

0: Select automatic mode

1: Select manual mode

6:0 **GAIN** [6:0] Minimum gain limit in automatic mode

[5:0] Digital gain in manual mode

12.3.41 AUDIO_IN:ALC_VOL_H - Maximum PGA Gain Limit

Address: 0x0b43
Reset: 0x33

	7	6	5	4	3	2	1	0
AUDIO_IN:ALC_VOL_H	RSVD	GAIN						
	rw, 0	rw, 51						

6:0 **GAIN** Maximum PGA gain limit in automatic mode

12.3.42 AUDIO_IN:ALC_VOL_THH - PGA High Volume Target

Address: 0x0b44
Reset: 0x60

	7	6	5	4	3	2	1	0
AUDIO_IN:ALC_VOL_THH	RSVD	INT						FRAC
	rw, 0	rw, 48						rw, 0

6:1	**INT**	Set integer part [dB] of high volume target in automatic mode
0	**FRAC**	Set fractional part [dB] of high volume target in automatic mode

12.3.43 AUDIO_IN:ALC_VOL_THL - PGA LOW volume Target

Address: 0x0b46
Reset: 0x40

	7	6	5	4	3	2	1	0
AUDIO_IN:ALC_VOL_THL	RSVD	INT						FRAC
	rw, 0	rw, 32						rw, 0

6:1	**INT**	Set integer part [dB] of low volume target in automatic mode
0	**FRAC**	Set fractional part [dB] of low volume target in automatic mode

12.3.44 AUDIO_IN:ALC_VOL_THN - PGA Noise Level Target

Address: 0x0b48
Reset: 0x02

	7	6	5	4	3	2	1	0
AUDIO_IN:ALC_VOL_THN	RSVD	INT						FRAC
	rw, 0	rw, 1						rw, 0

6:1	**INT**	Set integer part [dB] of noise level in automatic mode
0	**FRAC**	Set fractional part [dB] of noise level in automatic mode

12.3.45 AUDIO_IN:ALC_VOL_L_R - PGA Left Channel Gain

Address: 0x0b4d
Reset: 0x00

	7	6	5	4	3	2	1	0
AUDIO_IN:ALC_VOL_L_R	GAIN							
	r, 0							

7:0 **GAIN** Current digital gain/volume in automatic/manual mode of left channel

12.3.46 AUDIO_IN:ALC_VOL_R_R - PGA Right Channel Gain

Address: 0x0b4e
Reset: 0x00

	7	6	5	4	3	2	1	0
AUDIO_IN:ALC_VOL_R_R	GAIN							
	r, 0							

7:0 **GAIN** Current digital gain/volume in automatic/manual mode of right channel

12.3.47 AUDIO_IN:ALC_PEAK_TICK_L - Peak Tick

Address: 0x0b50
Reset: 0x00

	7	6	5	4	3	2	1	0
AUDIO_IN:ALC_PEAK_TICK_L	TICK0							
	rw, 0							

7:0 **TICK0** Peak tick byte 0

12.3.48 AUDIO_IN:ALC_PEAK_TICK_H - Peak Tick

Address: 0x0b51
Reset: 0x20

	7	6	5	4	3	2	1	0
AUDIO_IN:ALC_PEAK_TICK_H	TICK1							
	rw, 32							

7:0 **TICK1** Peak tick byte 1

12.3.49 AUDIO_IN:ALC_CFG - ALC Configuration

Address: 0x0b54
Reset: 0x0a

	7	6	5	4	3	2	1	0
AUDIO_IN:ALC_CFG	RSVD			MAXEN	TICKCLR	IIRAEN	IIRVEN	ANSEL
	rw, 0			rw, 0	rw, 1	rw, 0	rw, 1	rw, 0

4 **MAXEN** Enable vad maximum

0: Disables vad maximum

1: Enables vad maximum

3 **TICKCLR** Clear ALC_PEAK_TICK

0: Not used

1: ALC_PEAK_TICK bytes will be cleared

If ALC_PEAK_TICK is cleared, the bit is automatically reset

2 **IIRAEN** Enable analog IIR

0: Disables analog IIR

1: Enables analog IIR

1 **IIRVEN** Enable vad IIR

0: Disables vad IIR

1: Enables vad IIR

0 **ANSEL** Analog mode selection

0: Select digital mode

1: Select analog mode

12.3.50 AUDIO_IN:ALC_COEF_IIR - IIR coefficient

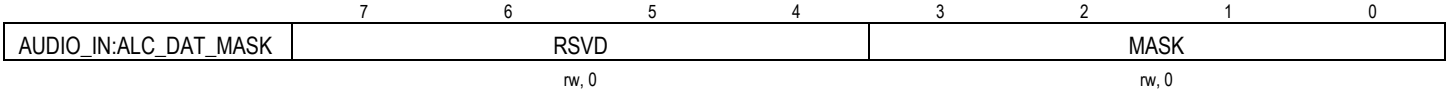
Address: 0x0b55
Reset: 0xfa

	7	6	5	4	3	2	1	0
AUDIO_IN:ALC_COEF_IIR	COEF							
	rw, 250							

7:0 **COEF** IIR coefficient

12.3.51 AUDIO_IN:ALC_DAT_MASK - Data Mask

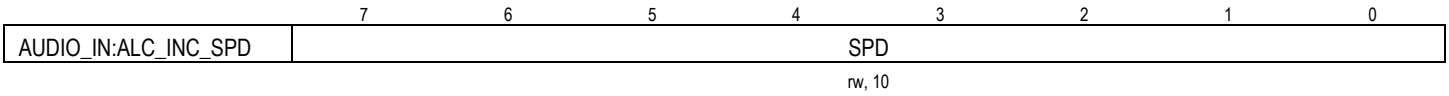
Address: 0x0b56
Reset: 0x00



3:0 **MASK** Configure the data to be masked for gain changes in automatic mode

12.3.52 AUDIO_IN:ALC_INC_SPD - PGA Gain Increase Speed

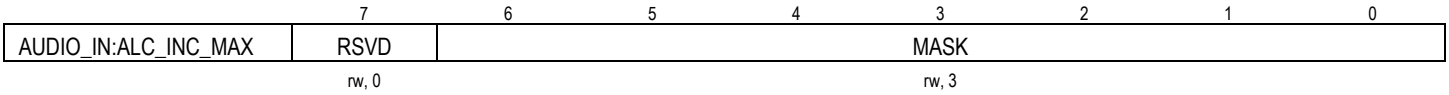
Address: 0x0b57
Reset: 0x0a



7:0 **SPD** PGA gain increase speed in automatic mode

12.3.53 AUDIO_IN:ALC_INC_MAX - PGA Maximum Gain Increase

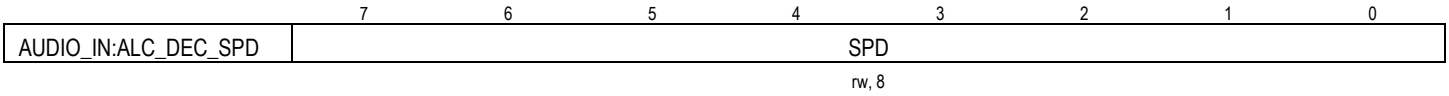
Address: 0x0b58
Reset: 0x03



6:0 **MASK** PGA maximum gain increase of a peak tick cycle in automatic mode

12.3.54 AUDIO_IN:ALC_DEC_SPD - PGA Gain Decrease Speed

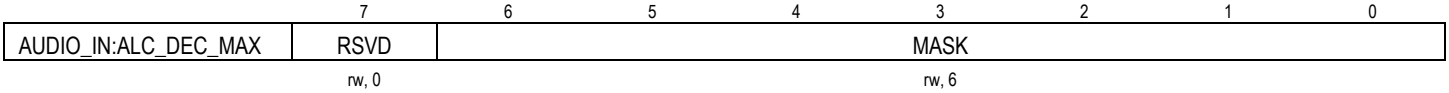
Address: 0x0b59
Reset: 0x08



7:0 **SPD** PGA gain decrease speed in automatic mode

12.3.55 AUDIO_IN:ALC_DEC_MAX - PGA Maximum Gain Decrease

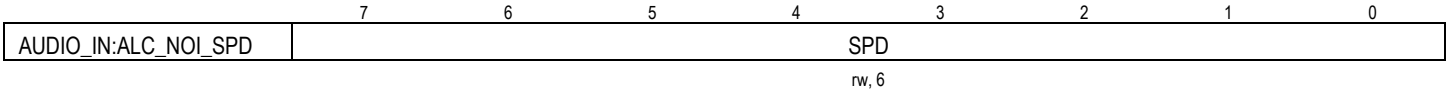
Address: 0x0b5a
Reset: 0x06



6:0 **MASK** PGA maximum gain decrease of a peak tick cycle in automatic mode

12.3.56 AUDIO_IN:ALC_NOI_SPD - PGA Gain Decrease Speed (noise)

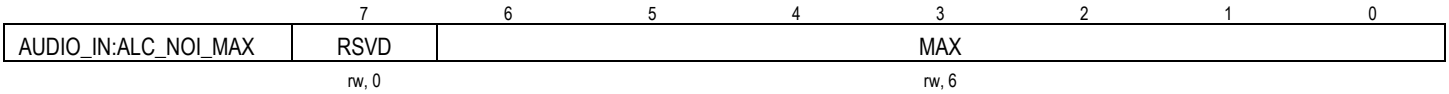
Address: 0x0b5b
Reset: 0x06



7:0 **SPD** PGA gain decrease speed in automatic mode, if there is noise

12.3.57 AUDIO_IN:ALC_NOI_MAX - PGA Maximum Gain Decrease (noise)

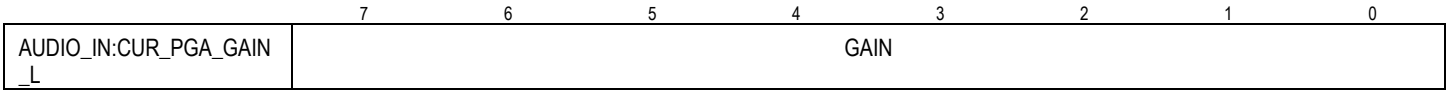
Address: 0x0b5c
Reset: 0x06



6:0 **MAX** PGA maximum gain decrease of a peak tick cycle in automatic mode, if there is noise

12.3.58 AUDIO_IN:CUR_PGA_GAIN_L - PGA Left Channel Current Gain

Address: 0x0b5e
Reset: 0x00



7:0 **GAIN** PGA left channel current gain in automatic analog mode

12.3.59 AUDIO_IN:CUR_PGA_GAIN_R - PGA Right Channel Current Gain

Address: 0x0b5f
Reset: 0x00

	7	6	5	4	3	2	1	0
AUDIO_IN:CUR_PGA_GAIN_R	GAIN							
	r, 0							

7:0 **GAIN** PGA right channel current gain in automatic analog mode

12.3.60 AUDIO_IN:PGA_MAN_SPD - PGA Gain Manual Increase Speed

Address: 0x0b60
Reset: 0x40

	7	6	5	4	3	2	1	0
AUDIO_IN:PGA_MAN_SPD	SPD							
	rw, 64							

7:0 **SPD** Set speed for PGA gain to reach the target gain value

12.3.61 AUDIO_IN:PGA_MAN_TARGET_L - PGA Left Channel Manual Target

Address: 0x0b61
Reset: 0x00

	7	6	5	4	3	2	1	0
AUDIO_IN:PGA_MAN_TARGET_L	TACC	TGAIN						
	r, 0	rw, 0						

7 **TACC** Target left channel value indication

0: PGA target left channel value not reached in manual mode

1: PGA target left channel value was reached in manual mode

6:0 **TGAIN** Set PGA target left channel gain value in manual mode

12.3.62 AUDIO_IN:PGA_VALUE_L - PGA Left Channel Value

Address: 0x0b62
Reset: 0x00

	7	6	5	4	3	2	1	0
AUDIO_IN:PGA_VALUE_L	MUTE	VAL						
	r, 0	r, 0						

7 **MUTE** Left channel mute control
0: Channel is not muted
1: Channel is muted

6:0 **VAL** Current left channel value in manual mode

12.3.63 AUDIO_IN:PGA_FIX_VALUE - PGA Fixed Value

Address: 0x0b63
Reset: 0x80

	7	6	5	4	3	2	1	0
AUDIO_IN:PGA_FIX_VALUE	FGEN	FGAIN						
	rw, 1	rw, 0						

7 **FGEN** Enable fix PGA gain
0: Disables fix PGA gain
1: Enables fix PGA gain

6:0 **FGAIN** Set PGA gain fix value

12.3.64 AUDIO_IN:PGA_R_L - Change PGA Channel Control

Address: 0x0b64
Reset: 0x00

	7	6	5	4	3	2	1	0
AUDIO_IN:PGA_R_L	RSVD							CHG
	rw, 0							rw, 0

0 **CHG** Change PGA L R Channel
0: Channel will not be changed
1: Channel will be changed

12.3.65 AUDIO_IN:PGA_MAN_TARGET_R - PGA Right Channel Manual Target

Address: 0x0b65
Reset: 0x00

	7	6	5	4	3	2	1	0
AUDIO_IN:PGA_MAN_TARGET_R	TACC	TGAIN						
	r, 0	rw, 0						

7	**TACC**	Target right channel value indication **0:** PGA target right channel value not reached in manual mode **1:** PGA target right channel value was reached in manual mode
6:0	**TGAIN**	Set PGA target right channel gain value in manual mode

12.3.66 AUDIO_IN:PGA_VALUE_R - PGA Right Channel Value

Address: 0x0b66
Reset: 0x00

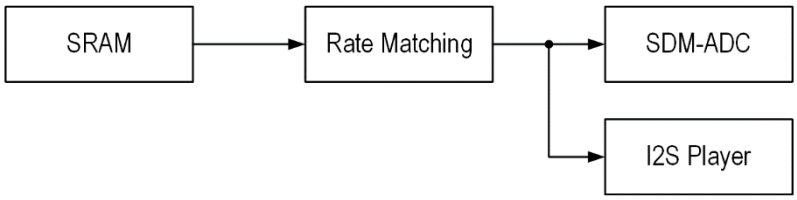
	7	6	5	4	3	2	1	0
AUDIO_IN:PGA_VALUE_R	MUTE	VAL						
	r, 0	r, 0						

7	**MUTE**	Right channel mute control **0:** Channel is not muted **1:** Channel is muted
6:0	**VAL**	Current right channel value in manual mode

12.4 Audio Output Path

Audio output path mainly includes Rate Matching module, SDMDAC (Sigma-Delta Modulation DAC) and I2S Player. The audio data fetched from SRAM is processed by the Rate Matching module, then transferred to the SDM/I2S Player as the input signal.

Figure 23. Audio Output Path



12.4.1 Rate Matching

The rate matching block performs clock rate conversion and data synchronization between the input audio data and the SDM/I2S output.SRAM works in system clock domain with 24MHz/32MHz/48Mhz clocks and the SDM/I2S works between 4MHz and 8MHz.

When needed, the audio data from SRAM is interpolated to the SDM/I2S input rate. If the audio sampling rate is 48kHz and the working clock of SDM/I2S is F_{I2S} , then the interpolation ratio is given as follows: 48KHz/F_{I2S} =BS/0x80000. Where BS is configured in **AUDIO_OUT:I2SCLK:BSL** and **AUDIO_OUT:ASCL_STEP:BSH**

Linear interpolation or delay interpolation is used as shown below.

Figure 24. Linear Interpolation

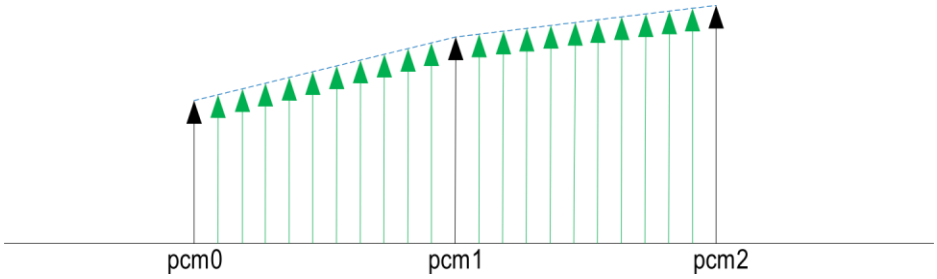
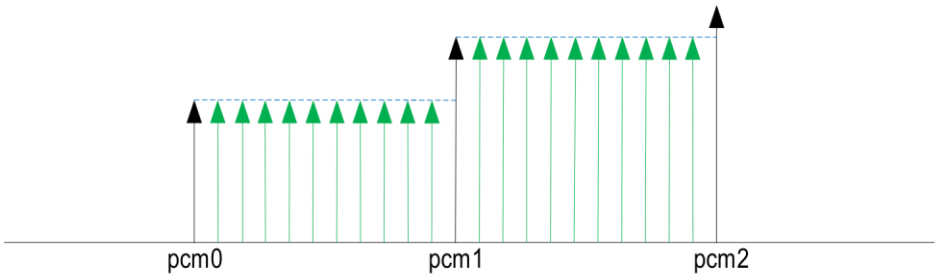


Figure 25. Delay Interpolation

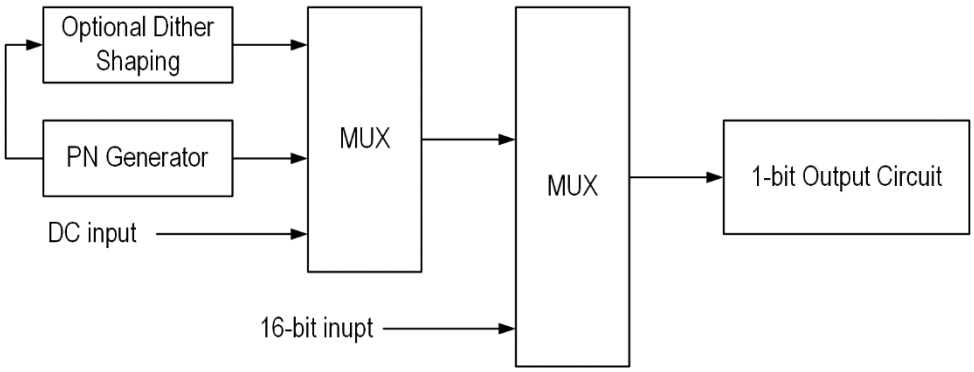


12.4.2 Sigma Delta Modulator (SDM)

The SDM takes 16-bits audio data from SRAM and provides 1-bit modulated output. Only a simple passive filter network is needed to drive the audio device directly.

Dither control can be added to the SDM to avoid spurs in output data. There are three dithering options: PN sequence, PN sequence with Shaping, and DC constant. Only one type of input is allowed at any time.

Figure 26. SDM Block Diagram



12.4.3 Register Configuration

Bit 1 to 4 of **AUDIO_OUT:CTRL** should be set to 1b'1 to enable I2S recorder, ISO player, SDM player and I2S player, while **AUDIO_OUT:CTRL:MODE** is to select either mono or stereo audio output. **AUDIO_OUT:CTRL:HPFEN** should be set to 1b'1 to enable the HPF in audio output path.

AUDIO_OUT:VOL_CTRL controls the volume level.

AUDIO_OUT:PWM_CTRL:IPSEL serves to select either linear interpolation or delay interpolation for the rate matching block. Setting **AUDIO_OUT:PWM_CTRL:IPSEL** to 0b'1 is to select linear interpolation, while clearing the bit is to select delay interpolation.

Input for SDM Dither control is configurable through **AUDIO_OUT:PN_CTRL** and **AUDIO_OUT:PWM_CTRL**.

For the left channel:

- **AUDIO_OUT:PN_CTRL:PNLEN** should be set to 1b'1 to select a constant DC input. When DC input is used, **AUDIO_OUT:CONST_LEFT** serves to configure the input constant value.
- **AUDIO_OUT:PN_CTRL:PNLEN** should be set to 1b'0 to use the PN generator. **AUDIO_OUT:PWM_CTRL:LSEN** serves to enable/mask the dither shaping module. There are two PN generators to generate random dithering sequence. **AUDIO_OUT:PN_CTRL:PN2LEN** or **AUDIO_OUT:PN_CTRL:PN1LEN** enable the corresponding PN generator.
  1. To select the PN sequence as input, **AUDIO_OUT:PN_CTRL:PNLEN** and **AUDIO_OUT:PWM_CTRL:LSEN** should be set to 1b'0 and **AUDIO_OUT:PN_CTRL:PN2LEN** and **AUDIO_OUT:PN_CTRL:PN1LEN** should be set to 1b'1.
  2. To select the PN sequence with Shaping as input, **AUDIO_OUT:PN_CTRL:PNLEN** should be set to 1b'0 and **AUDIO_OUT:PWM_CTRL:LSEN**, **AUDIO_OUT:PN_CTRL:PN2LEN** and **AUDIO_OUT:PN_CTRL:PN1LEN** should be set to 1b'1.
- When PN sequence or PN with Shaping is used, **AUDIO_OUT:PN_CTRL:BPN1L** and **AUDIO_OUT:PN_CTRL:BPN2L** determines the number of bits (ranging from 0 to 16) used in PN1/PN2 generator.

For the right channel:

- **AUDIO_OUT:PN_CTRL:PNREN** should be set to 1b'1 to select constant DC input. When DC input is enabled, **AUDIO_OUT:CONST_RIGHT** serves to configure the input constant value.
- **AUDIO_OUT:PN_CTRL:PNREN** should be set to 1b'0 to use PN generator. **AUDIO_OUT:PWM_CTRL:RSEN** serves to enable/mask the dither shaping module. There are two PN generators to generate random dithering sequence. **AUDIO_OUT:PN_CTRL:PN2REN** and **AUDIO_OUT:PN_CTRL:PN1REN** enable the corresponding PN generator.
  1. To select the PN sequence as input, **AUDIO_OUT:PN_CTRL:PNREN** and **AUDIO_OUT:PWM_CTRL:RSEN** should be set to 1b'0, **AUDIO_OUT:PN_CTRL:PN2REN** and **AUDIO_OUT:PN_CTRL:PN1REN** should be set to 1b'1.
  2. To select the PN sequence with Shaping as input, **AUDIO_OUT:PN_CTRL:PNREN** should be set to 1b'0, **AUDIO_OUT:PWM_CTRL:RSEN**, **AUDIO_OUT:PN_CTRL:PN2REN** and **AUDIO_OUT:PN_CTRL:PN1REN** should be set to 1b'1.
- When PN sequence or PN with Shaping is used, **AUDIO_OUT:PN_CTRL:BPN1R** and **AUDIO_OUT:PN_CTRL:BPN2R** determine the number of bits (ranging from 0 to 16) used in PN1/PN2 generator.

The bits **AUDIO_OUT:I2SCLK:BSL** and **AUDIO_OUT:ASCL_STEP:BSH** are to set BS for the rate matching block, while **AUDIO_OUT:ASCL_TUNE:TBS** is to tune the BS value. BS should be in accordance with the F_{I2S} provided by the SDM/I2S clock.

12.5 Audio Output Path Register Reference

12.5.1 AUDIO_OUT:CTRL - Audio Out Control

Address: 0x0560
Reset: 0x04

	7	6	5	4	3	2	1	0
AUDIO_OUT:CTRL	HPFEN	GRPEN	I2S_EN	I2S_REC	ISO_PLY	SDM_PLY	I2S_PLY	MODE
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0	rw, 1	rw, 0	rw, 0

7 **HPFEN** HPF player enable control bit
0: Disables HPF
1: Enables HPF

6 **GRPEN** GPR player enable control bit
0: Disables GRP
1: Enables GRP

5 **I2S_EN** I2S interface enable control bit
0: Disables I2S interface
1: Enables I2S interface

4 **I2S_REC** I2S recorder enable control bit
0: Disables I2S recorder
1: Enables I2S recorder

3 **ISO_PLY** ISO player enable control bit
0: Disables ISO player
1: Enables ISO player

2 **SDM_PLY** SDM player enable control bit
0: Disables SDM player
1: Enables SDM player

1 **I2S_PLY** I2S player enable control bit
0: Disables I2S player
1: Enables I2S player

0 **MODE** Audio output mode selection
0: Activate stereo mode audio output
1: Activate mono mode audio output

12.5.2 AUDIO_OUT:MIDGRP - Middle of GRP

Address: 0x0561
Reset: 0x40

	7	6	5	4	3	2	1	0
AUDIO_OUT:MIDGRP	MGRP							
	rw, 64							

7:0 **MGRP** Middle of GRP

12.5.3 AUDIO_OUT:VOL_CTRL - Audio Out Volume Control

Address: 0x0562
Reset: 0x40

	7	6	5	4	3	2	1	0
AUDIO_OUT:VOL_CTRL	MUTE	SHIFT					HEN	QEN
	rw, 0	rw, 16					rw, 0	rw, 0

7 **MUTE** Volume mute control

0: Disables mute volume

1: Enables mute volume

6:2 **SHIFT** Current volume shift left

1 **HEN** Enable half volume add

0: Disables half volume increase

1: Enables half volume increase

0 **QEN** Enable quarter volume add

0: Disables quarter volume increase

1: Enables quarter volume increase

12.5.4 AUDIO_OUT:PWM_CTRL - Audio Out PWM Control

Address: 0x0563
Reset: 0x64

	7	6	5	4	3	2	1	0
AUDIO_OUT:PWM_CTRL	I2SCHS	RSEN	LSEN	RSVD		IPSEL	EN	MULF
	rw, 0	rw, 1	rw, 1	rw, 0		rw, 1	rw, 0	rw, 0

7 **I2SCHS** I2S input left/right channel swap

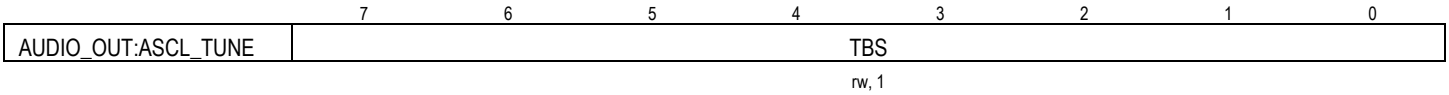
0: No input channel swapping

1: Input channel swapping

6	**RSEN**	Right channel shaping enable **0:** Right channel shaping disable **1:** Right channel shaping enabled
5	**LSEN**	Left channel shaping enable **0:** Left channel shaping disable **1:** Left channel shaping enabled
2	**IPSEL**	Interpolation selection **0:** Select delay interpolation **1:** Select linear interpolation
1	**EN**	Enable PWM **0:** Disables PWM **1:** Enables PWM
0	**MULF**	PWM multiply **0:** No doubling the PWM **1:** Doubling the PWM

12.5.5 AUDIO_OUT:ASCL_TUNE - Tune Step

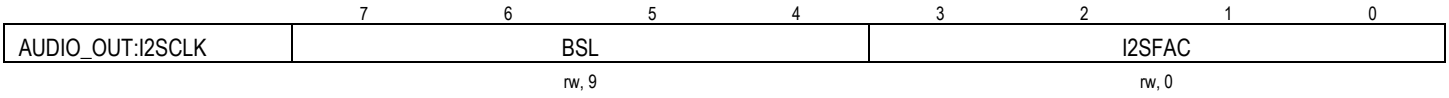
Address: 0x0564
Reset: 0x01



7:0	**TBS**	Tune step for rate matching block

12.5.6 AUDIO_OUT:I2SCLK - I2S Clock configuration

Address: 0x0565
Reset: 0x90



7:4	**BSL**	Low 4 bits of rate matching block step [3:0]
3:0	**I2SFAC**	I2S clock factor

12.5.7 AUDIO_OUT:ASCL_STEP - Rate Matching Block Step

Address: 0x0566
Reset: 0x00c4

	7	6	5	4	3	2	1	0
AUDIO_OUT:ASCL_STEP[1]	BSH							
	rw, 0							
AUDIO_OUT:ASCL_STEP[0]	BSH							
	rw, 196							

15:0 **BSH** High 16 bits of rate matching block step [19:4]

12.5.8 AUDIO_OUT:PN_CTRL - PN Generator Control

Address: 0x0568
Reset: 0x00104050

	7	6	5	4	3	2	1	0
AUDIO_OUT:PN_CTRL[3]	RSVD	PNREN	PNLEN	BPN2R				
	rw, 0	rw, 0	rw, 0	rw, 0				
AUDIO_OUT:PN_CTRL[2]	RSVD	EXSMD	CLKI	BPN1R				
	rw, 0	rw, 0	rw, 0	rw, 16				
AUDIO_OUT:PN_CTRL[1]	RSVD	PN1REN	PN2REN	BPN2L				
	rw, 0	rw, 1	rw, 0	rw, 0				
AUDIO_OUT:PN_CTRL[0]	RSVD	PN1LEN	PN2LEN	BPN1L				
	rw, 0	rw, 1	rw, 0	rw, 16				

30 **PNREN** Right Channel PN Selection

0: Right channel use PN generator

1: Right channel use constant value

29 **PNLEN** Left Channel PN Selection

0: Left channel use PN generator

1: Left channel use constant value

28:24 **BPN2R** Right channel PN2 bits

Range from 0 to 16

22 **EXSMD** SDM data exchange

0: Not exchange data between SDMs

1: Exchange data between SDMs

21 **CLKI** Audio clock inverter

0: Clock is inverted

1: Clock is not inverted

20:16	**BPN1R**	Right channel PN1 bits Range from 0 to 16
14	**PN1REN**	Right channel PN1 enable **0:** Disables PN generator 1 of right channel **1:** Enables PN generator 1 of right channel
13	**PN2REN**	Right channel PN2 enable **0:** Disables PN generator 2 of right channel **1:** Enables PN generator 2 of right channel
12:8	**BPN2L**	Left channel PN2 bits Range from 0 to 16
6	**PN1LEN**	Left channel PN1 enable **0:** Disables PN generator 1 of left channel **1:** Enables PN generator 1 of left channel
5	**PN2LEN**	Left channel PN2 enable **0:** Disables PN generator 2 of left channel **1:** Enables PN generator 2 of left channel
4:0	**BPN1L**	Left channel PN1 bits Range from 0 to 16

12.5.9 AUDIO_OUT:CONST_LEFT - Constant Left Channel

Address: 0x056c
Reset: 0x0000

	7	6	5	4	3	2	1	0
AUDIO_OUT:CONST_LEFT[1]	CCHL							
	rw, 0							
AUDIO_OUT:CONST_LEFT[0]	CCHL							
	rw, 0							

15:0	**CCHL**	DC input constant of left channel

12.5.10 AUDIO_OUT:CONST_RIGHT - Constant Right Channel

Address: 0x056e
Reset: 0x0000

	7	6	5	4	3	2	1	0
AUDIO_OUT:CONST_RIGHT[1]	CCHR							
	rw, 0							
AUDIO_OUT:CONST_RIGHT[0]	CCHR							
	rw, 0							

15:0 **CCHR** DC input constant of right channel

13. Quadrature Decoder

The RYZ012 embeds one quadrature decoder (QDEC) that is designed mainly for applications such as wheel. The QDEC provides optional input debouncing to filter out jitter on the two phase inputs, and it generates smooth square waves for the two phase.

13.1 Input Pin Selection

The QDEC supports a two-channel input. A different pin from Port A to D can be assigned to each channel by **QDEC:CHA** and **QDEC:CHB**. In this context, the corresponding pin must be activated as input (IE) and deactivated as output (ODIS).

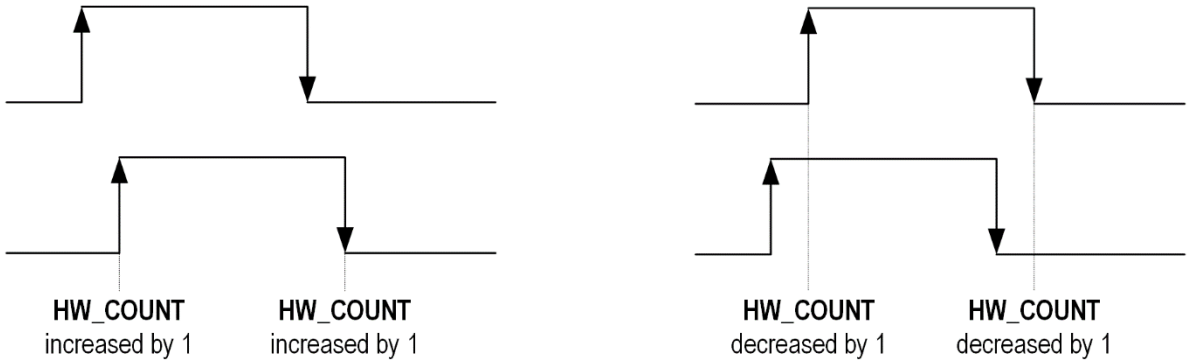
Table 12. Input Pin Selection

CHA | CHB	Pin
2	PB6
3	PB7
4	PC2
5	PC3
7	PD7

13.2 Common Mode and Double Accuracy Mode

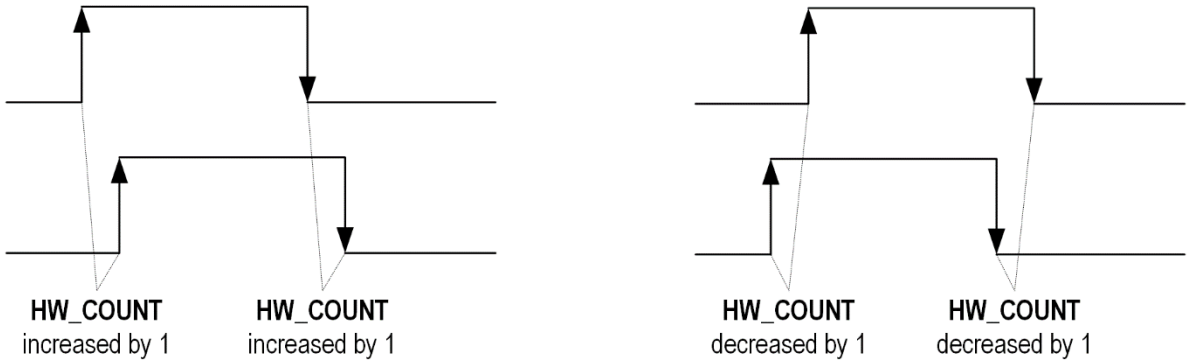
QDEC:DOUBLE:EN serves to select Common Mode or double accuracy mode. In Common Mode, for each wheel rolling step, two pulse edges (rising edge or falling edge) are generated. If **QDEC:DOUBLE:EN** is cleared to select common mode, the QDEC Counter value (real time counting value) is increased/decreased by 1 when the same rising/falling edges are detected from the two phase signals

Figure 27. Common Mode



If **QDEC:DOUBLE:EN** is set to 1b'1 to select double accuracy mode, the **QDEC:COUNT** is increased/decreased by 1 on each rising/falling edge of the two phase signals. The **QDEC:COUNT** is increased/decreased by 2 for one wheel rolling.

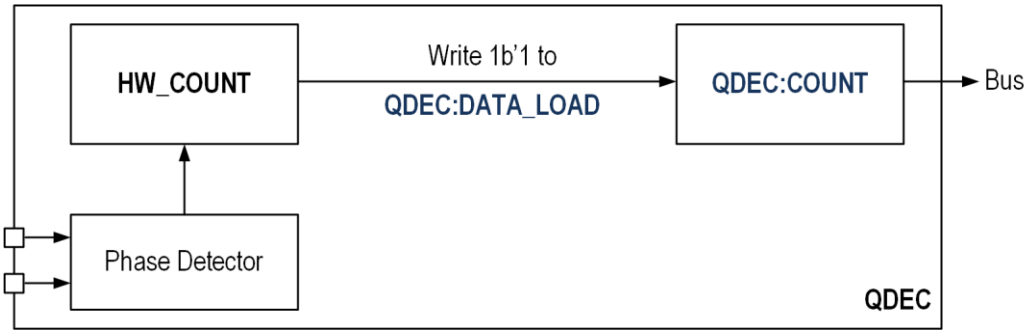
Figure 28. Double Accuracy Mode



13.3 Read Real-time Counting Value

The Hardware Counter value cannot be read directly through software, and the counting value in address **QDEC:COUNT** cannot be updated automatically. To read the real-time counting value, first write **QDEC:DATA_LOAD** with 1b'1 to load the hardware counter data into the **QDEC:COUNT**, before the register is read. The register is cleared automatically after it has been read.

Figure 29. Read Real-time Counting Value



13.4 QDEC Reset

QDEC:RST serves to reset the QDEC. The QDEC Counter value is cleared to zero.

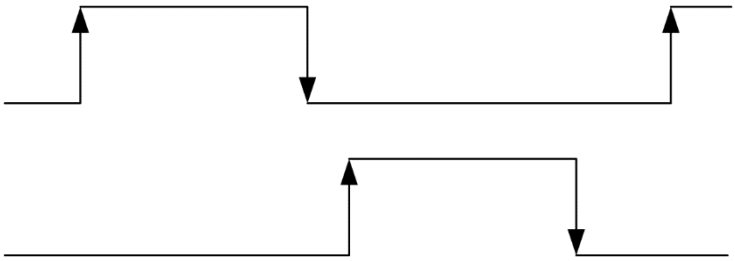
13.5 Other Configuration

The QDEC supports hardware debouncing. **QDEC:GC:FTIME** serves to set the filtering window duration. All jitter with period less than the value is filtered out and therefore does not trigger a count change.

QDEC:GC:POL serves to set the input signal initial polarity.

QDEC:GC:SHU serves to enable the shuttle mode. Shuttle mode allows non-overlapping two phase signals as shown below.

Figure 30. Shuttle Mode



13.6 Timing

Figure 31. Timing Sequence

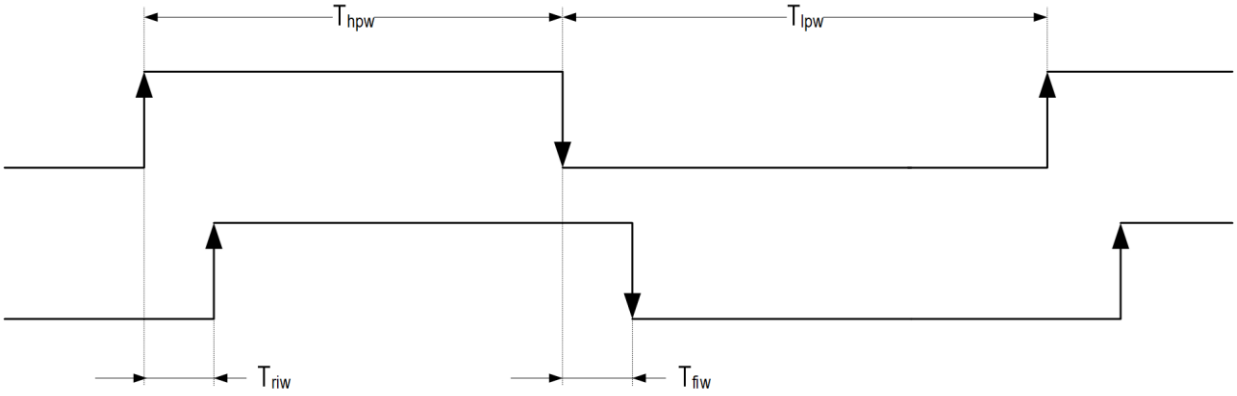


Table 13. Timing Constraints

Time Interval	Minimum Value (n = QDEC:GC:FTIME)
T_{hpw} (High-level pulse width)	$2^{(n+1)}$ * clk_32kHz * 3
T_{lpw} (Low-level pulse width)	$2^{(n+1)}$ * clk_32kHz * 3
T_{riw} (Interval width between two rising edges)	$2^{(n+1)}$ * clk_32kHz
T_{fiw} (Interval width between two falling edges)	$2^{(n+1)}$ * clk_32kHz

QDEC module works based on 32kHz clock to ensure it can work in suspend mode. The debouncing function regards any signal with a width lower than the threshold (that is $2^{(n+1)}$ * clk_32kHz) as jitter. Therefore, effective signals input from Channel A and B should contain high/low level with width T_{hpw} /T_{lpw} more than the threshold. The 2^n * clk_32kHz clock is used to synchronize input signal of QDEC module, so that the interval between two adjacent rising/falling edges from Channel A and B (marked as T_{riw} and T_{fiw}) should exceed $2^{(n+1)}$ * clk_32kHz.

When the timing requirements above are met, the QDEC module recognizes wheel rolling times correctly.

13.7 Register Reference

13.7.1 QDEC:COUNT - QDEC Pulse Edge Count

Address: 0x00d0
Reset: 0x00

	7	6	5	4	3	2	1	0
QDEC:COUNT	COUNT							
	r, 0							

7:0 **COUNT** Pulse edge number counting value

Register will be cleared by reading

13.7.2 QDEC:GC - QDEC General Configuration

Address: 0x00d1
Reset: 0x00

	7	6	5	4	3	2	1	0
QDEC:GC	RSVD		SHU	POL	RSVD	FTIME		
	rw, 0		rw, 0	rw, 0	rw, 0	rw, 0		

5 **SHU** Enable Shuttle Mode which allows non-overlapping two phase signals

0: Disables Shuttle Mode

1: Enables Shuttle Mode

4 **POL** Input signal polarity selection

0: Input signal is initial LOW

1: Input signal is initial HIGH

2:0 **FTIME** Set filter time

Can filter 2^n * clk_32k * 2 width deglitch

13.7.3 QDEC:CHA - QDEC Input Channel A

Address: 0x00d2
Reset: 0x00

7	6	5	4	3	2	1	0
QDEC:CHA	RSVD					INSEL	
	rw, 0					rw, 0	

2:0 **INSEL** Input pin select for channel A

0: Select Port A Pin 2

1: Select Port A Pin A

2: Select Port B Pin 6

3: Select Port B Pin 7

4: Select Port C Pin 2

5: Select Port C Pin 3

6: Select Port D Pin 6

7: Select Port D Pin 7

13.7.4 QDEC:CHB - QDEC Input Channel B

Address: 0x00d3
Reset: 0x01

7	6	5	4	3	2	1	0
QDEC:CHB	RSVD					INSEL	
	rw, 0					rw, 1	

2:0 **INSEL** Input pin select for channel B

0: Select Port A Pin 2

1: Select Port A Pin A

2: Select Port B Pin 6

3: Select Port B Pin 7

4: Select Port C Pin 2

5: Select Port C Pin 3

6: Select Port D Pin 6

7: Select Port D Pin 7

13.7.5 QDEC:RST - QDEC Reset Control

Address: 0x00d6
Reset: 0x00

7	6	5	4	3	2	1	0
QDEC:RST	RSVD						RST
	rw, 0						rw, 0

0 **RST** QDEC Reset

0: Is set automatically when QDEC was reset

1: If bit is set to 1 data can be loaded

13.7.6 QDEC:DOUBLE - QDEC Mode Configuration

Address: 0x00d7
Reset: 0x00

7	6	5	4	3	2	1	0
QDEC:DOUBLE	RSVD						EN
	rw, 0						rw, 0

0 **EN** QDEC Mode selection

0: Enables common mode

1: Enables double accuracy mode

13.7.7 QDEC:DATA_LOAD - QDEC Data Status

Address: 0x00d8
Reset: 0x00

7	6	5	4	3	2	1	0
QDEC:DATA_LOAD	RSVD						LOAD
	rw, 0						rw, 0

0 **LOAD** Data load status

0: Is set automatically when the data is completely loaded

1: If bit is set to 1 data can be loaded

14. SAR-ADC

The RYZ012 integrates one SAR ADC module, which can be used to sample analog input signals such as battery voltage, temperature sensor, mono or stereo audio signals. The SAR ADC is disabled by default. To power on the ADC, the analog register **SCTL:APCTRL:ADC** should be set as 1b'0.

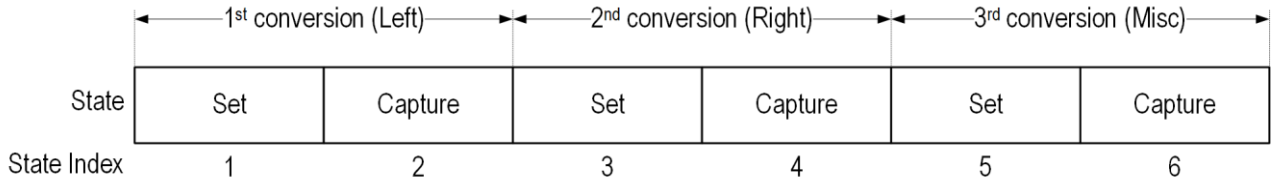
The ADC clock is derived from the external 24MHz crystal source, with a frequency dividing factor that is configurable through the analog register **SAR_ADC:CLKDIV:ADCDIV**. The ADC clock frequency is F_{ADC} = 24MHz / (ADCDIV + 1).

14.1 ADC Control

14.1.1 ADC Channel Selection

The SAR ADC supports up to three channels including left channel, right channel and Misc channel, which are sampled sequentially. The sampling sequence for each channel consists of a Set state and a Capture state. The bit of the analog register **SAR_ADC:CHEN:SCNT** controls the max state index. As shown in the figure below, **SCNT** should be set to 6 to capture all three channels.

Figure 32. Conversion Sequence for all Channels



The left and Misc channel can be enabled independently through **SAR_ADC:CHEN:LEN** and **SAR_ADC:CHEN:MEN**. When the left channel is enabled, the right channel can be enabled through **SAR_ADC:CHEN:REN**. To sample mono audio signals, the left channel should be enabled. To sample stereo audio signals, both the left channel and the right channel should be enabled.

14.1.2 ADC Set State

The length of Set state for left, right and Misc channel is configurable through the analog register **SAR_ADC:CAPCFG:ST**. Set state duration is defined as T_{sd} = **ST** / 24MHz.

Each Set state serves to set ADC control signals for current channel through corresponding analog registers.

To select differential input mode **SAR_ADC:CHCFG:MODEL** (left channel), **SAR_ADC:CHCFG:MODER** (right channel) or **SAR_ADC:CHCFG:MODEM** (Misc channel) must be set as 1b'1.

The positive and negative inputs for left channel, right channel and Misc channel in differential mode are selected through the registers **SAR_ADC:CHL_INPUT**, **SAR_ADC:CHR_INPUT** and **SAR_ADC:CHM_INPUT**. The positive input is selected through **PCHSEL** and the negative input is selcted through **NCHSEL**

Set reference voltage V_{REF} with **SAR_ADC:VREF_CTRL:VREFL** (left channel), **SAR_ADC:VREF_CTRL:VREFR** (right channel) or **SAR_ADC:VREF_CTRL:VREFM** (Misc channel). ADC maximum input range is the determined by the ADC reference voltage.

Set scaling factor for ADC analog input to 1 (default) or 1/8 **SAR_ADC:APSC:VAL**. By setting this scaling factor, ADC maximum input range can be extended based on the V_{REF} .

For example, suppose the V_{REF} is set as 1.2V:

Since the scaling factor is 1 by default, the ADC maximum input range should be 0 to 1.2V (negative input is GND) and -1.2V to +1.2V (negative input is ADC GPIO pin). If the scaling factor is set as 1/8, in theory ADC maximum input range should change to 0 to 9.6V (negative input is GND) and -9.6V to +9.6V (negative input is ADC GPIO pin). But limited by input voltage of the chips PAD, the actual range is narrower. Set resolution as 8/10/12/14 bits with **SAR_ADC:CHCFG:RESL** (left channel), **SAR_ADC:CHCFG:RESR** or **SAR_ADC:CHCFG:RESM** (Misc channel).

ADC data is always 15-bit format no matter what the resolution is set. For example, 14 bits resolution indicates ADC data consists of 14-bit valid data and 1-bit sign extension bit. Set a sampling time that determines the speed to stabilize input signals with **SAR_ADC:TSAMP:CNUML** (left channel), **SAR_ADC:TSAMP:CNUMR** (right channel) or **SAR_ADC:TSAMP:CNUMM** (Misc channel). Sampling time is defined as T_{samp} = TSAMP / F_{ADC} . The lower sampling cycle, the shorter ADC convert time.

See section **Programmable Gain Amplifier (PGA)** for configuration details of the PGA gain in Boost stage and Gain stage.

14.1.3 ADC Capture State

For the left, right and Misc channels, at the beginning of each Capture state, a run signal is issued automatically to start an ADC sampling and conversion process; at the end of each Capture state, the ADC output data is captured.

The length of the Capture state of the Misc channel is defined as T_{cd} = CTM / 24MHz, where CTM is configured in the analog registers **SAR_ADC:CAPCFG:CTML** and **SAR_ADC:CAPCFG:CTMH**.

Similarly, the length of Capture state for left and right channel is defined as T_{cd} = CTLR / 24MHz, where CTLR is configured in the analog registers **SAR_ADC:CAPCFG:CTLRL** and **SAR_ADC:CAPCFG:CTLRH**.

The status flag **SAR_ADC:DATM:VLD** is set at the end of Capture state to indicate the ADC data is valid, and this flag bit will be cleared automatically. The 15-bit ADC output data for Misc channel can be read from **SAR_ADC:DATM:DAT**.

The total duration T_{td} , which is the sum of the length of the Set state and the Capture state of all channels, determines the sampling rate.

Sampling frequency is defined as $F_s = 1 / T_{td}$

14.1.4 Use Cases

Table 14 lists all possible channel configurations and shows how they are setup in the **SAR_ADC:CHEN** register. In addition, the total sampling time and the sampling order are shown in the table.

Table 14. Configuration Setting for Different ADC Use Cases

Use Case	SAR_ADC:CHEN Setting	Total Duration	Sampling Order
Stereo Audio and Misc	**LEN** = 1; **REN** = 1; **MEN** = 1 **SCNT** = 6	T_{td} = (3*ST+CTM+2*CTLR) / 24MHz	Left, Right, Misc
Stereo Audio	**LEN** = 1; **REN** = 1; **MEN** = 0 **SCNT** = 4	T_{td} = (2*ST+2*CTLR) / 24MHz	Left, Right
Mono Audio and Misc	**LEN** = 1; **REN** = 0; **MEN** = 1 **SCNT** = 4	T_{td} = (2*ST+CTM+CTLR) / 24MHz	Left, Misc
Mono Audio	**LEN** = 1; **REN** = 0; **MEN** = 0 **SCNT** = 2	T_{td} = (ST+CTLR) / 24MHz	Left
Misc	**LEN** = 0; **REN** = 0; **MEN** = 1 **SCNT** = 2	T_{td} = (ST+CTM) / 24MHz	Misc

14.1.4.1 Example with Detailed Settings

This example shows the register setting details for 3-channel sampling of left, right and Misc channels. The ADC must be switched on by setting 1b'0 in register **SCTL:APCTRL:ADC**. **SAR_ADC:CHEN:LEN** and **SAR_ADC:CHEN:REN** and **SAR_ADC:CHEN:MEN** should be set as 1b'1 to enable the corresponding channels. The max state index should be set as "6" by setting **SAR_ADC:CHEN:SCNT**. Under use of **SAR_ADC:CLKDIV:ADCDIV** = 5 the ADC frequency must be divided to 4Mhz.

F_{ADC} = 24M / (ADCDIV + 1) = 4Mhz

Table 15. Register Setting for L/R/M Channel

Function	Register Setting		
	Left	Right	Misc
Set T_{sd} (Set state duration)	ST = 10 T_{sd} = ST / 24MHz = 10 / 24MHz = 0.417µs		
Set T_{cd} (Capture state duration)	**SAR_ADC:CAPCFG:CTLRH** = 0 **SAR_ADC:CAPCFG:CTLRL** = 170 T_{cd} = CTLR / 24MHz = 170 / 24MHz = 7.1µs		**SAR_ADC:CAPCFG:CTMH** = 0 **SAR_ADC:CAPCFG:CTML** = 130 T_{cd} = CTM / 24MHz = 130 / 24MHz = 5.4µs
T_{td} (total duration)	T_{td} = (CTM + 3 * ST + 2 * CTLR) / 24MHz = 500 / 24MHz = 20.83µs		
F_s (Sampling frequency)	F_s = 1 / T_{td} = 24MHz / 500 = 48kHz		
Select differential input	**SAR_ADC:CHCFG:MODEL** = 1 differential input	**SAR_ADC:CHCFG:MODER**= 1 differential input	**SAR_ADC:CHCFG:MODEM** = 1 differential input
Set input channel	**SAR_ADC:CHL_INPUT** = 0x12 Select B0 and B1 as positive input and negative input	**SAR_ADC:CHR_INPUT** = 0x34 Select B2 and B3 as positive input and negative input	**SAR_ADC:CHM_INPUT** = 0xaf Select C5 as positive input, select GND as negative input
Set reference voltage VREF	**SAR_ADC:VREF_CTRL:VREFL** = 0 V_{REF} = 0.6V	**SAR_ADC:VREF_CTRL:VREFR** = 1 V_{REF} = 0.9V	**SAR_ADC:VREF_CTRL:VREFM** = 2 V_{REF} = 1.2V
Set scaling factor for ADC analog input	**SAR_ADC:APSC** = 0 scaling factor: 1		
	ADC maximum input range: -0.6 to +0.6V	ADC maximum input range: -0.9 to +0.9V	ADC maximum input range: 0 to +1.2V
Set resolution	**SAR_ADC:CHCFG:RESL** = 1 operates with 10 bit resolution	**SAR_ADC:CHCFG:RESR** = 2 operates with 12 bit resolution	**SAR_ADC:CHCFG:RESM** = 3 operates with 14 bit resolution
Set T_{samp} (determines the speed to stabilize input before sampling)	**SAR_ADC:TSAMP:CNUML** = 1 T_{samp} = adc_tsamp / F_{ADC} = 6/4MHz = 1.5µs	**SAR_ADC:TSAMP:CNUMR** = 2 T_{samp} = adc_tsamp / F_{ADC} = 9/4MHz = 2.25µs	**SAR_ADC:TSAMP:CNUMM** = 3 T_{samp} = adc_tsamp / F_{ADC} = 12/4MHz = 3µs

14.2 Analog Register Reference

14.2.1 SAR_ADC:VREF_CTRL - SAR Reference Voltage Configuration

Address: 0x00e7
Reset: 0x00

	7	6	5	4	3	2	1	0
SAR_ADC:VREF_CTRL	RSVD		VREFM		VREFR		VREFL	
	rw, 0		rw, 0		rw, 0		rw, 0	

5:4 **VREFM** V_{REF} Misc channel selection

00: Select V_{REF} = 0.6V

01: Select V_{REF} = 0.9V

10: Select V_{REF} = 1.2V

11: Not used

3:2 **VREFR** V_{REF} right channel selection

00: Select V_{REF} = 0.6V

01: Select V_{REF} = 0.9V

10: Select V_{REF} = 1.2V

11: Not used

1:0 **VREFL** V_{REF} left channel selection

00: Select V_{REF} = 0.6V

01: Select V_{REF} = 0.9V

10: Select V_{REF} = 1.2V

11: Not used

14.2.2 SAR_ADC:CHM_INPUT - SAR Input Misc Channel Configuration

Address: 0x00e8
Reset: 0x00

	7	6	5	4	3	2	1	0
SAR_ADC:CHM_INPUT	PCHSEL				NCHSEL			
	rw, 0				rw, 0			

7:4 **PCHSEL** Positive input selection for Misc channel

0: Select no input channel

1: Select Port B Pin 0 as input

2: Select Port B Pin 1 as input

3: Select Port B Pin 2 as input

4: Select Port B Pin 3 as input

5: Select Port B Pin 4 as input

6: Select Port B Pin 5 as input

7: Select Port B Pin 6 as input

8: Select Port B Pin 7 as input

9: Select Port C Pin 4 as input

10: Select Port C Pin 5 as input

11: Select pga_p Pin 0 (PGA left-channel positive output)

12: Select pga_p Pin 1 (PGA right-channel positive output)

13: Select tempsensor_p (temperature sensor positive output)

14: Not used

15: Not used

3:0	**NCHSEL**	Negative input selection for Misc channel **0:** Select no input channel **1:** Select Port B Pin 0 as input **2:** Select Port B Pin 1 as input **3:** Select Port B Pin 2 as input **4:** Select Port B Pin 3 as input **5:** Select Port B Pin 4 as input **6:** Select Port B Pin 5 as input **7:** Select Port B Pin 6 as input **8:** Select Port B Pin 7 as input **9:** Select Port C Pin 4 as input **10:** Select Port C Pin 5 as input **11:** Select pga_n Pin 0 (PGA left-channel negative output) **12:** Select pga_n Pin 1 (PGA right-channel negative output) **13:** Select tempsensor_n (temperature sensor negative output) **14:** Select GND **15:** Select GND

14.2.3 SAR_ADC:CHL_INPUT - SAR Input Left Channel Configuration

Address: 0x00e9
Reset: 0x00

	7	6	5	4	3	2	1	0
SAR_ADC:CHL_INPUT	PCHSEL				NCHSEL			
	rw, 0				rw, 0			

7:4 **PCHSEL** Positive input selection for left channel

0: Select no input channel

1: Select Port B Pin 0 as input

2: Select Port B Pin 1 as input

3: Select Port B Pin 2 as input

4: Select Port B Pin 3 as input

5: Select Port B Pin 4 as input

6: Select Port B Pin 5 as input

7: Select Port B Pin 6 as input

8: Select Port B Pin 7 as input

9: Select Port C Pin 4 as input

10: Select Port C Pin 5 as input

11: Select pga_p Pin 0 (PGA left-channel positive output)

12: Select pga_p Pin 1 (PGA right-channel positive output)

13: Select tempsensor_p (temperature sensor positive output)

14: Not used

15: Not used

3:0	**NCHSEL**	Negative input selection for left channel **0:** Select no input channel **1:** Select Port B Pin 0 as input **2:** Select Port B Pin 1 as input **3:** Select Port B Pin 2 as input **4:** Select Port B Pin 3 as input **5:** Select Port B Pin 4 as input **6:** Select Port B Pin 5 as input **7:** Select Port B Pin 6 as input **8:** Select Port B Pin 7 as input **9:** Select Port C Pin 4 as input **10:** Select Port C Pin 5 as input **11:** Select pga_n Pin 0 (PGA left-channel negative output) **12:** Select pga_n Pin 1 (PGA right-channel negative output) **13:** Select tempsensor_n (temperature sensor negative output) **14:** Select GND **15:** Select GND

14.2.4 SAR_ADC:CHR_INPUT - SAR Input Right Channel Configuration

Address: 0x00ea
Reset: 0x00

	7	6	5	4	3	2	1	0
SAR_ADC:CHR_INPUT	PCHSEL				NCHSEL			
	rw, 0				rw, 0			

7:4 **PCHSEL** Positive input selection for right channel

0: Select no input channel

1: Select Port B Pin 0 as input

2: Select Port B Pin 1 as input

3: Select Port B Pin 2 as input

4: Select Port B Pin 3 as input

5: Select Port B Pin 4 as input

6: Select Port B Pin 5 as input

7: Select Port B Pin 6 as input

8: Select Port B Pin 7 as input

9: Select Port C Pin 4 as input

10: Select Port C Pin 5 as input

11: Select pga_p Pin 0 (PGA left-channel positive output)

12: Select pga_p Pin 1 (PGA right-channel positive output)

13: Select tempsensor_p (temperature sensor positive output)

14: Not used

15: Not used

3:0 **NCHSEL** Negative input selection for right channel

0: Select no input channel

1: Select Port B Pin 0 as input

2: Select Port B Pin 1 as input

3: Select Port B Pin 2 as input

4: Select Port B Pin 3 as input

5: Select Port B Pin 4 as input

6: Select Port B Pin 5 as input

7: Select Port B Pin 6 as input

8: Select Port B Pin 7 as input

9: Select Port C Pin 4 as input

10: Select Port C Pin 5 as input

11: Select pga_n Pin 0 (PGA left-channel negative output)

12: Select pga_n Pin 1 (PGA right-channel negative output)

13: Select tempsensor_n (temperature sensor negative output)

14: Select GND

15: Select GND

14.2.5 SAR_ADC:CHCFG - SAR General Channel Configuration

Address: 0x00eb
Reset: 0x0333

	7	6	5	4	3	2	1	0
SAR_ADC:CHCFG[1]	RSVD	MODEM	MODER	MODEL	RSVD		RESM	
	rw, 0	rw, 0	rw, 0	rw, 0	rw, 0		rw, 3	
SAR_ADC:CHCFG[0]	RSVD		RESR		RSVD		RESL	
	rw, 0		rw, 3		rw, 0		rw, 3	

14 **MODEM** Input mode selection for Misc channel

0: Select standard mode

1: Select differential mode

13 **MODER** Input mode selection for left channel

0: Select standard mode

1: Select differential mode

12 **MODEL** Input mode selection for left channel

0: Select standard mode

1: Select differential mode

9:8	**RESM**	Misc channel resolution selection **00:** Select 8-bit resolution **01:** Select 10-bit resolution **10:** Select 12-bit resolution **11:** Select 14-bit resolution
5:4	**RESR**	Right channel resolution selection **00:** Select 8-bit resolution **01:** Select 10-bit resolution **10:** Select 12-bit resolution **11:** Select 14-bit resolution
1:0	**RESL**	Left channel resolution selection **00:** Select 8-bit resolution **01:** Select 10-bit resolution **10:** Select 12-bit resolution **11:** Select 14-bit resolution

14.2.6 SAR_ADC:TSAMP - SAR Sampling Time Configuration

Address: 0x00ed
Reset: 0x0000

	7	6	5	4	3	2	1	0
SAR_ADC:TSAMP[1]	RSVD				CNUMM			
	rw, 0				rw, 0			
SAR_ADC:TSAMP[0]	CNUMR				CNUML			
	rw, 0				rw, 0			

11:8 **CNUMM** ADC clock cycle number selection for Misc channel

0: 3 cycles sampling time

1: 6 cycles sampling time

2: 9 cycles sampling time

3: 12 cycles sampling time

4: 15 cycles sampling time

5: 18 cycles sampling time

6: 21 cycles sampling time

7: 24 cycles sampling time

8: 27 cycles sampling time

9: 30 cycles sampling time

10: 33 cycles sampling time

11: 36 cycles sampling time

12: 39 cycles sampling time

13: 42 cycles sampling time

14: 45 cycles sampling time

15: 48 cycles sampling time

7:4 **CNUMR** ADC clock cycle number selection for right channel

For values see CNUMM

3:0 **CNUML** ADC clock cycle number selection for left channel

For values see CNUMM

14.2.7 SAR_ADC:CAPCFG - SAR Channel Capture Configuration

Address: 0x00ef
Reset: 0x000000

	7	6	5	4	3	2	1	0
SAR_ADC:CAPCFG[2]	CTMH		CTLRH		ST			
	rw, 0		rw, 0		rw, 0			
SAR_ADC:CAPCFG[1]	CTLRL							
	rw, 0							
SAR_ADC:CAPCFG[0]	CTML							
	rw, 0							

23:22	**CTMH**	State length of 24M clock cycle number that is occupied by the Capture state for Misc channel (high byte)
21:20	**CTLRH**	State length of 24M clock cycle number that is occupied by the Capture state for left and right channel (high byte)
19:16	**ST**	State length of 24M clock cycle number that is occupied by the Set state for left, right and Misc channel
15:8	**CTLRL**	State length of 24M clock cycle number that is occupied by the Capture state for left and right channel (low byte)
7:0	**CTML**	State length of 24M clock cycle number that is occupied by the Capture state for Misc channel (low byte)

14.2.8 SAR_ADC:CHEN - SAR Channel Enable Control

Address: 0x00f2
Reset: 0x00

	7	6	5	4	3	2	1	0
SAR_ADC:CHEN	RSVD	SCNT			RSVD	MEN	REN	LEN
	rw, 0	rw, 0			rw, 0	rw, 0	rw, 0	rw, 0

6:4	**SCNT**	Set total length for sampling state machine (that is max state index)
2	**MEN**	Enable Misc channel **0:** Disables channel **1:** Enables channel
1	**REN**	Enable right channel **0:** Disables channel **1:** Enables channel
0	**LEN**	Enable left channel **0:** Disables channel **1:** Enables channel

14.2.9 SAR_ADC:CLKDIV - SAR Clock Divider Configuration

Address: 0x00f4
Reset: 0x03

	7	6	5	4	3	2	1	0
SAR_ADC:CLKDIV	RSVD						ADCDIV	
	rw, 0						rw, 3	

2:0 **ADCDIV** Set ADC clock divider (derive from external 24M crystal)

F_{ADC} = 24M / (ADCDIV + 1)

14.2.10 SAR_ADC:DATM - SAR Data Misc Channel

Address: 0x00f7
Reset: 0x00

	7	6	5	4	3	2	1	0
SAR_ADC:DATM[1]	VLD	DAT						
	ro, 0	ro, 0						
SAR_ADC:DATM[0]	DAT							
	ro, 0							

15 **VLD** ADC data status indication

This bit is set by hardware when the data of the last ADC conversion has been written to the DAT field. It is cleared at the beginning of every new conversion.

0: Data in field DAT is not valid

1: Data in field DAT is valid

14:0 **DAT** Data from Misc channel

14.2.11 SAR_ADC:APSC - Analog Pre-scaler

Address: 0x00fa
Reset: 0x00

	7	6	5	4	3	2	1	0
SAR_ADC:APSC	VAL		RSVD					
	rw, 0		rw, 0					

7:6 **VAL** Analog input pre-scaling factor

00: Select 1 as factor

01: Reserved

10: Reserved

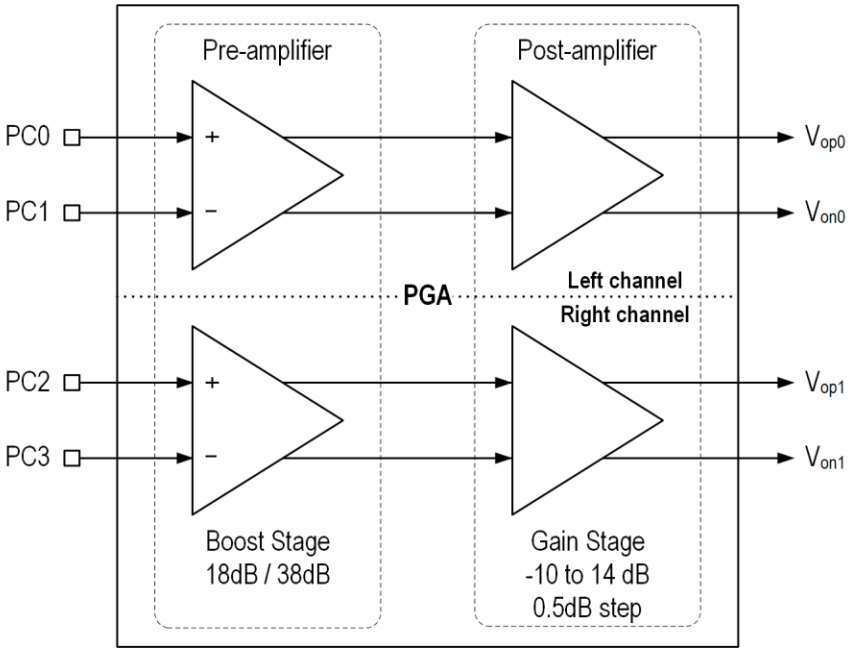
11: Select 0.125 as factor

15. Programmable Gain Amplifier (PGA)

The PGA supports two channels including left channel and right channel and each channel consists of a Boost stage pre-amplifier and a Gain stage post-amplifier.

The PGA is used in combination with the audio and ADC module: by adjusting the gain of pre-amplifier and post-amplifier, the PGA can amplify mono or stereo differential input audio signals from specific AMIC pins before ADC sampling.

Figure 33. Block Diagram of PGA



Notes:

V_{ip} <0>, V_{in} <0>: Positive / Negative input of PGA left channel;
V_{op} <0>, V_{on} <0>: Positive / Negative output of PGA left channel;
V_{ip} <1>, V_{in} <1>: Positive / Negative input of PGA right channel;
V_{op} <1>, V_{on} <1>: Positive / Negative output of PGA right channel.

15.1 Power-on / down

Both PGA channels are powered down by default. To power on the PGA channels, the bits **PGAL** and **PGAR** in register **SCTL:APCTRL** should be set to 1b'0.

15.2 Input Channel

The PGA input pins are fixed to PC0 and PC1 as left channel positive and negative inputs and PC2 and PC3 as right channel positive and negative input. The analog register **PGA:VINSEL** must be set as 0x55 to enable both channel inputs.

15.3 Adjust Gain

To adjust the PGA gain, the ALC of the audio module should be configured as analog mode, and the following three cases can apply:

Auto regulate

If auto regulate function is enabled, the user can set an initial PGA gain. The (AMIC input * current PGA gain) is compared with the pre-configured high volume target, low volume target and volume noise level, and the PGA gain automatically adjusts within the pre-configured range.

See **Automatic Regulation in Analog Mode** for further details.

Manual mode 1

If manual mode 1 is enabled, the PGA gain is directly adjustable via digital register **AUDIO_IN:PGA_FIX_VALUE**: **FGEN** serves to set gain for the pre-amplifier as 18dB (1b'0, default) or 38dB (1b'1); while register **FGAIN** serves to set gain for the post-amplifier as -10dB (0x0, default) - 14dB (0x30) with step of 0.5dB. The total PGA gain should be the sum of the two gain values.

Refer to section **Manual Regulation in Analog Mode** for details.

Manual mode 2

If manual mode 2 is enabled, the PGA gain will be automatically adjusted to the pre-configured target gain value with the pre-configured speed.

Refer to section **Manual Regulation in Analog Mode** for details.

15.4 Analog Register Reference

15.4.1 PGA:VINSEL - PGA Channel Input Configuration

Address: 0x00fd
Reset: 0x00

	7	6	5	4	3	2	1	0
PGA:VINSEL	INRN		INRP		INLN		INLP	
	rw, 0		rw, 0		rw, 0		rw, 0	

7:6 **INRN** Right channel negative input source selection

Gate off all input with pga_pd_r

00: Select Port C Pin 3 as input

01: Select no input

10: Select no input

11: Select no input

5:4 **INRP** Right channel positive input source selection

Gate off all input with pga_pd_r

00: Select Port C Pin 2 as input

01: Select no input

10: Select no input

11: Select no input

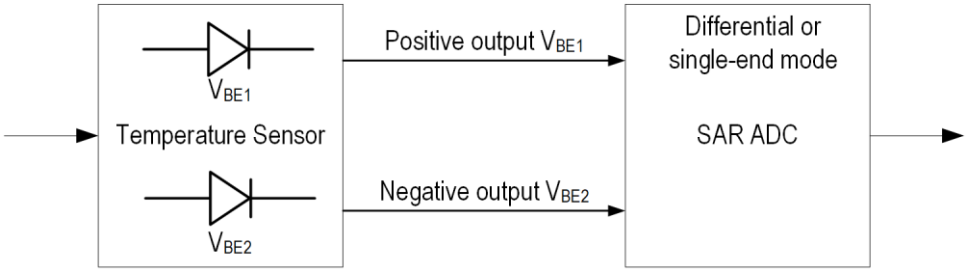
3:2	**INLN**	Left channel negative input source selection Gate off all input with pga_pd_l **00:** Select Port C Pin 1 as input **01:** Select no input **10:** Select no input **11:** Select no input
1:0	**INLP**	Left channel positive input source selection Gate off all input with pga_pd_l **00:** Select Port C Pin 0 as input **01:** Select no input **10:** Select no input **11:** Select no input

16. Temperature Sensor

The RYZ012 integrates a temperature sensor and it is used in combination with the SAR ADC to detect real-time temperature.

The temperature sensor is disabled by default. The analog register **SCTL:PDC1:TSPD** must be cleared to enable the temperature sensor. The temperature sensor embeds two diodes. It takes the real-time temperature (T) as input, and outputs two-way forward voltage drop (V_{BE}) signals of diodes as positive and negative output respectively.

Figure 34. Block Diagram of Temperature Sensor



The difference of the two-way V_{BE} signals (V_{BE}) is determined by the real-time temperature T, as shown below: V_{BE} = 130mV + 0.51mV / °C * (T - (-40°C)) = 130mV + 0.51mV / °C * (T + 40°C)

In this formula, "130mV" indicates the value of V_{BE} at the temperature of "-40°C".

To detect the temperature, the positive and negative output of the temperature sensor should be enabled as the input channels of the SAR ADC. The ADC will convert the two-way V_{BE} signals into digital signal.

When the ADC is configured in differential mode, the positive and negative output of the temperature sensor should be configured as differential input of the ADC. The ADC should initiate one operation and obtain one output signal (ADCOUT); therefore,

V_{BE} = ADCOUT /(2^N - 1) * V_{REF} .

In the formula, N and V_{REF} indicate the selected resolution and reference voltage of the SAR ADC.

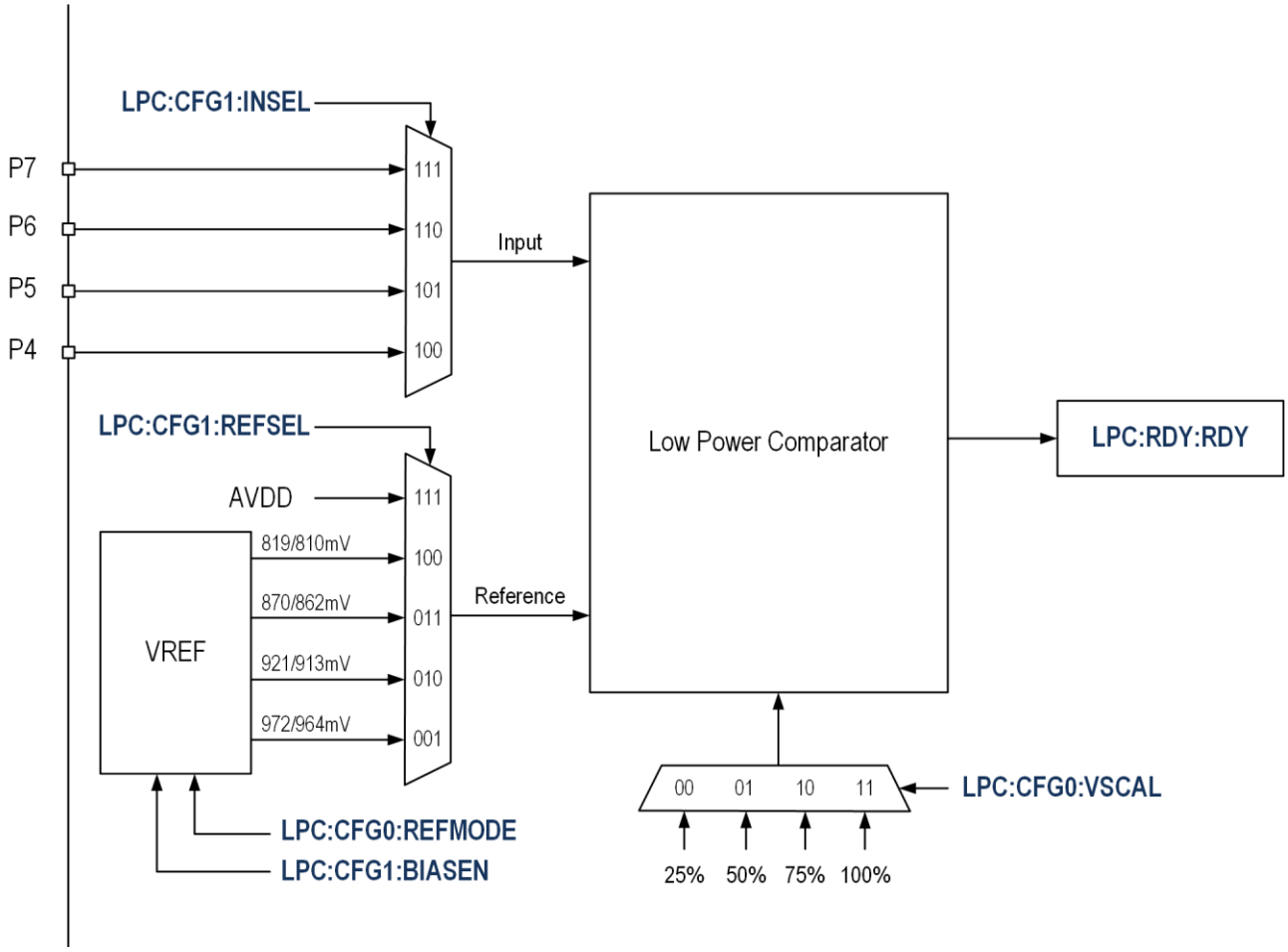
Then the real-time temperature T can be calculated according to the V_{BE} .

17. Low Power Comparator

The RYZ012 embeds a low power comparator. This comparator takes two inputs: input derived from external PortB (PB4-PB7), and reference input derived from internal reference or AVDD.

By comparing the input voltage multiplied by selected scaling coefficient with reference input voltage, the low power comparator outputs high or low level accordingly.

Figure 35. Block Diagram of Low Power Comparator



17.1 Power-on/down

The low power comparator is powered down by default. The bit **LPCPD** in the analog register **SCTL:PDC1** serves to control the power state of the low power comparator. By clearing this bit, the comparator is powered on; by setting this bit to 1b'1, the comparator is powered down. To use the low power comparator, first set **LPCPD** as 1b'0, then the 32K RC clock source is enabled as the comparator clock.

17.2 Input Channel Selection

Input channel is selectable from the PortB (PB4-PB7) through the analog register **LPC:CFG1:REFSEL**.

17.3 Mode and Reference Selection

Generally, it is needed to clear both the **LPC:CFG0:REFMODE** and **LPC:CFG1:BIASEN** to select the normal mode. In normal mode, the internal reference is derived from UVLO and has higher accuracy, but current bias is larger (10μA); reference voltage input channel is selectable from internal reference of 972mV, 921mV, 870mV and 819mV, as well as PB0, PB3, AVDD3 and float.

To select the low power mode, both the **LPC:CFG0:REFMODE** and **LPC:CFG1:BIASEN** should be set as 1b'1. In low power mode, the internal reference is derived from Bandgap and has lower accuracy, but current bias is decreased to 50nA; reference voltage input channel is selectable from internal reference of 964mV, 913mV, 862mV and 810mV, as well as PB0, PB3, AVDD3 and float.

17.4 Select Scaling Coefficient

Equivalent reference voltage equals the selected reference input voltage divided by scaling coefficient.
The analog register **LPC:CFG0:VSCAL** serves to select one of the four scaling options: 25%, 50%, 75% and 100%.

17.5 Low Power Comparator Output

The low power comparator output is determined by the comparison result of the value of [input voltage * scaling] and reference voltage input. The comparison principle is shown as below:

- If the value of [input voltage * scaling] is larger than reference voltage input, the output will be low (0).
- If the value of [input voltage * scaling] is lower than reference voltage input, the output will be high (1).
- If the value of [input voltage * scaling] equals reference voltage input, or input channel is selected as float, the output will be uncertain. User can read the output of the low power comparator via **LPC:RDY:RDY**. The output of the low power comparator can be used as signal to wakeup system from low power modes.

17.6 Analog Register Reference

17.6.1 LPC:CFG0 - LPC Configuration

Address: 0x000b
Reset: 0x18

	7	6	5	4	3	2	1	0
LPC:CFG0	RSVD		VSCAL		REFMODE	RSVD		
	rw, 0		rw, 1		rw, 1	rw, 0		

5:4 **VSCAL** Reference voltage scaling

00: 25% reference voltage scaling

01: 50% reference voltage scaling

10: 75% reference voltage scaling

11: 100% reference voltage scaling

3 **REFMODE** Reference mode selection

0: Select normal mode

1: Select low power mode

17.6.2 LPC:CFG1 - LPC Configuration

Address: 0x000d
Reset: 0x80

	7	6	5	4	3	2	1	0
LPC:CFG1	BIASEN	REFSEL			RSVD	INSEL		
	rw, 1	rw, 0			rw, 0	rw, 0		

7 **BIASEN** Enable 10µA current bias (low active)

0: Enables 10µA current bias

1: Disables 10µA current bias

6:4 **REFSEL** Low power comparator reference voltage selection

000: Reference voltage is floating in normal and low power mode

001: Select 972mV as reference voltage in normal mode

Select 964mV as reference voltage in low power mode

010: Select 921mV as reference voltage in normal mode

Select 913mV as reference voltage in low power mode

011: Select 870mV as reference voltage in normal mode

Select 862mV as reference voltage in low power mode

100: Select 819mV as reference voltage in normal mode

Select 810mV as reference voltage in low power mode

111: Select AVDD3 as reference voltage in normal and low power mode

Others: Reserved

2:0 **INSEL** Low power comparator reference voltage input channel selection

000: Select no input channel

100: Select Port B Pin 4 as input

101: Select Port B Pin 5 as input

110: Select Port B Pin 6 as input

111: Select Port B Pin 7 as input

Others: Reserved

17.6.3 LPC:RDY - LPC Status

Address: 0x0088
Reset: 0x00

	7	6	5	4	3	2	1	0
LPC:RDY	RSVD	RDY	RSVD					
	r, 0	r, 0	r, 0					

6 **RDY** LPC result (comparator) ready indication

18. AES

The RYZ012 embeds an AES module with encryption and decryption function. The 128-bit plaintext input in combination with the AES key is converted into the output ciphertext through encryption; otherwise, the 128-bit ciphertext in combination of key can also be converted into 128-bit plaintext through decryption.

The AES hardware accelerator provides automatic encryption and decryption. It only takes 1000 system clock cycles to encrypt/decrypt an 128-bit block. Supposed the system clock is 20MHz, the time needed for AES encryption/decryption is 50μs.

18.1 RISC Mode

For RISC mode, configuration of related registers is as follows:

1. Set the value of key through writing **AES:KEY**.
2. Select AES encryption or decryption by setting **AES:CTRL:SEL** as 1b'0 or 1b'1, respectively.
3. For encryption method, write registers **AES:DAT** for four times to set the 128-bit plaintext. After encryption, the 128-bit ciphertext can be obtained by reading **AES:DAT** for four times.
4. For decryption method, write registers **AES:DAT** for four times to set the 128-bit ciphertext. After decryption, the 128-bit plaintext can be obtained by reading **AES:DAT** for four times.
5. **AES:CTRL:IDRDY** will be cleared automatically after quartic writing of **AES:DAT**.
6. **AES:CTRL:ODRDY** will be set as 1b'1 automatically after encryption/decryption, and then cleared automatically after quartic reading of **AES:DAT**.

18.2 DMA Mode

As for DMA mode, it is only needed to configure the value of key and encryption/decryption method for AES module. See item number 1 and 2 in section **RISC Mode** .

18.3 AES-CCM

The AES-CCM (Counter with the CBC-MAC) mode is disabled by default. The AES output is directly determined by current encryption and decryption, irrespective of previous encryption and decryption result.

If **AES:CTRL:CCMEN** is set as 1b'1 to enable AES-CCM mode, the AES output takes the previous encryption and decryption result into consideration.

18.4 Register Reference

18.4.1 AES:CTRL - AES Control

Address: 0x0540
Reset: 0x00

	7	6	5	4	3	2	1	0
AES:CTRL	CCMEN	RSVD				ODRDY	IDRDY	SEL
	rw, 0	rw, 0				ro, 0	ro, 0	rw, 0

7 **CCMEN** Enable AES-CCM mode for AES encryption and decryption

0: Disables CCM mode for further AES processing

1: Enables CCM mode for further AES processing

2 **ODRDY** Signals the processing of the data in the output buffer

0: Output data needed

1: Output data ready

1 **IDRDY** Signals the processing of the data in the input buffer

0: Input data needed

1: Input data ready

0 **SEL** Selection to decrypt or encrypt current data

0: Selects encryption of the data

1: Selects decryption of the data

18.4.2 AES:DAT - AES Data

Address: 0x0548
Reset: 0x00000000

	7	6	5	4	3	2	1	0
AES:DAT[3]	DAT3							
	rw, 0							
AES:DAT[2]	DAT2							
	rw, 0							
AES:DAT[1]	DAT1							
	rw, 0							
AES:DAT[0]	DAT0							

7:0, 15:8, 23:16, 31:24 **DATx** AES Input/Output data

18.4.3 AES:KEY - AES Key Data

Address: 0x0550
Reset: 0x00

	7	6	5	4	3	2	1	0
AES:KEY[15]	KEY15							
	rw, 0							
AES:KEY[14]	KEY14							
	rw, 0							
AES:KEY[13]	KEY13							
	rw, 0							
AES:KEY[12]	KEY12							
	rw, 0							
AES:KEY[11]	KEY11							
	rw, 0							
AES:KEY[10]	KEY10							
	rw, 0							
AES:KEY[9]	KEY9							
	rw, 0							
AES:KEY[8]	KEY8							
	rw, 0							
AES:KEY[7]	KEY7							
	rw, 0							
AES:KEY[6]	KEY6							
	rw, 0							
AES:KEY[5]	KEY5							
	rw, 0							
AES:KEY[4]	KEY4							
	rw, 0							
AES:KEY[3]	KEY3							
	rw, 0							
AES:KEY[2]	KEY2							
	rw, 0							
AES:KEY[1]	KEY1							
	rw, 0							
AES:KEY[0]	KEY0							
	rw, 0							

7:0, 15:8, 23:16, 31:24, 39:32, 47:40, 55:48, 63:56, 71:64, 79:72, 87:80, 95:88, 103:96, 111:104, 119:112, 127:120	**KEYx**	AES-Key Data AES-Key Data buffer to corresponding byte (128 bit key)

19. Bluetooth Low Energy/802.15.4/2.4GHz RF Transceiver

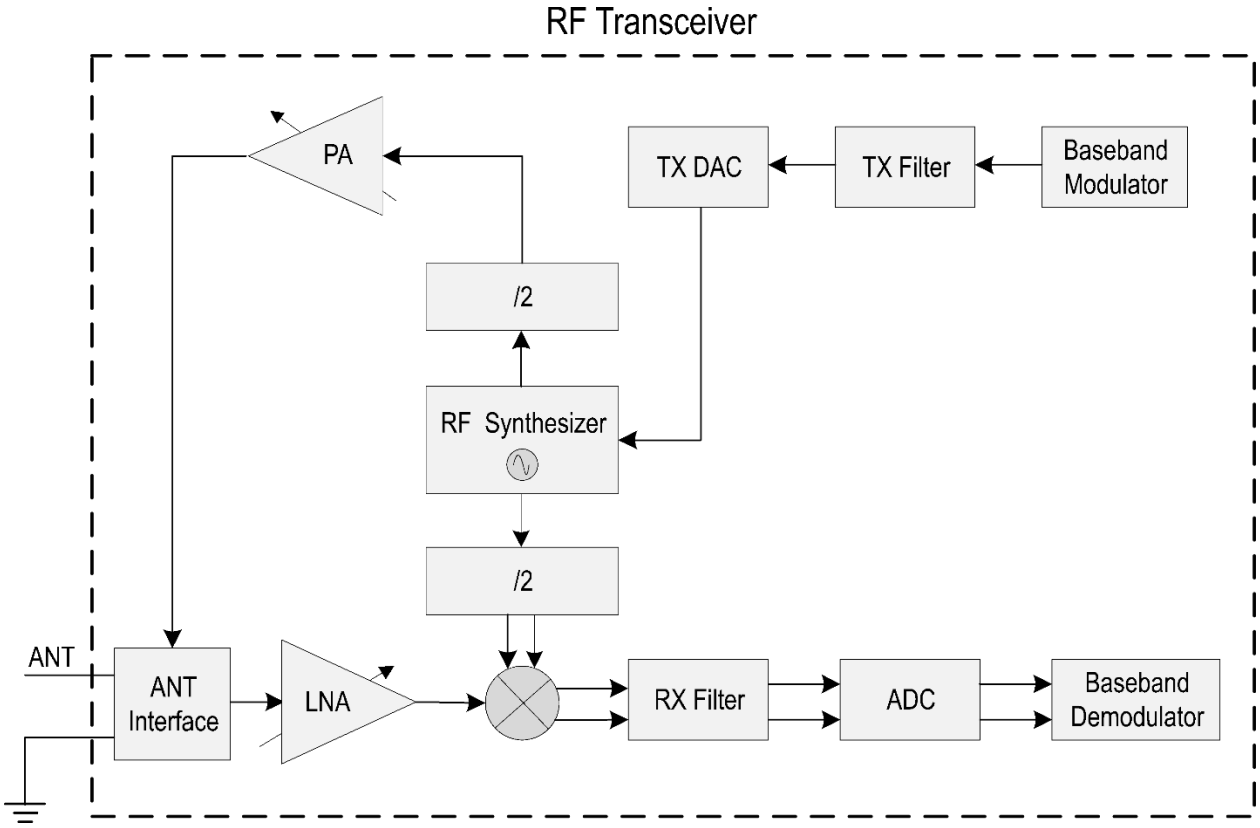
19.1 Block Diagram

The RYZ012 integrates an advanced Bluetooth LE/802.15.4/2.4GHz RF transceiver. The RF transceiver works in the worldwide 2.4GHz ISM (Industrial Scientific Medical) band.

The transceiver consists of a fully integrated RF synthesizer, a Power Amplifier (PA), a Low Noise Amplifier (LNA), a TX filter, a RX filter, a TX DAC, an ADC, a modulator and a demodulator. The transceiver can be configured to work in standard-compliant 1Mbps Bluetooth LE mode, 2Mbps enhancement Bluetooth LE mode, 125kbps Bluetooth LE long range mode (S8), 500kbps Bluetooth LE long-range mode (S2), IEEE 802.15.4 standard-compliant 250kbps mode, and Proprietary 1Mbps, 2Mbps, 250kbps and 500kbps mode.

The internal PA can deliver a maximum 10dBm output power, avoiding the need for an external RF PA.

Figure 36. Block Diagram of RF Transceiver



19.2 Baseband

The baseband is disabled by default. The corresponding API is available for user to power on/down the baseband and enable/disable clock, so that the baseband can be turned on/off flexibly.

The baseband contains dedicated hardware logic to perform fast AGC control, access code correlation, CRC checking, data whitening, encryption/decryption and frequency hopping logic.

The baseband supports all features required by Bluetooth 5 and 802.15.4 specification.

19.2.1 Packet Format

Packet format in standard 1Mbps Bluetooth LE mode is shown as Table 16:

Table 16. Packet Format in Standard 1Mbps Bluetooth LE Mode

LSB	Preamble (1 octet)	Access Address (4 octets)	PDU (2–257 octets)	CRC (3 octets)	MSB

Packet length 80bit–2120bit (80–2120μs at 1Mbps).
Packet format in standard 2Mbps Bluetooth Low Energy mode is shown as Table 17:

Table 17. Packet Format in Standard 2Mbps Bluetooth LE Mode

LSB	Preamble (2 octet)	Access Address (4 octets)	PDU (2–257 octets)	CRC (3 octets)	MSB

Packet format in standard 500kbps/125kbps Bluetooth Low Energy mode is shown as Table 18:

Table 18. Packet Format in Standard 500kbps/125kbps Bluetooth LE Mode

LSB	Preamble (10 octet)	Access Address (4 octets)	CI (2 bits)	TERM1 (3 bits)	PDU (2-257 octets)	PDU (2–257 octets)	CRC (3 octets)	TERM2 (3 bits)	MSB

Packet format in 250kbps 802.15.4 mode is shown as Table 19:

Table 19. Packet Format in 802.15.4 Mode

LSB	Preamble (4 octets)	SFD (1 octet)	Frame length (1 octet)	PSDU (Variable 0–127 octets)	CRC (2 octets)	MSB
	PHR		PHY payload			

Packet format in 2.4GHz Proprietary mode is shown as Table 20:

Table 20. Packet Format in Proprietary Mode

LSB	Preamble (8 bits)	Address code (configurable 3–5 bytes)	Packet Controller + Payload (1–33 bytes)	CRC (1-2 bytes)	MSB

19.2.2 RSSI and Frequency Offset

The RYZ012 provides accurate RSSI (Receiver Signal Strength Indicator) and frequency offset indication.

- RSSI can be read from the 1byte at the tail of each received data packet.
- If no data packet is received (for example to perform channel energy measurement when no desired signal is present), real-time RSSI can also be read from specific registers which will be updated automatically.
- RSSI monitoring resolution can reach ±1dB.
- Frequency offset can be read from the 2bytes at the tail of the data packet. Valid bits of actual frequency offset may be less than 16bits, and different valid bits correspond to a different tolerance range.

20. Electrical Characteristics

20.1 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the BLW8252 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions can affect device reliability.

Table 21. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{DD}	Supply Voltage	All AVDD, DVDD and VDD_IO pins must have the same voltage	-0.3	3.6	V
V_{In}	Voltage on Input Pin		-0.3	V_{DD} + 0.3	V
V_{Out}	Output Voltage		0	V_{DD}	V
T_{Str}	Storage Temperature Range		-65	150	°C
T_{Sld}	Soldering Temperature			260	°C

CAUTION:

Stresses above those listed in Table 21 can cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

20.2 Recommended Operating Conditions

Table 22. Recommended Operating Conditions

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		1.8	3.3	3.6	V
t_R	Supply Rise Time (from 1.6V to 1.8V)				10	ms
T_{Opr}	Operating Temperature Range		-40		85	°C

20.3 Electrical Characteristics

Table 23. Electrical Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
I_{Rx}	RX current	Whole chip		5.3		mA
I_{Tx}	TX current	Whole chip at 0dBm with DCDC		4.8		mA
I_{Deep1}	Deep sleep with 8kB SRAM retention			1	3.1	uA
	Deep sleep with 16kB SRAM retention			1.2	3.3	uA
	Deep sleep with 32kB SRAM retention			1.4	3.5	uA
I_{Deep2}	Deep sleep without SRAM retention			0.4		uA

Table 24. AC Characteristics (V_{DD} = 3.3V, T_A = 25°C)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
Digital Inputs/Outputs						
V_{IH}	Input High Voltage		$0.7V_{DD}$		V_{DD}	V
V_{IL}	Input Low Voltage		VSS		$0.3V_{DD}$	V
V_{OH}	Output High Voltage		$0.9V_{DD}$		V_{DD}	V
V_{OL}	Output Low Voltage		VSS		$0.1V_{DD}$	V
RF Parameters						
	RF Frequency Range	Programmable in 1MHz step	2380		2500	MHz
	Data Rate	Bluetooth LE/2.4G Proprietary 1Mbps, ±250kHz deviation Bluetooth LE/2.4G Proprietary 2Mbps, ±500kHz deviation Bluetooth LE 125kbps, ±250kHz deviation Bluetooth LE500kbps, ±250kHz deviation 802.15.4 250kbps, ±500kHz deviation 2.4G Proprietary 500kbps, ±125kHz deviation 2.4G Proprietary 250kbps, ±62.5kHz deviation				
RSSI						
	RSSI Range		-100		10	dBm
	Resolution			1		dB

Table 25. Bluetooth LE, 1 Mbps Mode

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
RX Performance[a] (±250kHz Deviation)						
1Mbps	Sensitivity			-96		dBm
	Frequency Offset Tolerance		-250		+300	kHz
	Co-channel Rejection	Wanted signal at -67dBm		11		dB
+1/-1 MHz offset	In-band Blocking Rejection(Equal Modulation Interference)	Wanted signal at -67dBm		-1/-3		dB
+2/-2 MHz offset				-37/-39		dB
>=3MHz offset	In-band Blocking Rejection (Equal Modulation Interference)	Wanted signal at -67dBm		-42		dB
	Image Rejection	Wanted signal at -67dBm		-37		dB
TX Performance						
	Output Power, Maximum Setting			10	12	dBm
	Output power, Minimum Setting			-45		dBm
	Programmable Output Power range		55			dB
	Modulation 20dB Bandwidth			1.4		MHz

[a] For actual sensitivity level of Bluetooth LE 1Mbps mode, see Bluetooth 5 specification.

Table 26. Bluetooth LE, 2 Mbps Mode

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
RX performance[b] (±500kHz Deviation)						
2Mbps	Sensitivity			-93		dBm
	Frequency Offset Tolerance		-300		+200	kHz
	Co-channel Rejection	Wanted signal at -67dBm		10		dB
+2/-2 MHz offset	In-band Blocking Rejection	Wanted signal at -67dBm		-6/-6		dB
+4/-4 MHz offset				-39/-38		dB
>4MHz offset				-42		dB
	Image Rejection	Wanted signal at -67dBm		-25		dB

TX Performance						
	Output Power, Maximum Setting			10	12	dBm
	Output Power, Minimum Setting			-45		dBm
	Programmable Output Power Range		55			dB
	Modulation 20dB Bandwidth			2.5		MHz

[b] For actual sensitivity level of Bluetooth LE 2Mbps mode, see Bluetooth 5 specification.

Table 27. Bluetooth LE, 500 kbps Mode

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
RX Performance[c] (±250kHz Deviation)						
500kbps	Sensitivity			-99		dBm
	Frequency Offset Tolerance		-150		+50	kHz
	Co-channel Rejection	Wanted signal at -67dBm		1		dB
+1/-1 MHz offset	In-band Blocking Rejection(Equal Modulation Interference)	Wanted signal at -67dBm		-34/-36		dB
+2/-2 MHz offset				-42/-42		dB
>3MHz offset				-42		dB
	Image Rejection	Wanted signal at -67dBm		-42		dB
TX Performance						
	Output Power, Maximum setting			10	12	dBm
	Output Power, Minimum Setting			-45		dBm
	Programmable Output Power Range		55			dB
	Modulation 20dB Bandwidth			1.4		MHz

[c] For actual sensitivity level of Bluetooth LE 500kbps mode, see Bluetooth 5 specification.

Table 28. Bluetooth LE, 125 kbps Mode

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
RX Performance[d] (±250kHz Deviation)						
125kbps	Sensitivity			-101		dBm
	Frequency Offset Tolerance		-150		+50	kHz
	Co-channel Rejection	Wanted signal at -67dBm		3		dB
+1/-1 MHz offset	In-band Blocking Rejection(Equal Modulation Interference)	Wanted signal at -67dBm		-32/-34		dB
+2/-2 MHz offset				-42/-42		dB
>=3MHz offset				-42		dB
	Image Rejection	Wanted signal at -67dBm		-42		dB
TX Performance						
	Output Power, Maximum Setting			10	12	dBm
	Output Power, Minimum Setting			-45		dBm
	Programmable Output Power Range		55			dB
	Modulation 20dB Bandwidth			1.4		MHz

[d] For actual sensitivity level of Bluetooth LE 125kbps mode, see Bluetooth 5 specification.

Table 29. IEEE 802.15.4, 250kbps

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
Rx performance[e] (±500kHz Deviation)						
250kbps	Sensitivity			-99.5		dBm
	Frequency Offset Tolerance		-300		+300	kHz
	Adjacent Channel Rejection (-1/+1 Channel)	Wanted signal at -82dBm		-42/-42		dB
	Adjacent Channel Rejection (-2/+2 Channel)	Wanted signal at -82dBm		-42/-42		dB
EVM	Error vector magnitude	Max (10dBm) power output			2%	
Tx Performance						
	Output Power, Maximum Setting			10	12	dBm
	Output power, Minimum Setting			-45		dBm
	Programmable Output		55			dB
	Power Range					
	Modulation 20dB Bandwidth			2.7		MHz

[e] For actual sensitivity level of IEEE802.15.4 mode, see 802.15.4 specification.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
Module Internal 24MHz Crystal						
f_{NOM}	Nominal Frequency			24		MHz
f_{TOL}	Frequency Tolerance		-20		+20	ppm
Module internal 32.768kHz Crystal						
f_{NOM}	Nominal Frequency			32.768		kHz
f_{TOL}	Frequency Tolerance		-30		+30	ppm
24MHz RC Oscillator						
f_{NOM}	Nominal Frequency			24		MHz
f_{TOL}	Frequency Tolerance	On chip calibration		1		%
32kHz RC Oscillator						
f_{NOM}	Nominal Frequency			32		kHz
f_{TOL}	Frequency Tolerance	On chip calibration		0.03		%
	Calibration Time			3		ms

ADC						
DNL	Differential Nonlinearity	10-bit resolution mode			1	LSB
INL	Integral Nonlinearity	10-bit resolution mode			2	LSB
SINAD	Signal-to-Noise and Distortion Ratio	F_{in} = 1kHz, f_S = 16kHz	70			dB
ENOB	Effective Number of Bits			10.5		bits
F_S	Sampling Frequency			200		ksps

20.4 SPI Characteristics

Table 30. SPI Characteristics (over process, voltage 1.9–3.6V, and T_A = -40 to +85˚C)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
F_{CK}	CK Frequency	Slave			4	MHz
	CK Duty Cycle Clock	Master		50		%
	DI Setup Time	Slave	30			ns
		Master	90			ns
	DI Hold Time	Slave	10			ns
		Master	90			ns
	CK Low to DO Valid Time	Slave			30	ns
		Master			120	ns
	CN Setup Time	Master/Slave	60			ns
	CN High to DI Tri-state[a]	Master				ns

[a] Note: Master actively stops reading during transmission, and Slave releases its driver DO and turns to tri-state.

20.5 I2C Characteristics

Table 31. I2C Characteristics (over process, voltage 1.9–3.6V, and T_A = -40 to +85°C)

Symbol	Parameter	Conditions	Standard Mode		Fast Mode		Units
			Min	Max	Min	Max	
F_{SCL}	SCL Frequency			100		400	kHz
T_R	Rise Time of SDA and SCL Signals			1000		300	ns
T_F	Fall Time of SDA and SCL Signals			300		300	ns
$T_{HD;STA}$	START Condition Hold Time		4		0.6		µs
$T_{HD;DAT}$	Data Hold Time		0	3.45		0.9	µs
$T_{SU;DAT}$	Data Setup Time		250		100		ns
$T_{SU;STO}$	STOP Condition Setup Time		4		0.6		µs

20.6 Flash Characteristics

Table 32. Flash Characteristics (T_A = -40 to +85°C)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
	Retention Period		20			Year
	Number of Erase Cycles		100k			Cycle
	V_{DD} for Programming	This refers to the SoC supply	1.65		2.0	V
	Sector Size			4		kB
T_{PP}	Page Programming Time			1.6	6	ms
T_{SE}	Sector Erase Time			150	500	ms
T_{BE}	Block Erase Time(32kB/64kB)			0.5/0.8	2.0/3.0	s
I_P	Program Current				10	mA
I_E	Erase Current				10	mA

21. Integration Instructions

Module integrators must adhere to the integration guidelines in given in the following sections to maintain compliance with the certification requirements while providing the maximum performance.

Note: Any modifications to the RYZ012 modules are not allowed and may void the users permission to operated the module.

21.1 List of applicable FCC / ISED rules

FCC	ISED
47 CFR Part 15 Subpart C §15.247	RSS-247, Issue 2, February 2017

21.2 Specific Operational Use Conditions

21.2.1 North America (FCC)

The module must not be operated at power levels above 10.0dBm. Host devices that need higher output power may not be marketed without prior re-certification.

21.2.2 Europe (RED)

The module must not be operated at power levels above 8.4dBm. Host devices that need higher output power may not be marketed in regions covered by RED regulation without prior re-certification.

21.2.3 Japan (MIC)

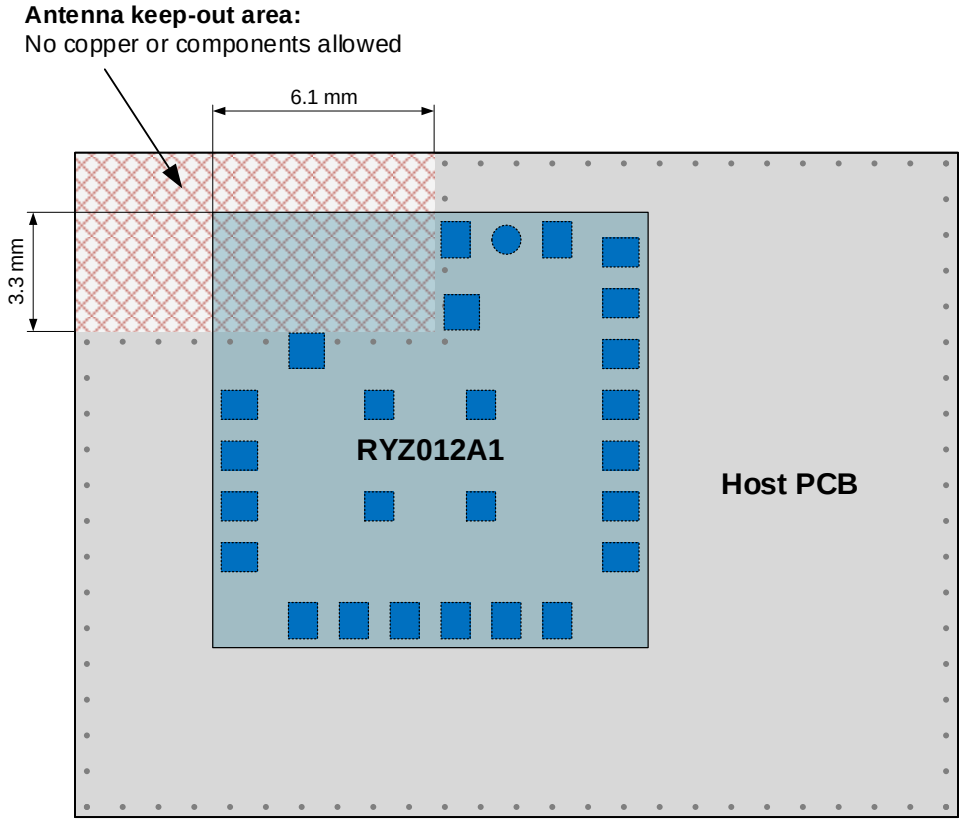
The module must not be operated at power levels above 4.8dBm. Host devices that need higher output power may not be marketed without prior re-certification.

21.3 Layout Guidelines

21.3.1 RYZ012A1

Place module close to the board corner. Do not place any metal in the keep-out area (no traces, planes, components, batteries, screws …). Ensure the module is properly connected to ground (e.g. ground plane)

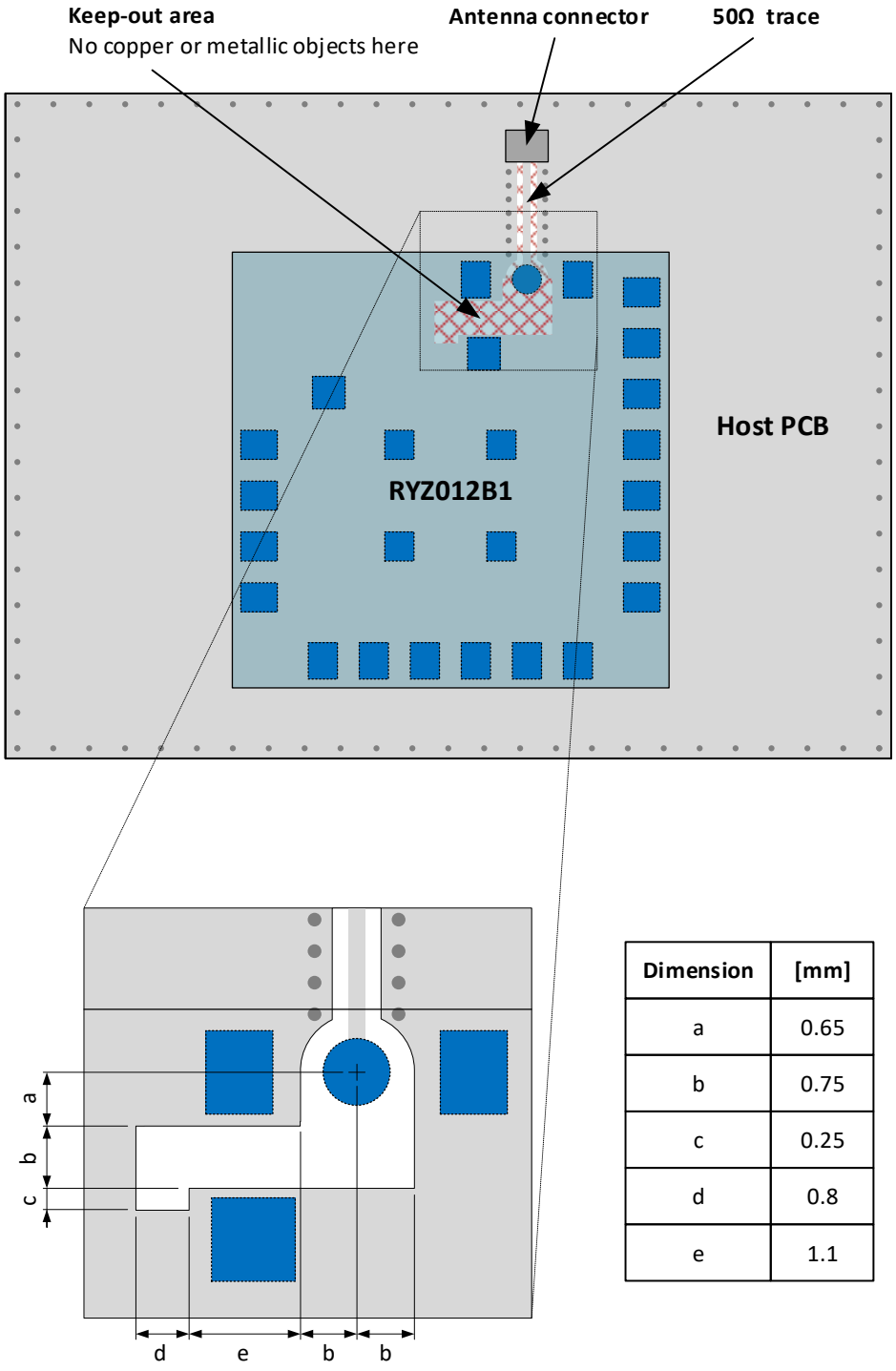
Figure 37 RYZ012A1 Layout Guidelie



21.3.2 RZY012B1

Do not place any metal in the keep-out area (no traces, planes, components, batteries, screws …).Ensure the module is properly connected to ground (e.g. ground plane). Ensure the antenna connection trace is 50Ohms matched to achieve proper antenna performance.

Figure 38 RYZ012B1 Layout Guideline

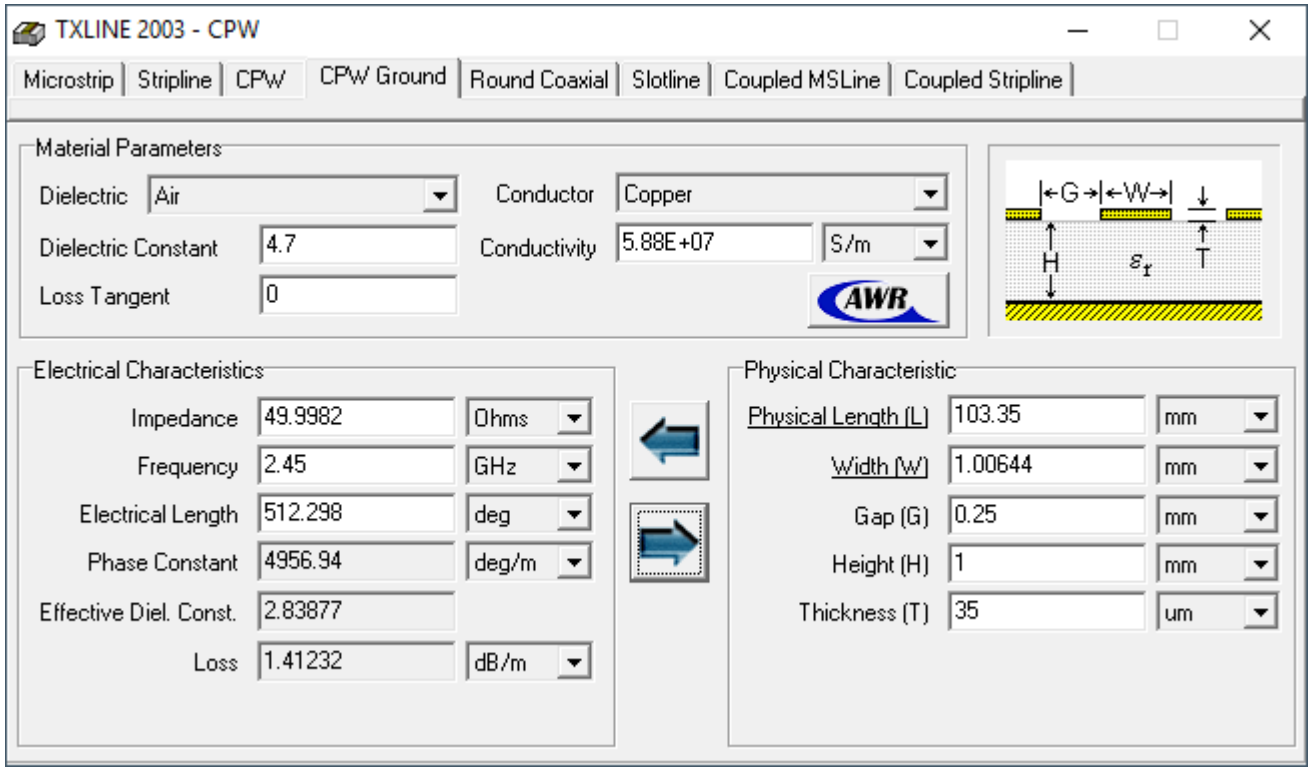


Dimension	[mm]
a	0.65
b	0.75
c	0.25
d	0.8
e	1.1

21.3.2.1 Antenna Trace Design

The antanna trace connecting the modules RF pad with the antenna connector must be designed to have 50 Ohms impedance. The impedance of the trace depends on different parameters such as the dielectric constant, trace width and height and distances to ground planes. The integrator should use a calculator such as AWR TXLine to compute the exact geometry of the antenna trace. The picture below shows an exemplary configuration for a Coplanar Wave Guide antenna trace with εr = 4.7 and 1mm substrate height.

Figure 39 AWR TXLine Tool for Antenna Trace Impedance Calculation



21.4 Antennas

21.4.1 RYZ012A1

The RYZ012A1 has an integrated antenna. The host integrator should follow the instructions from section 21 to ensure best antenna performance.

21.4.2 RYZ012B1

The RYZ012B1 doesn't have an own antenna, but comes with an antenna pad instead. The antenna must be provided by the host device. Please strictly follow the integration instructions given in section 21 to ensure proper antenna performance.

RYZ012B1 has been certified in all reagions with antenna model

PulseLarsen W1095K

Which is a monopole antenna with 1dBi gain.

21.4.2.1 FCC/ISED (North America)

FCC/ISED covered regions allow the use of other monopole antennas with less than 1dBi gain. Antennas which do not fulfill both requirements must be tested before they may be used with the module. Please contact Renesas for further information.

Important Notice: If the antenna is not fixed to the device, the antenna connector must be unique (non-standard). One type of antenna connector that fulfils this requirement is the Reverse SMA connector.

21.4.2.2 RED (Europe)

Any design should undergo radiated RF measurements, regardless of the antenna being used (including the original antenna noted in section 21.4.2). It is recommended to use a professional test house for these measurements.

21.4.2.3 MIC (Japan)

The antenna noted in section 21.4.2 may be used without any further measurements. Any other antenna requires antenna pattern measurements and listing with the MIC. Please contact Renesas for further information.

21.5 RF Exposure Considerations

This product complies with the FCC/IC RF exposure limits set for mobile applications. That means, the product may be used in applications that have more than 20cm distance from the human body.

21.6 Labeling Requirements

21.6.1 FCC (US)

Host devices integrating the RYZ012 should indicate the use of this module on a label on the host device by the following statement:

Contains FCC-ID: COR-RYZ012X1

In addition, the host device should include the following text on the label (if possible):

This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions. (1) This device may not cause harmful interference (2) This device must accept any interference received, including interference that may cause undesired operation. Caution: Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

If above statement cannot be included on the host device label, this statement must be included in the users manual of the host device.

21.6.2 ISED (Canada)

Host devices integrating the RYZ012 should indicate the use of this module on a label on the host device by the following statement:

Contains IC: 24477-RYZ012X1

In addition, the host device should include the following text on the label (if possible):

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device. Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

If above statement cannot be included on the host device label, this statement must be included in the users manual of the host device.

21.6.3 Japan

Host devices integrating the RYZ012 should indicate the use of this module on a label on the host device by the following statement:

当該機器には電波法に基づく、技術基準適合証明等を受けた特定無線設備を装着している

(Translation: “This equipment contains specified radio equipment that has been certified to the Technical Regulation Conformity Certification under the Radio Law.”)

21.7 Information on test modes and additional testing requirements

The module can provide RF signals required for additional regulatory testing through a dedicated firmware. This firmware may be obtained from Renesas upon request.

21.8 Additional testing, Part 15 Subpart B disclaimer

Not applicable.

22. Regulatory Information

22.1 FCC Statement

This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in an industrial or residential installation. This equipment generates and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Caution: Any changes or modification not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This transmitter must be co-located or operating in conjunction with any other antenna and transmitter.

22.2 EU Declaration of Conformity

Integrated Device Technology, a Renesas Corporation company declares that the RYZ012 complies with the essential requirements and other relevant provisions of Directive 2014/53/EU. A copy of the Declaration of Conformity is available on request.

22.3 Japanese Radio Law and Japanese Telecommunications Business Law Compliance

This device is granted pursuant to the Japanese Radio Law (電波法).

This device should not be modified (otherwise the granted designation number will become invalid)

23. Package Outline Drawings

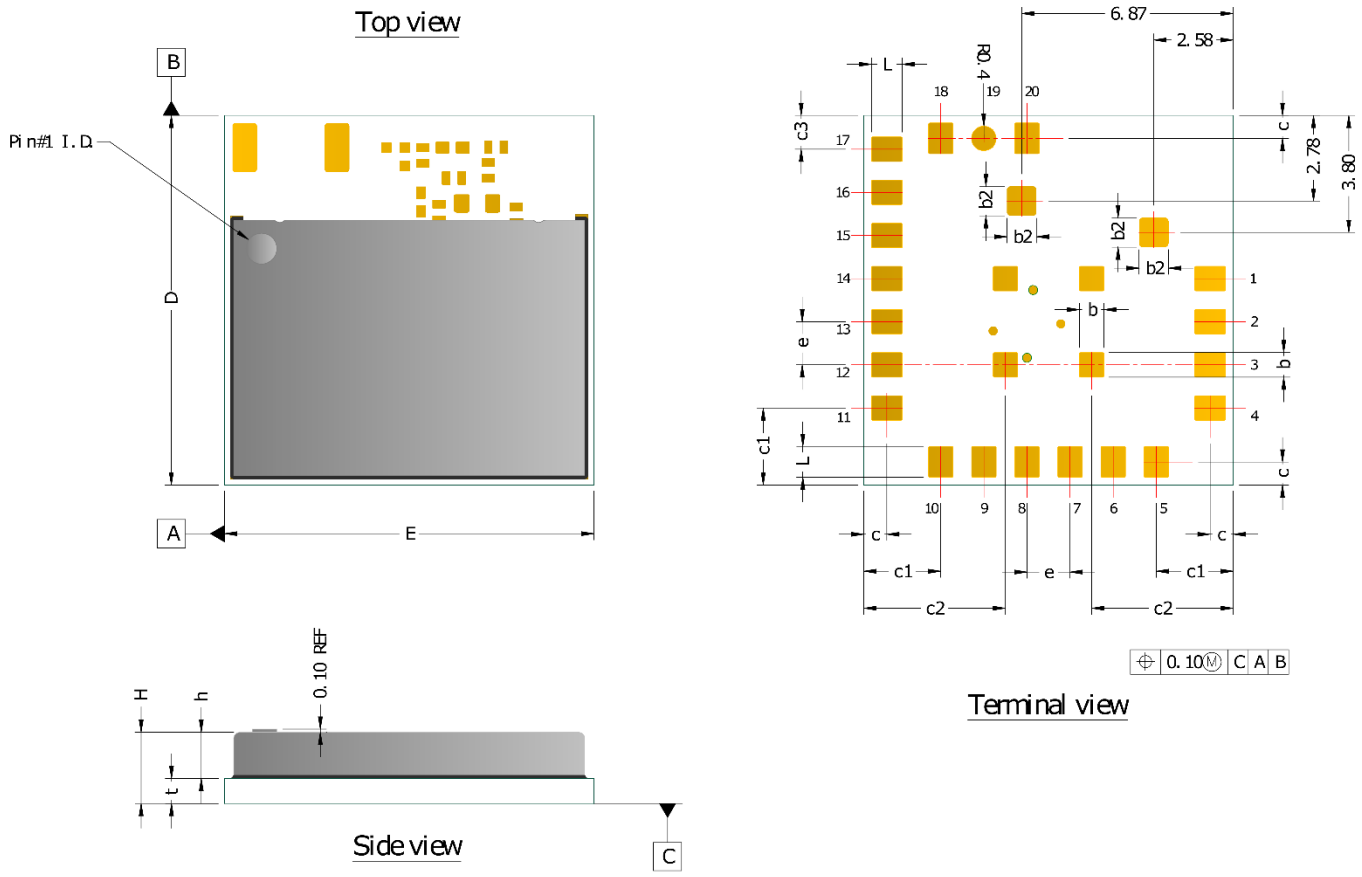


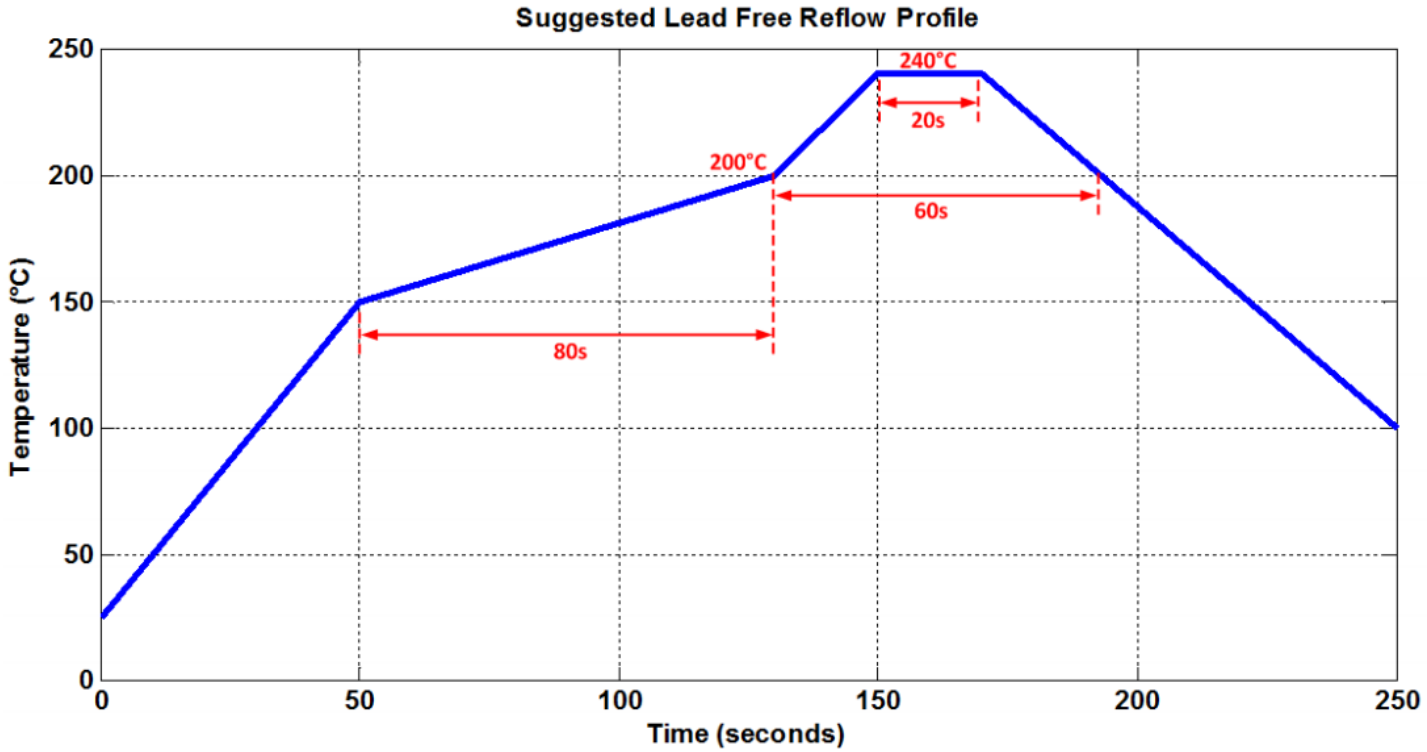
Table 33. Module Dimensions

In mm	Min.	Nom.	Max
D	11.85	12.00	12.15
E	11.85	12.00	12.15
b	0.7	0.8	0.9
b2	0.96		
L	0.9	1.00	1.1
e	1.4		
c	0.75		
c1	2.5		
c2	4.6		
c3	1.1		
H	2.16	2.31	2.46
t	0.71	0.81	0.91

24. Soldering Information

The recommended soldering profile for a lead-free (RoHS-compliant) process is shown below.

Figure 40. Recommended Soldering Profile



It is important to ensure this temperature profile is measured at the sensor itself. Measuring the profile at a larger component with a higher thermal mass results in the temperature at the small sensor measuring higher than expected. For manual soldering, the contact time must be limited to 5 seconds with a maximum iron temperature of 350°C. It is strongly recommended that a no-clean solder paste is used to avoid the need to wash the PCB.

25. Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Ambient Temperature
RYZ012A100FZ00#HD0	Bluetooth Low Energy Module with internal antenna	3	Tape&Reel	-40°C to +85°C
RYZ012B100FZ00#HD0	Bluetooth Low Energy Module needing external antenna	3	Tape&Reel	-40°C to +85°C
RYZ012A100FZ00#BD0	Module with internal antenna	3	Tray	-40°C to +85°C

26. Marking Diagram

27. Revision History

Revision Date	Description of Change
Oct.09.2020	Initial release.
Jan.13.2021	Fixed several typos
Feb.19.2021	Fixed typos and usage of Bluetooth and Bluetoot Low Energy terms
Apr.9.2021	Specified Tape&Reel for Shipping Packaging. Removed reference to FCC Statement and EU Compliance.
Apr.21.2021	Added Tray for Shipping Packaging.
Jun.8 2012	Updated