Applications

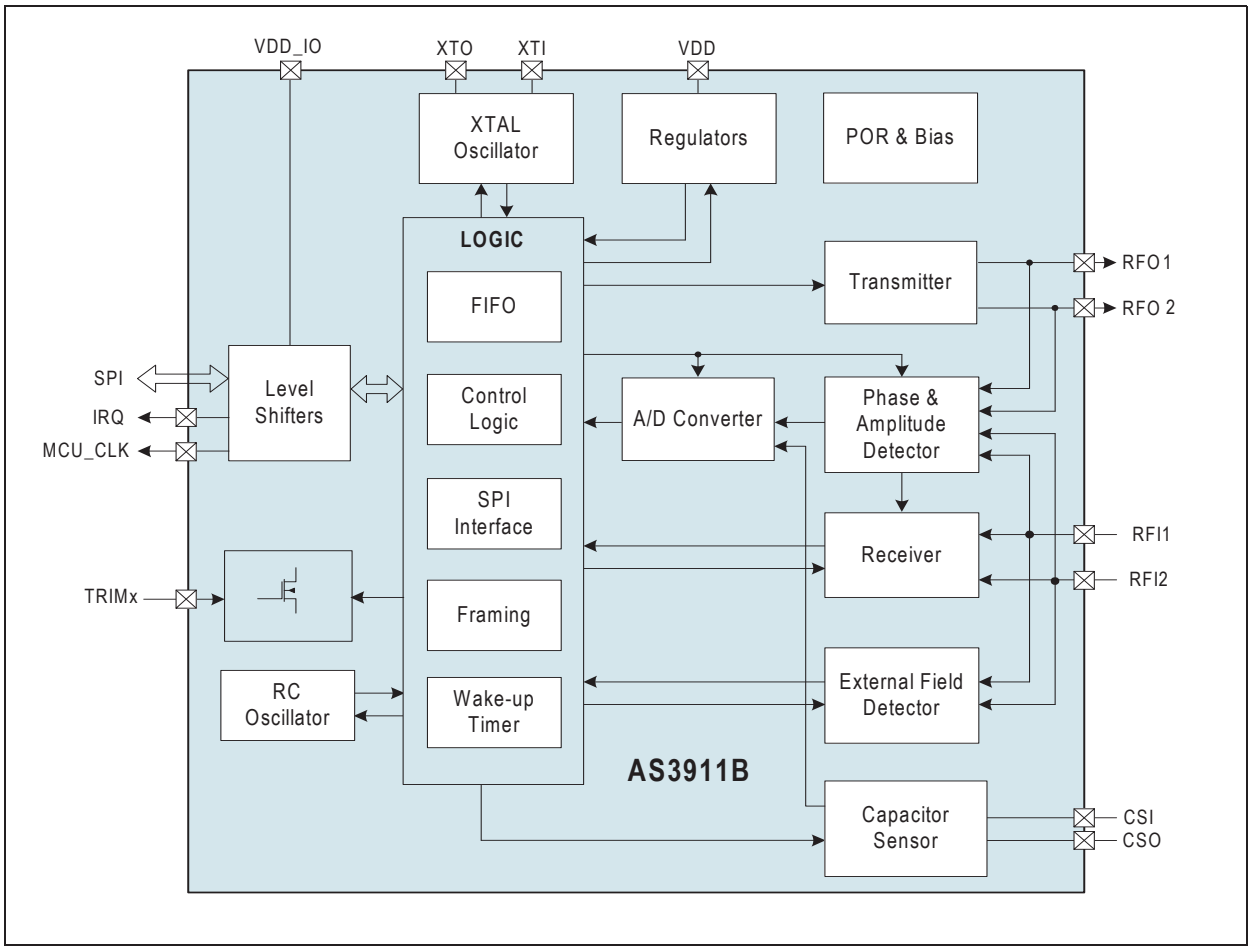
The AS3911B is suitable for a wide range of applications including:

- EMV Payment
- Access Control
- NFC Infrastructure
- Ticketing

Block Diagram

The functional blocks of this device for reference are shown below:

Figure 2:
AS3911B Block Diagram



Detailed Description

Figure 13:
Minimum Configuration with Single Sided Antenna Driving Including EMC Filter

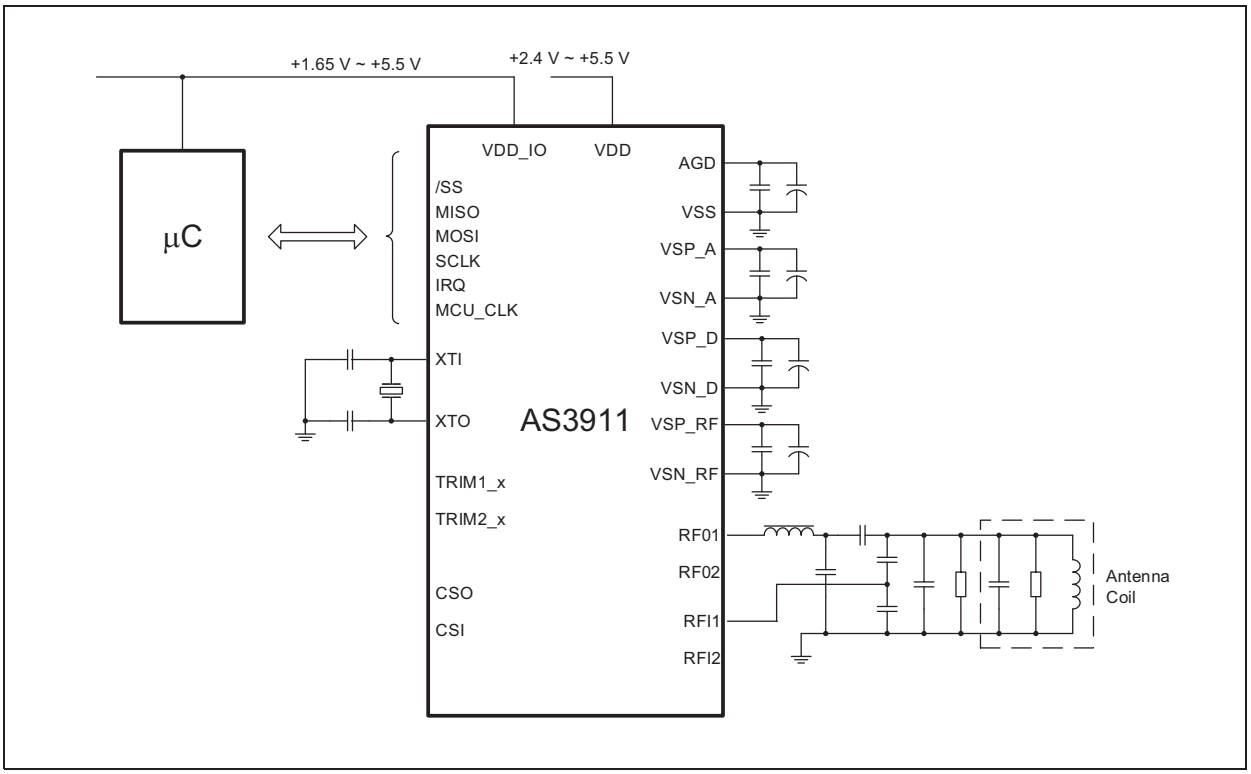
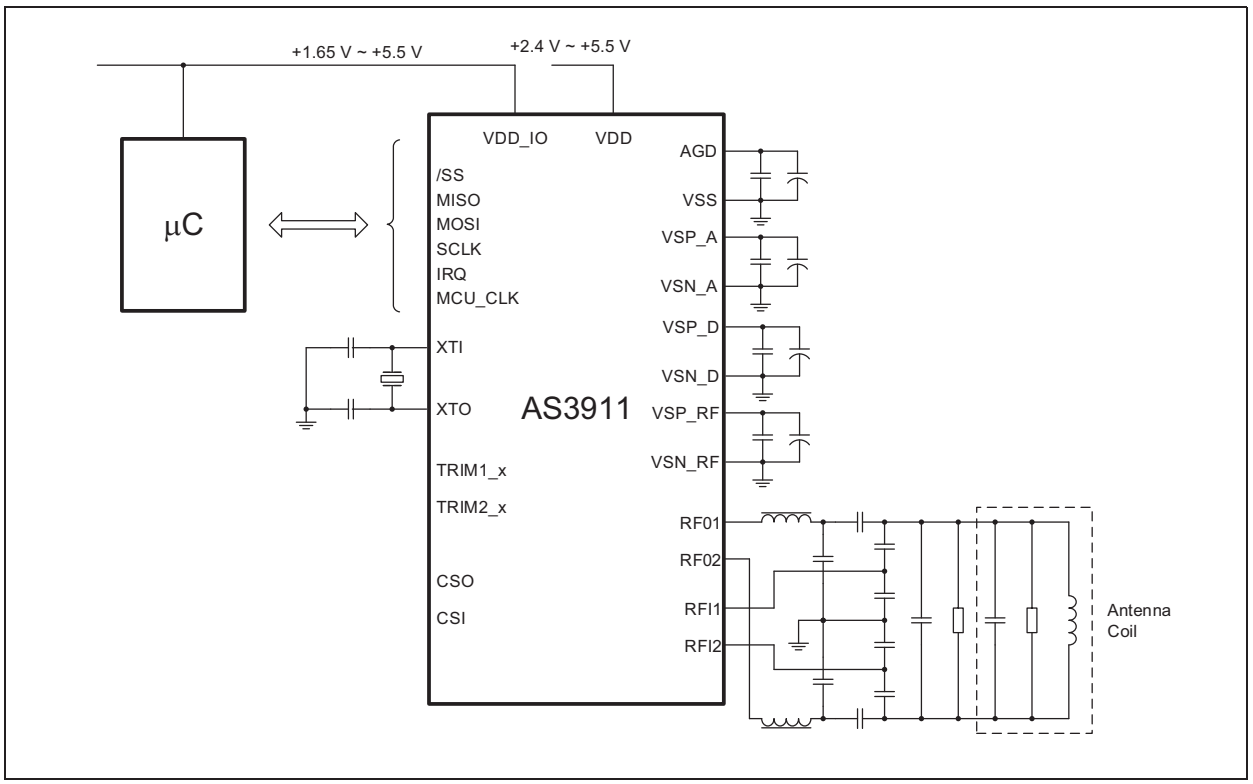


Figure 14:
Minimum Configuration with Differential Antenna Driving Including EMC Filter



Transmitter

The transmitter incorporates drivers which drive external antenna through pins RFO1 and RFO2. Single sided and differential driving is possible. The transmitter block additionally contains a sub-block which modulates transmitted signal (OOK or configurable AM modulation).

The AS3911B transmitter is intended to directly drive antennas (without 50 Ω cable, usually antenna is on the same PCB). Operation with 50 Ω cable is also possible, but in that case some of the advanced features are not possible.

By applying FFh to the register 27h, the output driver are in tristate.

Receiver

The receiver detects transponder modulation superimposed on the 13.56MHz carrier signal. The receiver contains two receive chains (one for AM and another for PM demodulation) which are composed of a peak detector followed by two gain and filtering stages and a final digitizer stage. The filter characteristics are adjusted to optimize performance over different ISO modes and bit rates (sub-carrier frequencies from 212 kHz to 6.8 MHz are supported). The receiver chain inputs are RFI1 and RFI2 pins; output of digitizer stage is demodulated sub-carrier signal. The receiver chain incorporates several features which enable reliable operation in challenging phase and noise conditions.

Phase and Amplitude Detector

The phase detector is observing the phase difference between the transmitter output signals (RFO1 and RFO2) and the input signals RFI1 and RFI2. Signals RFI1 and RFI2 are proportional to the signal on the antenna LC tank. RFI1 and RFI2 signals are also used to run the self-mixer which generates output proportional to their amplitude. The phase detector and self-mixer blocks are used for several purposes:

- PM demodulation by observing RFI1 and RFI2 phase variation (LF signal is fed to the Receiver)
- Average phase difference between RFOx pins and RFIx pins is used to check antenna tuning
- Output of mixer is used to measure amplitude of signal present on pins RFI1 and RFI2

A/D Converter

The AS3911B contains a built in A/D Converter. Its input can be multiplexed from different sources and is used in several applications (measurement of RF amplitude and phase, calibration of modulation depth…). The result of A/D conversion is stored in a register which can be read through the SPI interface.

Capacitive Sensor

The Capacitive sensor is used to implement low power detection of transponder presence. Capacitive sensor performs measurement of capacitance between its two electrodes. Presence of an object (card, hand) changes the capacitance. During calibration the reference capacitance, which represents parasitic capacitance of environment is stored. In normal operation capacitance is periodically measured and compared to stored reference value. When the measured capacitance is larger than stored reference value (threshold value can be defined in a register) an interrupt is sent to external controller.

External Field Detector

The External Field Detector is a low power block which is used in NFC mode to detect presence of external RF field. It supports two different detection thresholds, Peer Detection Threshold and Collision Avoidance Threshold. Peer Detection Threshold is used in the NFCIP-1 target mode to detect presence of initiator field. It is also used in active communication initiator mode to detect activation of target field. Collision Avoidance Threshold is used to detect a presence of RF field during NFCIP-1 RF Collision Avoidance procedure.

Quartz Crystal Oscillator

The quartz crystal oscillator can operate with 13.56 MHz and 27.12 MHz crystals. At start-up the transconductance of the oscillator is increased to achieve fast start-up. Since the start-up time varies depending on crystal type, temperature and other parameters, the oscillator amplitude is observed and an interrupt is sent when stable operation is reached to inform the controller that the clock signal is stable and reader field can be switched on. The use of 27.12 MHz crystal is mandatory in case VHBR framing is used.

It also provides a clock signal to the external microcontroller (MCU_CLK) according to setting in the control register.

Power Supply Regulators

Integrated power supply regulators ensure high power supply rejection of a complete reader system. In case PSRR of the reader system has to be improved, the command Adjust Regulators is sent. As result of this command, the power supply level of V_{DD} is measured in maximum load conditions and the regulated voltage reference is set 250 mV below this measured level to assure a stable regulated supply. The resulting regulated voltage is stored in a register. It is also possible to define regulated voltage by writing a configuration register. In order to decouple any noise sources from different parts of IC there are three regulators integrated with separated external blocking capacitors (regulated voltage of all is the same in 3.3 V supply mode). One regulator is for the analog blocks, one for

digital blocks, there is also a separate one for the antenna drivers. In case of low cost applications some (or all) regulators may not be used to save on external components.

This block additionally generates a reference voltage for the analog processing (AGD - analog ground). This voltage also has an associated external buffer capacitor.

POR and Bias

This block contains the bias current and voltage generator which provides bias currents and reference voltages to all other blocks. It also incorporates a Power on Reset (POR) circuit which provides a reset at power-up and at low supply levels.

RC Oscillator and Wake-up Timer

The AS3911B includes several possibilities of low power detection of a card presence (capacitive sensor, phase measurement, amplitude measurement). RC oscillator and register configurable Wake-up timer are used to schedule periodic detection. When presence of a card is detected an interrupt is sent to controller.

ISO14443 and NFCIP-1 Framing

This block performs framing for receive and transmit according to the selected ISO mode and bit rate settings.

In reception it takes demodulated sub-carrier signal from Receiver. It recognizes the SOF, EOF and data bits, performs parity and CRC check, organizes the received data in bytes and places them in the FIFO.

During transmit, it operates inversely, it takes bytes from FIFO, generates parity and CRC bits, adds SOF and EOF and performs final encoding before passing modulation signal to transmitter.

In Transparent mode, the framing and FIFO are bypassed, the digitized sub-carrier signal, which is Receiver output, is directly sent to MISO pin, signal applied to MOSI pin is directly used to modulate the transmitter.

FIFO

The AS3911B contains a 96 byte FIFO. Depending on the mode, it contains either data which has been received or data which is to be transmitted.

Control Logic

The control logic contains I/O registers which define operation of device.

SPI Interface

A 4-wire Serial Peripheral Interface (SPI) is used for communication between external microcontroller and the AS3911B.