WLM-01 Based WLAN Module Theory of Operation

The WLM-01 WLAN module implements an 802.11 g WLAN (Wireless Local Area Network) transceiver. System on Chip is at the center of the module. Frequency reference for the radio functions is provided by a 26MHz Crystal. Power is regulated by an on-board 3.3V LDO.
SoC consists of WLAN transceiver and an integrated ARM processor.
The transceiver section consists of a receiver, transmitter, switcher, balun and clock generating sections.
The 2.4GHz direct conversion receiver down-converts the RF signal to quadrature baseband and then into a digital domain with two high-resolution, high-speed ADCs. To adapt to varying signal conditions, RF filters, AGC and DC offset cancelation circuits and baseband filters are integrated as well.
The 2.4GHz transmitter up-converts the quadrature baseband signals to 2.4GHz and drives the antenna circuitry with a high-powered CMOS PA. The use of digital calibration improves the linearity of the PA. I/Q phase matching is achieved through additional calibration circuitry.
The clock generator produces quadrature 2.4GHz clock for the Rx and Tx. It has a built-in calibration and self-test circuits. Quadrature clock phases and phase noise are optimized with calibration algorithms.

SDIO and UART are data interface ports available on the module pins. Apart from the standard command lines, there is also a BT coexistence port as well as JTAG.

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