VZ22Q LTE module
PCB layout guide

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History

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1. Introduction

This document introduces USI VZ22Q LTE Module and provides some advices and layout rules. Please comply with all rules as careful as possible, and module performance will be better and user’s cost will be reduced.

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2. PCB Design

2.1 PCB Design Guide

i. Keep away high interference signal as far as possible. （Ex: clock, high frequency signal, switch, ...etc.）

ii. **RF** and analog signals should be protected. If there is enough space, please divide ground plane into analog and digital part. **NO SIGNALS WHATEVER** is permitted to cross this gap.

iii. Ensure power integrity and current capability, and using “**Power plane**” will be a good solution.

iv. Ground integrity under module will reduce interference.

v. Traces under the pads or LGA module are prohibited. Please use radiative layout as follows.

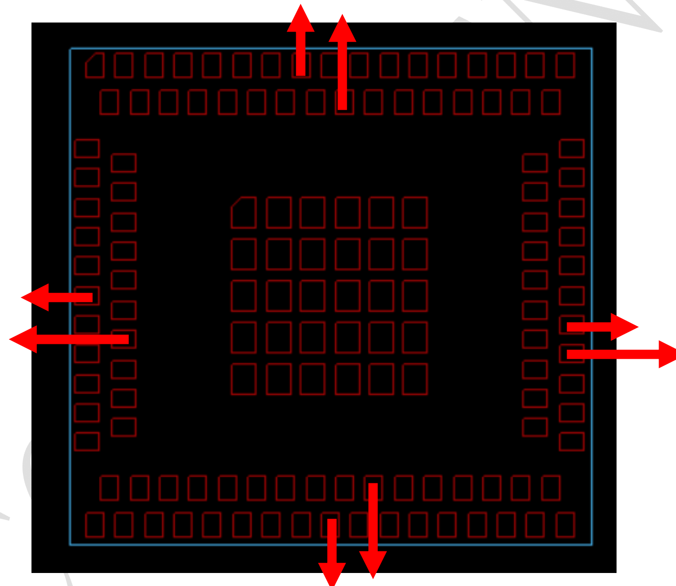

Figure 2-1: Radiative Layout

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2.2 Design for PCB Stack-up(recommend)

Using 4 layer stack-up design for PCB could reduce cost, and please refer to Table 2-1.

4 layer stack up for 0.8 mm+/- 0.08mm board thickness								
layer		Thickness(mil)	Thickness(mm)	ref. Layer(s)	impedance control (ohm)	Impedance trace width/space (mil)	spacing to GND	Impedance
	Solder mask	0.8	0.020					
L1(Top)	copper foil 0.5 oz+ plated	1.20	0.030	L2	50ohm+/-10%	4	12	50.38
				L3	50ohm+/-10%	15	4	49.65
				L2	90ohm+/-10%	4.8/10.7		88.53
	Prepreg 1080 66%	2.70	0.069					
L2(Inner)	copper foil 0.5 oz +plated	1.00	0.025	L1&L3	50ohm+/-10%	3.8	12.1	48.16
					90ohm+/-10%	4/10.5		90.15
	CORE 20mil	20.0	0.508					
L3(GND)	copper foil 0.5 oz +plated	1.00	0.025					
	Prepreg 1080 66%	2.70	0.069					
L4(BOT)	copper foil 0.5 oz+ plated	1.2	0.030	L3	50ohm+/-10%	4	12	50.38
				L3	90ohm+/-10%	4.8/10.7		88.53
				L2	90ohm+/-10%	12/4		89.18
	Solder mask	0.8	0.020					
	total	31.4	0.798					

Table 2-1. Example for Stack-up

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2.3 Recommended Package Dimension

The pad size of PCB recommended is SMD(Solder mask define).

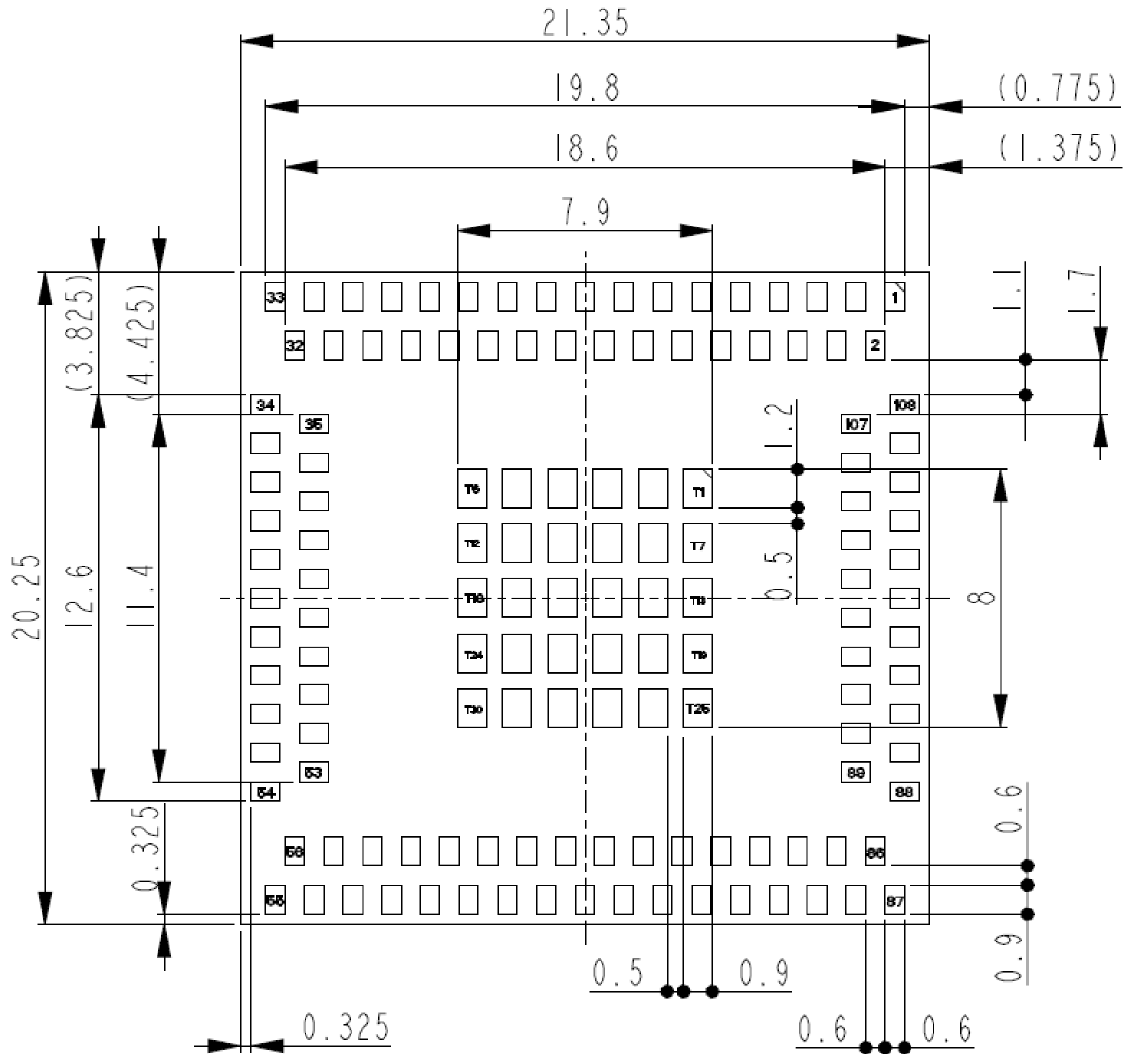

Figure 2-2: Recommended PCB footprint

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2.4 Pin define

Pin NO.	Pin name	Function	Internal PU/PD	Type	Power domain
1	GND	GND			
2	NETWORK_LED	NETWORK indicator LED	PU	O	1.8V
3	1V8	IO reference power		O	1.8V
4	USB_EXT_VBUS_VLD	USB cable detection		I	1.8V
5	FFF_FFH	FFF/FFH mode select , High =FFF ,Low=FFH		I	1.8V
6	ACTIVITY_LED	ACTIVITY indicator LED		O	1.8V
7	MODULE_ON_IND	Module on indicator		O	1.8V
8	HWID1	USB/HSIC/UART interface select pin1		I	1.8V
9	HSIC_DATA	Bidirectional data, frequency 480MHz.		I/O	1V1
10	HWID2	USB/HSIC/UART interface select pin2		I	1.8V
11	HSIC_STROBE	Bidirectional strobe signal, frenquency 480MHz		I/O	1V1
12	SIM_RST	Reset output pin for the SIM card.		O	1V8/3V3
13	USB_D+	Universal Serial BUS USB D+		I/O	3V3
14	SIM_CLK	Clock output pin for the SIM card.		O	1V8/3V3
15	USB_D-	Universal Serial BUS USB D-		I/O	3V3
16	SIM_DETECT	SIM_DETECT=1 signals that a card is present. SIM_DETECT=0 signals that no card is present.		I	1V8
17	SIM_IO	SIM card bidirectional data input/output. The SIM card output must be on an open-drain driver		I/O	1V8/3V3
18	SIM_VCC	SIM card supply voltage from internal LDO. The voltage at this pin can be selected for either 1.8 V or 3.0V.		O	1V8/3V3
19	SDIO_HOST_D2	SDIO DATA 2		I/O	1V8
20	GND	GND			
21	SDIO_HOST_CLK	SDIO CLK in/output		O	1V8
22	GND	GND			
23	SDIO_HOST_CMD	SDIO Command		I/O	1V8
24	GND	GND			
25	SDIO_HOST_D1	SDIO DATA 1		I/O	1V8
26	GND	GND			
27	SDIO_HOST_D0	SDIO DATA 0		I/O	1V8
28	GND	GND			

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Pin NO.	Pin name	Function	Internal PU/PD	Type	Power domain
29	SDIO_HOST_D3	SDIO DATA 3		I/O	1V8
30	GND	GND			
31	GND	GND			
32	GND	GND			
33	GND	GND			
34	GND	GND			
35	PCM_RXD	PCM receive data.		I	1.8V
36	PCM_CLK	PCM clock input, from 128kHz to 8192kHz		O	1.8V
37	PCM_FS	PCM frame synchroniztion at 8kHz		O	1.8V
38	PCM_TXD	PCM transmit data.		O	1.8V
39	Reserve	Reserve test pad for debug			
40	Reserve	Reserve test pad for debug			
41	Reserve	Reserve test pad for debug			
42	GND	GND			
43	GND	GND			
44	ANT1	Antenna 1		I/O	
45	GND	GND			
46	GND	GND			
47	/RESET	Module Rest pin		I	1.8V
48	JTAG_TD0	JTAG Test data output		O	1.8V
49	JTAG_TRST	JTAG Test Reset		I	1.8V
50	JTAG_TMS	JTAG Test Mode Select		I	1.8V
51	JTAG_TDI	JTAG Test data input		I	1.8V
52	JTAG_TCK	JTAG Test Clock		I	1.8V
53	GND	GND			
54	ANT0	Antenna 0		I/O	
55	GND	GND			
56	UART0_SOUT	Low speed UART, serial output data, debug only		O	1V8
57	AUX_ADC	Auxiliary A to D converter		I	1V8
58	UART0_SIN	Low speed UART, serial input data, debug only		I	1V8
59	SPI_SDI	Data to SPI device		I	1V8
60	SPI_CS_N_1	Active low chip selects to SPI devices.SPI_CS_N[1] is a primary output, muxed with GPIO[47]		O	1V8
61	SPI_CLK	Clock to SPI device. Configurable, up to 61.44MHz		O	1V8

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Pin NO.	Pin name	Function	Internal PU/PD	Type	Power domain
62	GND	GND		O	1V8
63	GND	GND		I	1V8
64	GND	GND			
65	GND	GND			
66	GND	GND			
67	SPI_SDO	Data from SPI device to SQN3221		O	1V8
68	GND	GND			
69	GND	GND			
70	GND	GND			
71	GND	GND			
72	GND	GND			
73	GND	GND			
74	GND	GND			
75	UART2_CTS	UART2 flow control, Clear-To-Send, active low		I	1V8
76	UART2_RTS	UART2 flow control, Ready-To-Send, active low		O	1V8
77	UART2_SIN	UART2 serial input data		I	1V8
78	UART3_SIN	UART3 serial input date		I	1V8
79	UART2_SOUT	UART2 serial output data		O	1V8
80	UART3_SOUT	UART3 serial output data		O	1V8
81	UART3_RTS	UART3 flow control, Ready-To-Send, active low		O	1V8
82	SQN3221_GPIO_38	General Purpose I/O,For customize.			1V8
83	UART3_CTS	UART3 flow control, Clear-To-Send, active low		I	1V8
84	SQN3221_GPIO_41	General Purpose I/O,For customize.			1V8
85	SQN3221_GPIO_39	General Purpose I/O,For customize.			1V8
86	GND	GND			
87	GND	GND			
88	SQN3221_GPIO_24	General Purpose I/O,For customize.			1V8
89	SQN3221_GPIO_25	General Purpose I/O,For customize.			1V8
90	SQN3221_GPIO_40	General Purpose I/O,For customize.			1V8
91	SQN3221_GPIO_26	General Purpose I/O,For customize.			1V8
92	SQN3221_GPIO_20	General Purpose I/O,For customize.			1V8
93	SQN3221_GPIO_23	General Purpose I/O,For customize.			1V8
94	SQN3221_GPIO_22	General Purpose I/O,For customize.			1V8

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Pin NO.	Pin name	Function	Internal PU/PD	Type	Power domain
95	SQN3221_GPIO_21	General Purpose I/O,For customize.			1V8
96	WAKE_1	WAKE_1		I	1V8
97	VCC1_PA	VCC1 PA POWER INPUT		I	Min : 3.3V, Mean : 3.8V, Max : 4.4V
98	VCC2_PA	VCC2 PA POWER INPUT		I	Min : 0.5V,
99	VCC2_PA	VCC2 PA POWER INPUT		I	Max : 3.6V
100	VCC_APT	APT POWER OUTPUT		O	Min : 0.5V,
101	VCC_APT	APT POWER OUTPUT		O	Max : 3.6V
102	VBAT_2	POWER INPUT For APT DC/DC		I	Min : 3.3V,
103	VBAT_2	POWER INPUT For APT DC/DC		I	Mean : 3.8V, Max : 4.4V
104	WAKE_0	WAKE UP Pin0		O	1V8
105	SAR_DETECT	SAR DETECT		I/O	1V8
106	MODULE_PWR_EN	PMIC enable pin for 1V2 and 3V3		I	1V8
107	VBAT_1	VBAT POWER INPUT		O	Min : 3.3V,
108	VBAT_1	VBAT POWER INPUT		O	Mean : 3.8V, Max : 4.4V
T1	GND	GND	X		
T2	GND	GND	X		
T3	GND	GND	X		
T4	GND	GND	X		
T5	GND	GND	X		
T6	GND	GND	X		
T7	GND	GND	X		
T8	GND	GND	X		
T9	GND	GND	X		
T10	GND	GND	X		
T11	GND	GND	X		
T12	GND	GND	X		
T13	GND	GND	X		
T14	GND	GND	X		
T15	GND	GND	X		
T16	GND	GND	X		

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Pin NO.	Pin name	Function	Internal PU/PD	Type	Power domain
T17	GND	GND	X		
T18	GND	GND	X		
T19	GND	GND	X		
T20	GND	GND	X		
T21	GND	GND	X		
T22	GND	GND	X		
T23	GND	GND	X		
T24	GND	GND	X		
T25	GND	GND	X		
T26	GND	GND	X		
T27	GND	GND	X		
T28	GND	GND	X		
T29	GND	GND	X		
T30	GND	GND	X		

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3. Power Design

Power integrity is a key factor for performance of **LGA** module, and it might cause some issues as follows.

i. **EMC** performance
ii. Phase and sensitivity

3.1 Power Integrity

i. Filter capacitors of power would be placed near the pads of module as close as possible. Especially, small capacitors should be the closest to pads.
ii. Power traces should be designed as wide as possible. It is better to be designed by "**plane**" type if there is enough space.

3.2 Layout Rule

3.2.1 Power Design

VZ22Q LTE LGA module cost different energy in different modes. The maximum of peak current would be 2.0A and the voltage range 3.3V~4.4V, so power trace should be wide enough to reduce impedance on them and keep adequate current capability. Recommended width should be 100 mils at the least, and design by "**Power Plane**" would be better choice.

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4. RF Layout Design

On PCB, all **RF** signal trace must be controlled its impedance of 50 ohm. Ground vias should be arranged uniformly in both side of **RF** trace. Impedance specifications normally depended on medium coefficient, trace width, and distance to ground plane. Please refer to the following to improve better performance.

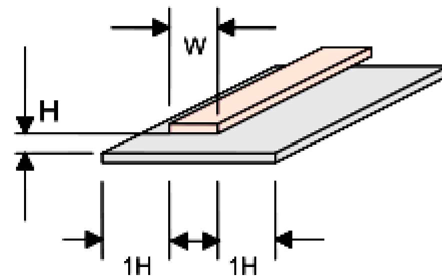

Figure 4-1. Microstrip Structure

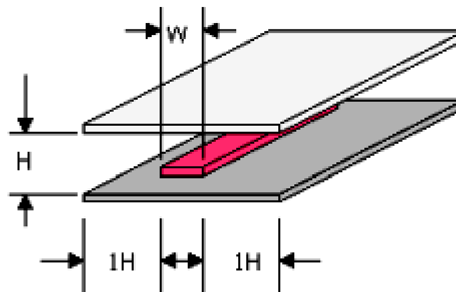

Figure 4-2. Stripline Structure

Layer of Single Trace	Impedance (Ω)	Width (mil)	Spacing to GND(mil)
L1→L2	50	4	12
L2→L1&L3	50	3.8	12.1

Table 4-1. Recommended width for 50 ohm trace

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4.1 Layout Rules

i. Antenna trace must be controlled its impedance of 50 ohm.

ii. RF trace must be as short as possible for better RF performance. (USI main antenna trace is about 1249mil, diversity antenna trace length is about 941mil)

iii. Keep away from other signals and power switch area.

iv. Surrounded by **GND** via and **GND** plane.

v. The antenna connect PN is Murata MM4829-2702

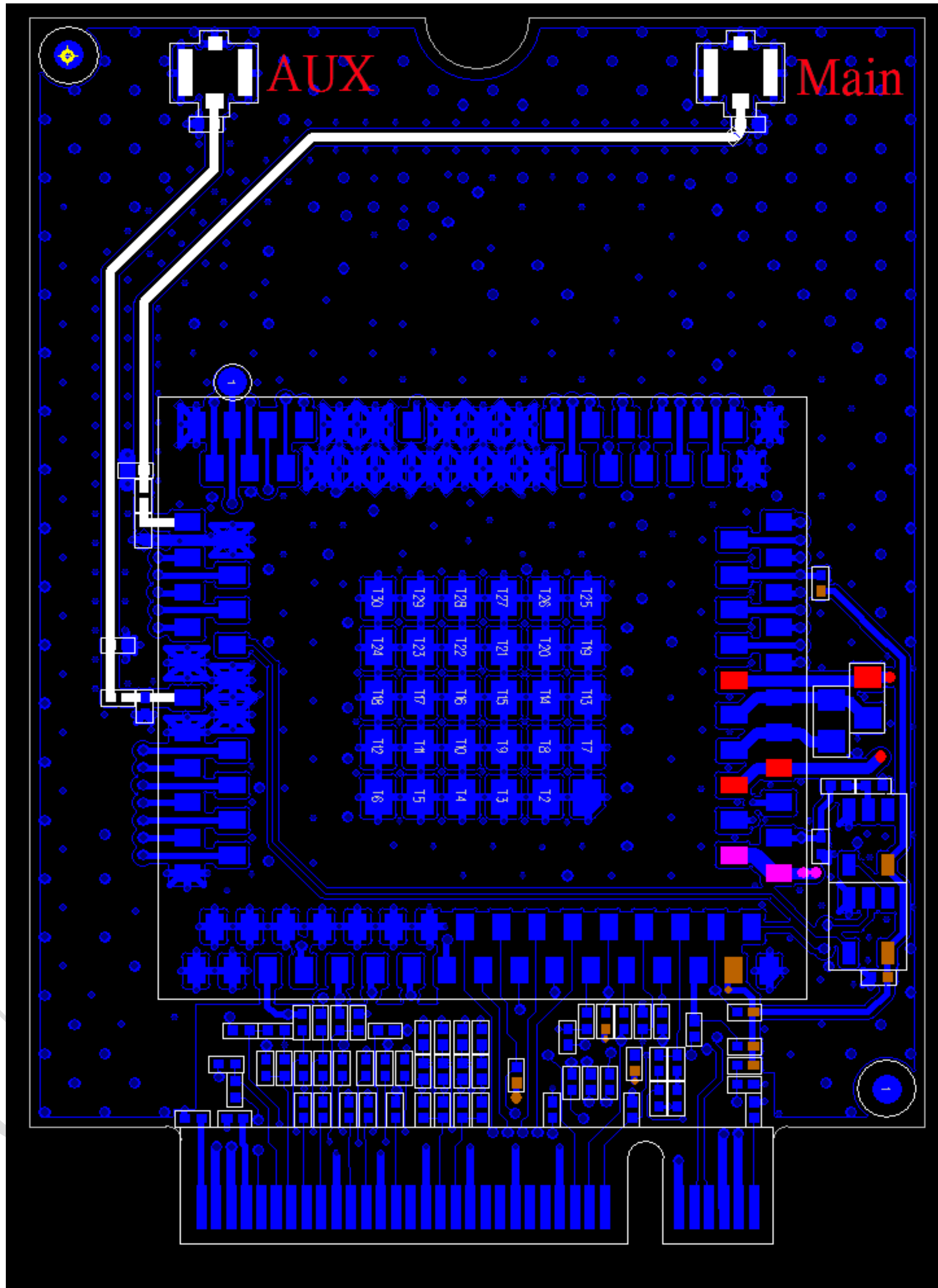

Figure 4-3. Example for RF trace

5. Audio Codec Layout Guide (TBD)

To ensure maximum performance from the **ALC5623** codec, Please refer to "Realtek realtekALC5623 Codec Layout Guide ver 0.1" for proper component placement and routing are very important. This document includes properly isolating the digital circuitry and analog circuitry. The effects of Analogue/Digital ground and Power supply plane geometry include decoupling/bypassing/filtering capacitors placement priorities, analog power supplies, and analog ground planes. Those issues would be discussed as below.

5.1 The Layout Design of Ground and Supply Plane Geometry

Figure. 5-1 shows a top view layout of ground plane for **ALC5623** codec. This layout method is to separates the analog and digital ground planes with a 60 to 100 mils gap. The moat helps to isolate noisy digital circuitry from quiet analog audio circuitry. The digital and analog ground planes are tied together at one point (FB2, Ferrite Bead). This will be the "**drawbridge**" that goes across the moat. Similarly, **NO SIGNALS WHATEVER** is permitted to cross the moat (to do so creates a "**slot antenna**" radiator which will hammer your PCB layout with crosstalk, and create huge amounts of EMI, totally defeating your purpose).

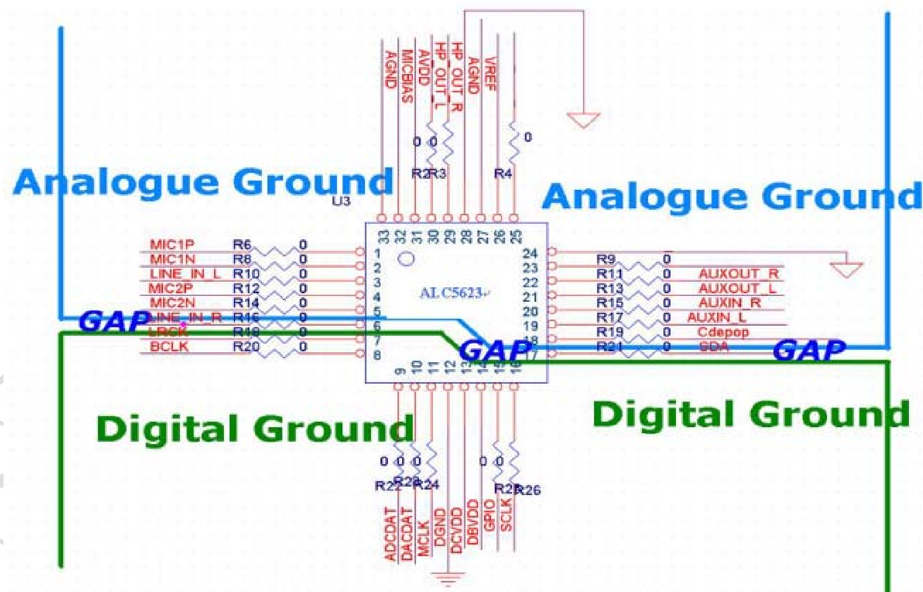

Figure. 5-1 **ALC5623** Ground plane

5.2 Component Placement

For a layout that helps to reduce noise, separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. In addition to ground planes scheme, digital and analog power supply planes should be partitioned directly over their respective ground planes. It should be place analog power coincident with analog ground planes, and digital power coincident with digital ground planes (as Figure. 5-2 – "**RIGHT**" separation). If any portions of analog and digital plane overlap, the distributed capacitance (result from power plane reference to ground plane or signal plane reference to ground plane) between the overlapping portions will couple digital noise into the analog circuitry. This defeats the purpose of isolated plane (as Figure. 5-3 – "**WRONG**" separation). The power and ground planes should be separated by approximately 40mils for the four layer PCB design. Using power and ground planes forming a natural, high capacitive, bypass capacitor to reduce overall PCB noise.

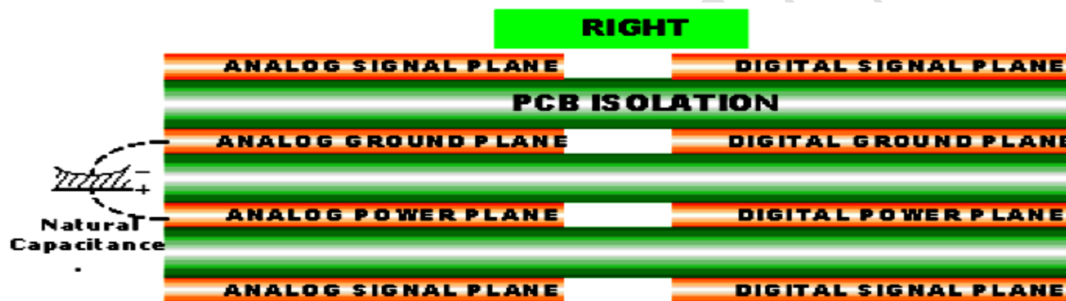

Figure. 5-2 Side view of PCB, the "**Right**" separation of analog and digital plane.

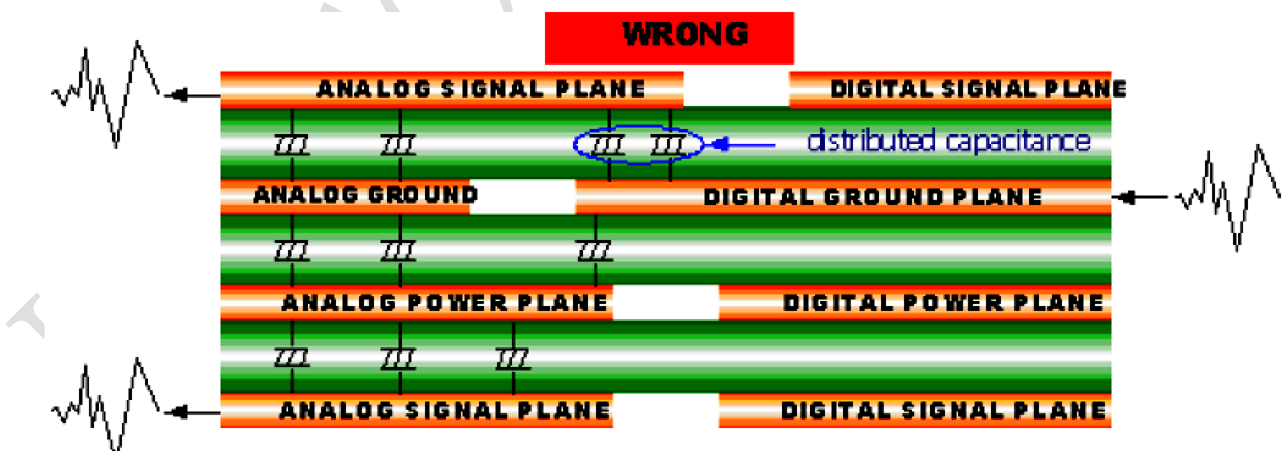

Figure. 5-3 Side view of PCB, the "**Wrong**" separation of analog and digital plane.

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5.3 Decoupling and Bypassing Capacitors

Bypass capacitors on the PCB are used to short digital noise into ground. Commonly, codec generates noise when its internal digital circuitry turns currents on and off. These current changes arise in the power and ground pins for the related section of the codec. The goal is to force AC currents to flow in the shortest possible loop from the supply pin through the bypass cap and back into the codec through the nearby ground pin. A bypassing circuit is supposed to be a low lead inductance between the codec and the bypass capacitors when in the operating frequency of the codec. The trace is longer, and the inductance is larger. To avoid long-trace inductance effects, use the shortest possible traces for bypass capacitors, with wide traces to reduce impedance. For best performance, use supply bypass leads of less than one-half inch.

In Table 5-1, it shows the priorities of series codec capacitor placemen.

i. Pins with a first – "**A**" priority components placed around the codec are the bypass caps, which are located as close as possible to the power supply pins. The capacitors must have low inductance and low equivalent series resistance (ESR). Tantalum 10μF surface mount devices are good if they are used in conjunction with 0.1μF ceramics.

ii. The filter capacitors with "**B**" priority stabilize the reference voltage for internal Ops should be placed close to codec. A good reference voltage is relative to good analog performance.

iii. These decoupling capacitors ("**C**" priority) should be close to the codec pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance. The Table 1 also point out the distribution of codec capacitor locations and placement priorities.

Signal Description	Package Pins	Priority of Close Proximity to Codec Pin Placement of Filter and Decoupling Capacitors
Digital Supply Voltage , +3.3DVDD	13,14	A
Analog Supply Voltage, +3.3AVDD	31	A
Speaker amp SPKVDD , +5V	26	A
Voltage Reference Filter (V_{REF})	27	B
Analog Signal Inputs & Output (Decouple)	1~6,19~25	C

Table 5-1. Series codec capacitor placement priorities

5.4 The Trace Routing

5.4.1 Power Input Trace

For the better loading, the power trace width is better to correspond to the suggestion as below.

i. AVDD, DCVDD, DBVDD≧15mils

5.4.2 Analog Input & Output Signal Trace

For reaching the best audio quality, some guideline should be obeyed.

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i. To avoid a cross-talk issue result from having no enough space between channels or input/output traces. The cross-talk may interfere in analog signal, especially the **MIC1P/MIC1N** and **MIC2P/MIC2N**. In Figure 5-4, the isolation between **LINE_IN_R/LINE_IN_L**, and **MIC1P/MIC1N** are routing as wider as possible (**L** at least 60 mils).

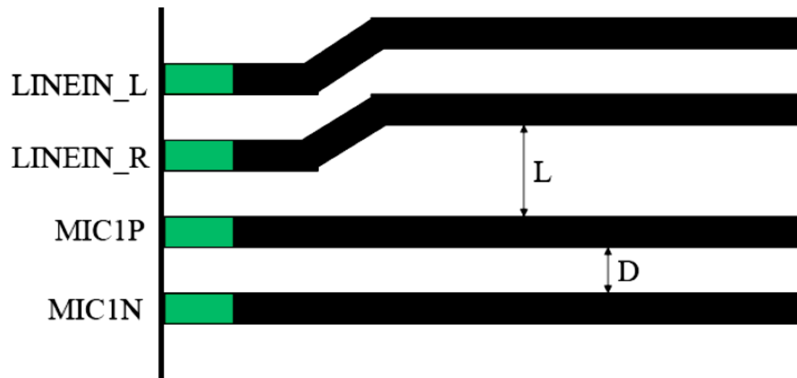

Figure 5-4. The routing for Analog Inputs (**L**>60 mils, D≦10 mils)

ii. The **MIC1P/MIC1N** and **MIC2P/MIC2N** input signals are more sensitive than the other signals. These two signals may route to the other layer if possible, and we can see that in Figure 5-5 .In Figure 5-5, **LINE_IN_R/LINE_IN_L** those input signals is routing on Layer-1. But MIC1P/MIC1N and MIC2P/MIC2N input are routing on different Layer (Ex. Layer-2) between codec and phone jack input.

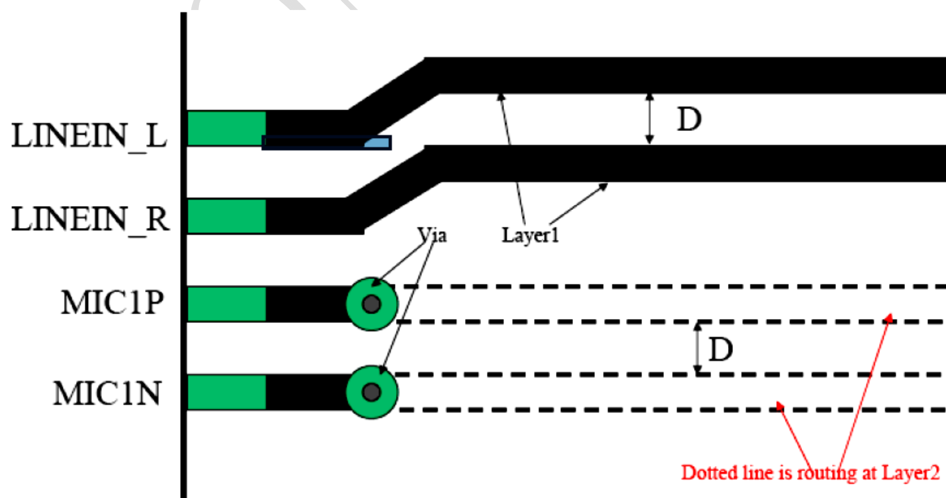

Figure 5-5. The special routing for **MIC** input signal (**D**≦10 mils)

iii. For better performance, analog input & output traces width should be as wide as possible.

- **MIC1P/MIC1N**, **MIC2P/MIC2N** >10 mils (15mils is better.)

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- **LINE_IN_L/LINE_IN_R** > 10 mils (15 mils is better)
- **AUX_OUT/AUX_OUTN** >10 mils (15mils is better)
- **SPKOUT/ SPKOUTN** > 20 mils (30 mils is better)

iv. The signal length from codec to input/output connector should be as short as possible.

v. The trace length difference between the differential signal (ex: **MIC1P/N**, **SPK_OUT_R/ SPK_OUT_RN**, ...etc) should be kept as small as possible. (better within 1 inch).

vi. The width between differential pair should be small (**D**≦10 mils).

vii. The space between each trace should better to be filled with copper which connect to analog ground.

5.4.3 QFN32 Footprint Layout

The layout of PCB footprint for **ALC5623** (QFN-32) can be seen in Figure 5-6. Note that the ground pad in the center is important. It is suggested to connect to Digital ground. It makes codec to have better performance.

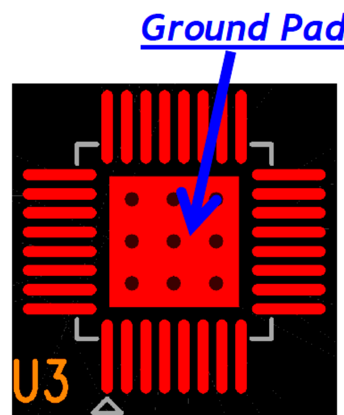

Figure 5-6. **ALC5623** PCB footprint

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6. USB Layout Design

6.1 Design & Layout Rule

i. USB pair impedance: 90 ohm differential.

ii. Avoid creating unnecessary stubs on data lines. If a stub is VZ22Q voidable (for example: ESD issue), please keep the stub as short as possible.

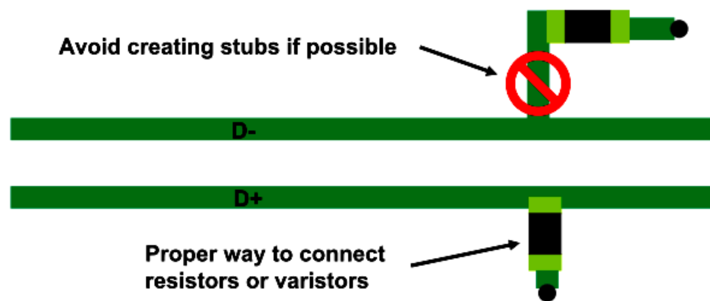

Figure 6-1. Layout management

iii. Keep away from other signals and power switch area.

iv. Surrounded by **GND** plane.

v. Recommend the length don't exceed 4 inch.

vi. The length tolerance between **USB_D**+& **USB_D-** is ± 10 mils.

6.2 Poor Routing

i. Cross split plane.

ii. Creating a stub by test point.

iii. Fail to maintain signals parallelism.

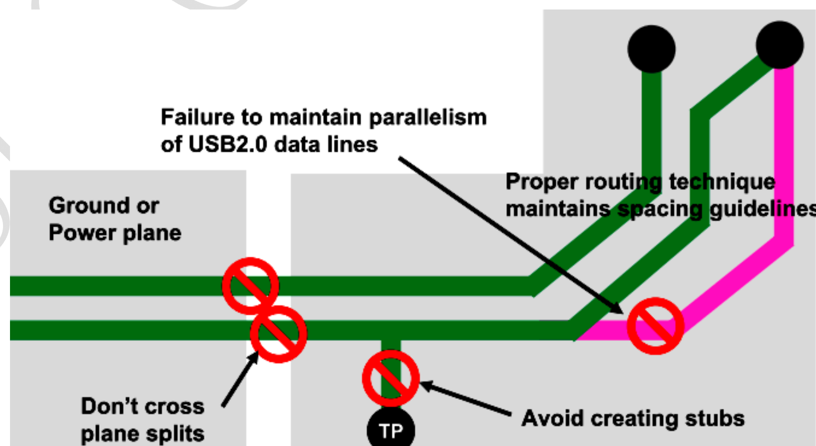

Figure 6-1. Poor Routing

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7. Layout Design of SIM Socket

i. The trace of SIM socket should be as short as possible. Recommended maximum value is 10 cm. Relative signals should be arranged together.
ii. The routing of SIM socket should follow the **BUS** routing. Notice the protection of the routing to avoid high frequency signal and interferences from clock, or it might take risk of SIM card restarting.
iii. To avoid interferences from static electricity, the **ESD** components should be close to SIM socket as much as possible.

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8. Grounding

i. The ground between module and main board should be well connected.
ii. Good ground management could enhance module performance. It would ensure signal integrity, upgrade **RF** performance, reduce **EMI**, and cool down devices.
iii. Notice structure of **RF** trace. Reference ground should be fully in side of the trace.
iv. Audio and clock signals should be wrapped by ground to isolate the interference and sensitive signals.
v. Note continuity of reference plane for each signal, and avoid crossing the spilt plane to get the shortest path of return current.

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