T32 Circuit Description/ Theory of Operation

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General.
The T32 transmitter is designed for hearing assistance and language translation functions. It is designed to operate in the 72-76 MHz band under part 15 of the FCC regulations and Industry Canada regulations. It is a portable transmitter designed to work with two AA size, alkaline or rechargeable batteries. It is sold with one of four different lapel or head worn microphones. The microphone cordage is also used as the transmitter antenna. The entire circuit board assembly is housed inside a polypropylene case.

Reference Documents:
Schematic P/N: SCH 195
User Manual P/N: MAN126A
Microphone/ Antenna drawings: MIC 054, MIC 090, MIC 086, MIC 044 2P
FCC label drawing P/N: IDL 373
T32 Block Diagram:

List of general characteristics:
User Controls, Indicators, and Connectors.
1. Power ON/OFF switch. This slide switch is located on the bezel. As indicated, it turns the transmitter battery power off and on.
2. Channel Selection switch. This is a 16 position binary rotary switch located inside the transmitter case, reached by opening up the back. It selects one of 16 RF channels for the transmitter to operate on.
3. Mute switch. This circuit reduces the audio output of the transmitter by 45 dB. It is located on the bezel.
4. Microphone jack. This is where the microphone plugs in. It is on the bezel.
5. Power/Low Battery indicator. This LED is located next to the microphone jack on the bezel. Solid "ON" indicates power on and blinking indicates a low battery condition.
6. Compression Jumper. This jumper and its associated 3 pins are located inside the transmitter case near the front bezel. The jumper positioned on the two 1:1 pins is for normal linear audio output. The jumper positioned on the 2:1 pins gives an audio output with a2: 1 compression ratio. The effect of 2:1 compression is the audio gain is raised higher at low microphone input levels than with a 1:1 ratio. At higher microphone input levels the gain is restored to the same level as the 1:1 ratio.

Circuit functions:
1. Audio circuit. This circuit accepts audio signals from the microphone jack and amplifies it to the level needed for modulation of the transmitter. Potentiometer R54 adjusts the microphone gain to accommodate several different microphone sensitivities. A 75u second pre-emphasis is added by a second amplifier. Audio limiting to prevent over modulation is done in two stages. The first stage senses the audio level and clamps it to a preset level while the second stage is a hard diode limiter or clamp circuit. The final modulation level is preset by adjusting the trimmer potentiometer R46 while the audio level is at the limiter level. This will ensure the transmitter will not over modulate.
2. Modulator circuit. This circuit combines the output of the audio circuit with the PLL loop filter output and applies them to the VCO in such a way as to provide good, clear, low distortion FM transmission.
3. VCO circuit. This circuit creates the RF output signal. It is controlled by the PLL and modulator circuits.
4. RF power amplifier circuit. This circuit provides a controlled amplification of the RF from the VCO, provides necessary harmonic filtering and matching to the RF antenna (the microphone cord).
5. PLL. The phase locked loop integrated circuit keeps the VCO on frequency.
6. Microcontroller. The microprocessor is programmed to read the channel switch and send the correct codes to the PLL chip to set it up correctly.
7. SMPS. The switched mode power supply converts the battery supply voltage to a stable, efficient 5VDC to operate the various functions of the transmitter.
8. Reverse Battery Protection Circuit. This circuit protects the transmitter when the batteries are installed backwards.
9. Linear Voltage Regulator. This circuit provides a low noise, well regulated 4.5 VDC to power various transmitter circuits. It gets its supply from the SMPS. Part of its function is to remove the high frequency ripple form the SMPS supply.

10. Low battery Monitor. Battery voltage is detected by the microcontroller which blinks the power LED when it gets below 2.0 volts.

Detailed Circuit Descriptions:
This section describes the details of how each individual circuit works, the inputs required, and the outputs it generates. Please reference SCH 195 to follow the explanation.

SMPS.
Input: 2.0VDC to 3.2VDC battery supply voltage. Current draw is up to 60 mA at 3.2VDC, 130 mA at 2.0VDC.
Output: regulated 5.0 VDC at 1.6 to 3.2 VDC input
Description:
This circuit accepts the battery current from Q10, the reverse battery protection circuit. The NCP1400 DC to DC converter is a standard boost regulator operating at 180 kHz. Pin 5 is periodically grounded through an internal switch, charging the flyback choke L4. When the switch opens, the field in L4 collapses charging C64 through the top diode in D6. D6 is a schottkey diode (BAT54s) for improved efficiency. The output voltage from C64 is connected back to pins 1 and 2. Pin 1 is the chip enable pin. If the voltage at pin 1 is less than 0.3V the chip will not start. The chip is enabled if the voltage here is greater than 0.9VDC. Pin 2 is the output voltage monitor (feedback pin) and also the power supply pin for the device. If this circuit is operating properly, there should be 5VDC on TP9 for any supply voltage form 2.0VDC to 3.2VDC.

Linear Voltage Regulator:
Input: 5.0VDC from the SMPS.
Output: 4.5VDC at TP9.
Description:
This circuit is a typical low noise, low dropout voltage regulator. It is comprised of C61, C62, C57, R61, C63, and IC5. C62 is the bypass cap and serves to reduce the output noise, critical in this application. C61 is the input capacitor, and C63 is the output capacitor. This device is protected internally against short circuits and should not be damaged by them. If this circuit is operating properly there should be solid 4.5VDC on TP9.

VCO:
Inputs: +4.5VDC from the linear Regulator. Steering voltage form the PLL loop filter circuit. Audio from the modulator circuit (2 places).
Outputs: 72-76MHz RF to the PLL chip pin17. 72-76 MHz RF to the RFPA via C24. This must be measured with a FET probe or equivalent. Standard probes have too low an impedance at RF and will corrupt the measurement..
Description:
This is a modified Colpitts circuit. The capacitive divider, C8 and C17, plus the parallel capacitances from D3 and D2, plus the load capacitances and strays resonate against L1 to form the tuning network of the oscillator. The oscillator is tuned via the voltage applied to the variable capacitance diode, D3 through R11. The VCO is modulated via D2 the audio input. Above several hundred hertz D2 is the dominant factor in modulation. Below 300 Hz D3 is the dominant factor. The oscillator is adjusted by setting the channel selection to the highest channel, (channel F 75.9 MHz). Then L1 is adjusted to present 4.0 VDC at TP6. This sets the upper end of the tuning range. The lower end of the tuning range should then be checked by setting the channel to channel 0 (72.1MHz). This voltage should now measure more than 1VDC at TP6, ensuring D3 has enough tuning voltage to maintain a high Q. R19 sets the drive level of the oscillator, which should draw about 2 mA. If this circuit is operating properly, the PLL should lock and the RF outputs should be as specified above.

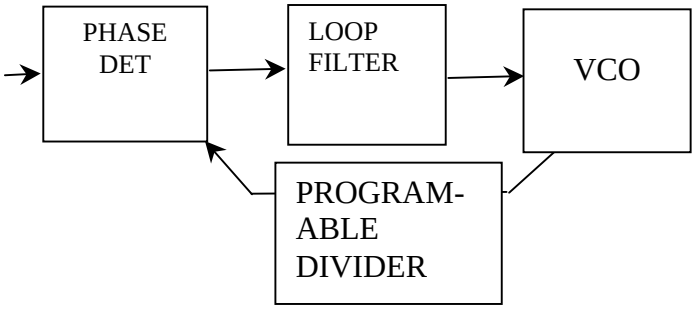
RFPA:
Inputs: +5VDC from VDD, +4.5VDC from VREG, RF input (72-76MHz) at gate 1 from the VCO.
Outputs: Approximately 6-7 mW RF output as measured in the test fixture, as shown on the HP8901B modulation analyzer.
Description:
This circuit uses a dual gate MOSFET (Q2) as a gain controlled amplifier. RF is applied at gate 1. The RF output power is adjusted by trimming the gate 2 bias pot (R18) for the desired power. Gate 1 presents a very light load to the VCO, helping maintain a high Q circuit for lowest noise. Also, the structure of the MOSFET provides a high isolation between the VCO and the antenna, reducing unwanted frequency pulling due to body-motion-induced antenna impedance changes. L2, L3, L4, L5. L6. C12, C14, C15, C21, and C10, comprise the RF match/filter network to match Q2 to the antenna, while filtering off unwanted harmonics. The circuit is designed to require no adjustment if the proper component values are inserted. If this circuit is operating

properly, the RF output should be as specified above.

Low Battery Monitor:
Inputs: +VBAT from batteries.
Output: LED D4 flashes when the battery is low. Otherwise it is "ON".
Description: The low battery detector uses the A/D converter function on the Microcontroller IC. It grounds pin 5 low when the battery reaches 2.0VDC and flashes the LED D4.
If this circuit is operating properly, D4 should flash whenever VBAT < 2V.

Microcontroller:
Inputs: +4.5VDC from VREG, 4 bit binary control nibble from S1.
Output: serial bus consisting of CLOCK, DATA, and ENABLE lines to setup and control the PLL chip.
Description:
IC1 is a FLASH based PIC16F676 microprocessor. This microprocessor interprets the channel switch (S1) setting and, through the serial bus connections, sets up the PLL chip, IC2. There is a 7.2 MHz reference oscillator used in this chip, which governs the operation of the device. The circuit is set up to permit reprogramming the part in the transmitter. If this part is working properly, the transmitter should respond correctly to channel switch setting changes. If this does not occur, further investigation may be done by observing the waveforms at pins 2 (CLK), 3 (DATA) and 11(CE) of the microprocessor. TP1-5 provides connections for in circuit programming. R2 and C2 decouple the microprocessor from the VREG line to keep digital noise out of the audio.

PLL:
Inputs: +4.5VDC from VREG, Control bus from IC1
Output: locked RF signal from VCO.
Description:
See Block Diagram below. Also reference SCH 195.
A simplified PLL is diagrammed below. Reference oscillator, Phase Detector, Loop Filter, and VCO.



The PLL in the T32 is comprised of these basic parts, with some modifications for more sophisticated operation. The reference oscillator is a 7.2000 MHz oscillator which is part of IC2, with the addition of the reference crystal X1, and its resonating capacitors C16 and C23. C23 is a 9-60 pF variable capacitor which serves to trim the reference frequency to exactly 7.2000 MHz. The phase detector and programmable divider are also built into IC2. The VCO has been described previously (see above). The loop filter is comprised of the following: R38, R27, C33, IC3A (op-amp) with C34, R33, C25, R26, R30, and C29. The loop filter is designed to roll off all noise and modulation below a few hundred hertz. If this part is working the frequency will lock and be stable on each channel selected. This is s necessary, but not sufficient condition, meaning that the circuit may lock and still not be quite right if it is noisy or produces distorted output. The connection of the modulator to the loop filter through R26 adds a level of sophistication and complexity which will be explained in the Modulator section of this document.

Modulator Section:
Inputs: +4.5VDC from VREG, +5VDC from VDD, Audio form the audio processor circuit.
Outputs: Audio to modulate D2, Integrated audio, scaled and summed with the PLL error voltage at IC3 pin 2.
Description:
This circuit has 2 outputs which, when summed together in the VCO, enable the loop filter to be set very wide (several hundred hertz) while passing audio down to less than 200 hertz to inhibit noise, microphonics, and human body movements. This is accomplished by a simple circuit. Audio is received from the audio processor

circuit at the top of the modulation pot (R46). The audio output is routed in 2 directions: One part is routed to D2 in the VCO, the audio modulation varicap. The other part is integrated by R38 and C33, buffered by IC3A, scaled by R33, and summed with the PLL error voltage at IC3 pin 2 (part of the loop filter). This second signal has the effect of canceling the error voltage resulting from the modulation, permitting the PLL to be modulated at frequencies below the loop roll off. If this part is working properly, the transmitter audio as demodulated in a receiver will be essentially flat from 200-16KHz. If the low end of the audio rolls off too soon, this circuit must be suspected.

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