Spacelabs Medical

90341-05 ULTRAVIEW® DIGITAL TELEMETRY TRANSMITTER

OPERATIONAL DESCRIPTION

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90341-05 Transmitter Operational Description

The following discussions are with reference to the circuit diagram shown in Block Diagram.pdf.

Transmitter Description

The 90341-05 Telemetry transmitter contain two main circuit boards:

- ECG Board
- RF Transmitter Board

ECG Board Description

Input Protection

- Series resistors and two clamp diodes on each input to protect the transmitter circuitry against a defibrillator discharge

Lead Drive Switches

- Control the ECG reference lead, depending upon which ECG lead wires are connected
- Selected by the automatic lead switching PAL

Input Buffers

- High input impedance op amps configured as voltage followers to buffer the ECG input signals
- Provide ECG inputs with a very high impedance

Lead Off Comparators

- Determine if lead fault has occurred
- Provide inputs to the ALS PAL to indicate lead fault

Differential Amplifiers

- Provide common mode rejection
- Eliminate ECG electrode offsets up to ± 300 mV

Pacer Blanking Switches

- Strip the detected pacer pulse

Bessel Filter

- Defines the system's 30 Hz bandwidth
- Provides a time delay to facilitate pacer blanking
- Prevents ringing due to transient inputs

Final ECG Amplifiers

- Provide most of the ECG signal gain

DC Restoration Comparators

- Become active when the ECG output is outside the dynamic range of the PWM converter
- Define the 0.05 Hz high pass pole frequency
- Eliminate the ECG electrode offsets (up to ± 300 mV)

Pacer Detection and Pacer Flag Generator

- The pacer detector triggers the pacer flag generator whenever a pacer signal is detected
- The pacer flag is transmitted to the receiver and controls the pacer blanking switches

Automatic Lead Switching PAL

- Decides which lead should be driven and closes the appropriate lead drive switch
- Provides logic to the pacer detector when selecting the ECG vector

Transmitter RF Board Description

Status Mux

Receives the following inputs:
- Lead Status indicators from the automatic lead switching PAL (ECG board)
- Transmitter ID switches
- Low battery flag from the low battery detector
- Record signal from the patient remote record switch

ECG Mux

- Multiplexes the two transmitted ECG vectors
- Controlled by the PWM PAL
- Followed by a buffer to isolate it from the PWM comparator

PWM PAL

- Controls all the timing and framing of the PWM signal
- Selects the inputs on the ECG mux and the status mux

PWM Ramp Generator

- Generates a ramp voltage for each ECG signal during each sample
- Controlled by the PWM PAL

PWM Comparator

- Compares the sampled ECG signal to the PWM ramp to generate a PWM encoded signal

PWM Data Formatter

- Combines framing information from the PWM PAL with the PWM-encoded ECG signals

PWM Filter

- Filters the modulation signal to define the modulation bandwidth of the RF signal

Voltage Controlled Crystal Oscillator

- Colpitts oscillator operating at the fifth overtone

- Frequency is pulled by modulating the voltage on two varactor diodes in series with the crystal

First and Second Frequency Doublers

- The transistor in each stage generates the second harmonic of the input frequency
- The filter following each transistor filters all frequencies except the second harmonic of the input frequency
- The two cascaded stages multiply the VCXO's frequency by a factor of four

Transmitter RF Radio Description

The following discussions are with reference to the circuit diagram shown in Schematics.pdf.

Tune-up Procedure

C10 is adjusted for maximum amplitude of the oscillator and to bring the oscillator within 250 Hz of the correct frequency. The frequency is then adjusted by R9 to within 50 Hz. C7, C6, C3 and C2 are then adjusted for maximum level at the 608 MHz to 614 MHz output. There is some interaction between C7 and C6 and between C3 and C2.

Frequency Stabilizing Circuitry

The frequency is determined by the Voltage Controlled Crystal Oscillator. The active device is Q3. L8, C10, C12 and C13 form a tunable parallel resonant circuit in the collector of Q3. X2, LI, L2, L3, D2 and D3 form a series resonant circuit feeding the emitter of Q3.

The frequency is determined primarily by crystal X2, which operates in the 5th overtone mode. X2 is specified to have an initial tolerance of +/- 5 ppm and a temperature stability of +/- 2 ppm from 10° C to 40° C. C10 tunes the parallel resonant circuit to approximately the crystal frequency. R9 adjusts the DC bias on the varactors D2 and D3 to bring the frequency within +/- 50 Hz.

Spurious Suppression

Spurious frequencies are generated by the VCXO and the frequency doublers. Suppression of these spurious frequencies are performed by the coupled resonator filters which act as tuned loads for both Ql and Q2. The filter following Q2, composed of L6, C7, C36, L7, and C6, is tuned to approximately 304 MHz and rejects all other harmonics of 152 MHz by more than 40 dB relative to the 304 MHz component. The filter following Ql, composed of L5, C3, C25, L4, C2, L10, C18, and C47 is tuned to approximately 608 MHz and rejects all other harmonics of 304 MHz by more than 35 dB relative to the 608 MHz component.

The modulation is limited by the amplitude of the digital waveform, the gain of the pre-modulation filters and the conversion gain of the VCXO. The digital waveform is fixed at 0 V to 5 V and cannot be any larger. This signal is attenuated by a variable resistor divider which is used to adjust the deviation. All circuits following this point have fixed gains.

The output power is limited by the current drain of the final amplifier stage and the level of the signal going into the final stage. The current drain of the final stage is controlled and is nonadjustable. When all signal levels are peaked, the output power will be slightly less than the rated power.

Digital Modulation

The several analog data channels are time multiplexed and then encoded with variable pulse widths. The system is constrained so the minimum pulse width is 240 us. A timing PAL, U4, is used to derive the 240 us minimum pulse width.

The digital waveform is filtered by a fourth-order Bessel filter with a cut-off frequency of 3.4 kHz before modulating the VCXO.