EXHIBIT 5

THEORY OF OPERATION

SEVEN PAGE THEORY OF OPERATION FOLLOWS THIS SHEET

1. DESCRIPTION OF CIRCUITS

1.1 OUTLINE OF BLOCKS

The NRD-545 can broadly be divided into six blocks: Receiver block, Synthesizer block, Control block, Wideband reception converter, Panel block, and Chassis block. Table 1-1 lists the units comprising each block.

Table 1-1 Table of Blocks and Units

Block	Unit	Type
Receiver block	RF TUNE UNIT	CFL-356
	1ST IF UNIT	CFH-71
	DSP UNIT	CDA-752
Synthesizer block	LOOP1 UNIT	CGA-184
	REF/DDS UNIT	CGK-160
WB converter block	WB CONVERTER	CHE-199
Panel block	DISPLAY UNIT	CDE-860
	JACK UNIT	CQB-83
Chassis block	MOTHER BOARD	CFQ-8350
	AVR UNIT	CBD-1363
	CHASSIS	NRD-545

The receiver block employs a triple superheterodyne system in which the 1st IF is 70.455MHz, the 2nd IF is 455kHz, and the 3rd IF is 20.22kHz. Variable-voltage tuning (electronic tuning using capacitance diodes) is used for the front end tuning circuit, allowing continuous tuning to the receiving frequency.
The RF amplifier and 1st mixer each use four junction-type FETs, which have low noise and excellent cross modulation characteristics, thus widening the dynamic range and improving sensitivity.
The 1st IF unit includes an RTTY demodulation circuit which demodulates the ITU-T No.2 codes at shift widths of 170, 425, and 850Hz and a baud rate of 37 to 75 baud. The demodulator output can be sent via an RS-232C line to a computer and displayed on the screen.
The DSP unit performs not only each modes demodulation but also BWC, PBS, NB, AGC, NOTCH, and BFO processing, etc.
The Synthesizer block generates the required frequency signals of 70.555MHz to 100.454999MHz and 70MHz for the receiver block, based on a highly stabilized reference frequency of 20MHz. The 70.555MHz to 100.454999MHz frequencies are generated by the PLL synthesizer, which employs a direct digital synthesizer (DDS) IC.
The wideband reception convertor block converts 30MHz to 1999.999MHz signals into 10.7MHz signal.
The panel block houses the switches and controls for operating the NRD-545.
A large color LCD displays the frequency, mode, band, and meter readings, etc.

The panel block is also provided with a CPU for switching among the receiver circuits, controlling the synthesizer frequency, processing key input, and controlling the LCD display, etc.
The chassis block is built around a motherboard that interconnects the respective units. A motherboard is used to reduce the amount of wiring harnesses and improve reliability and the ease of maintenance.

1.2 DESCRIPTION OF UNITS

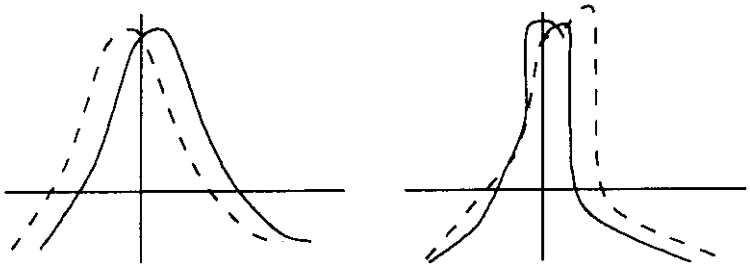
1.2.1 CFL-356 RF TUNE UNIT

The RF TUNE unit consists of a double tuning circuit, RF amplifier, and 1st mixer. The signals input via the antenna connector pass through a 20dB attenuator switching circuit with K1 to the double tuning circuit. In the double tuning circuit, the frequencies are grouped into six bands in the range from 100kHz to 30MHz (Tale 1-2). The decoder (IC1) and TR1 operate using the band switching signals from the CPU to select the desired reception band.

Table 1-2 Division of Bands in Double Tuning Circuit

Division	Frequency	Remarks
1	100kHz ~ 0.4kHz	LPF
2	0.4MHz ~ 1.6MHz	Double tuning circuit
3	1.6MHz ~ 4.4MHz	
4	4.4MHz ~ 12.3MHz	
5	12.3MHz ~ 20.5MHz	
6	20.5MHz ~ 30MHz	

The DISPLAY unit generates the variable voltage applied to the capacitor diode in the double tuning circuit. This voltage is controlled per 10kHz to optimize the tuning characteristics for the receiving frequency. In addition to extremely sharp resonance characteristics, the double tuning circuit also enjoys minimal detuning even if the antenna impedance fluctuates. That is, there is minimal effect on the resonance characteristics (Figure 1-1). The NRD-545 takes advantage of this merit so that a high level of sensitivity is obtained with a wide range of different antenna.



1. Single tuning 2. Double tuning

The solid line indicates the characteristics with the impedance matched with the antenna. The dashed line indicates the characteristics with the impedance mismatched with the antenna and the tuning circuit detuned.

Figure 1-1 Tuning Characteristics

After the double-tuning circuit, the received signals are sent to the RF amplifier. The RF amplifier in this receiver is a high-power gain type amplifier composed of four low-noise junction type FETs (TR2, 3, 4, and 5) connected in parallel. This RF amplifier provides four times (6dB) the power gain of an amplifier consisting of only one FET, and hence realizes a highly sensitive receiver. The received signals amplified by the RF amplifier are mixed by the 1st mixer (TR7, 8, 9, and 10) with the 1st local signal to create a 1st IF signal of 70.455MHz. The 1st mixer is a double balanced mixer composed of four low-noise junction-type FETs. Double balanced mixers suppress the intermodulation components of the odd-numbered orders and are therefore capable of greatly reducing the intermodulation product distortion (IMD) over a single-balanced mixer. Multiple signal characteristics are therefore improved, improving receiver performance.

1.2.2 CFH-71 1ST IF UNIT

The 1st IF unit consists of the 1st IF filter, 1st IF amplifier, 2nd mixer, and RTTY demodulator circuit.
The 70.455MHz 1st IF signal from the RF TUNE unit passes the monolithic filter (MCF) FL1 to be amplified by the 1st IF amplifier, consisting of TR1. As TR1 functions as an AGC amplifier, a dual-gate MOS-FET is used. The signal amplified by the 1st IF amplifier is mixed by the FET balance mixer (TR2 and TR3) with the 2nd local signal (70MHz) from the synthesizer block and converted into the 455kHz 2nd IF signal. The 2nd local signal (70MHz) is amplified by TR4 before being sent to the 2nd mixer.
The RTTY AF signal sent from the REF/DDS unit to be demodulated passes via the AGC circuit (IC1) to the mark filter circuit (IC2) and space filter circuit (IC3). The mark filter is an active bandpass filter with a center frequency of 2295Hz and a pass band width of approximately 30Hz. The space filter has a center frequency of 2125Hz.
The pass bandwidth of the 1895Hz and 1145Hz active bandpass filters is also about 30Hz. One of the three space filters is selected according to the shift width. The filter outputs are sent to the slideback detection circuit (IC4) and the drive circuit (IC6) for lighting the internal mark/space LED indicators.
The slideback detection circuit mixes the mark and space signals before detection. The demodulated code passes to the data line via the gate, which inverts the code from normal to reverse, and is sent to the CED-860 DISPLAY unit.

1.2.3 CDA-752 DSP UNIT

The DSP unit consists of the 3rd local oscillation circuit, 3rd mixer, A/D Convertor (ADC), DSP circuit, D/A Convertor (DAC), and line amplifier, etc.
In the 3rd local oscillation circuit, the 20MHz reference frequency is divided by IC7 to create a 434.78kHz signal which is supplied to the 3rd mixer (IC11).
The 3rd mixer mixes the 455kHz 2nd IF signal and 434.78kHz 3rd local signal to output a 20.22kHz 3rd IF signal.
The 3rd IF signal is converted by the ADC (IC8) into a digital signal, which is supplied to the DSP (IC1). The DSP not only performs the necessary demodulation but also the BWC, PBS, NB, AGC, NOTCH, and BFO processes, etc. The digital signal demodulated by the DSP is converted back to analog by the DAC (IC9), amplified by the audio amplifier (IC13), and output.

1.2.4 CGA-184 LOOP1 UNIT

The LOOP1 unit is a PLL synthesizer that generates signals at 1Hz steps between 70.555 and 100.454999MHz. It consists of a frequency converter, VCO, and PLL IC.
TR15 of the frequency converter is frequency tripler circuit that creates a 60MHz signal from a 20MHz signal. The 60 MHz signal is supplied to pin 6 of IC6. IC6 is a mixer that converts the 2.545 to 2.045MHz signal from the DDS into a signal between 57.455 and 57.955MHz. The unwanted component in the converted signal is eliminated by the SAW filter (FL3), and the signal is then amplified by TR18. The amplified signal is supplied to pin 1 of IC3.
The VCO block consists of four VCOs between 70.555 and 100.454999MHz, as shown below.

TR1 VCO1 70.555～78.454999MHz
TR2 VCO2 78.455～84.954999MHz
TR3 VCO3 84.955～91.954999MHz
TR4 VCO4 91.955～100.454999MHz

Transistors TR5, TR6, TR7, and TR8 switch any one of VCO1, VCO2, VCO3, and VCO4 ON under control from the CPU according to the frequency. The signal output from the VCO passes via the buffer amplifier (TR9) to the local amplifier (IC1 and IC2). The output from IC1 passes the BPF to be supplied to the receiver block as the 1st local signal. The output from IC2 is used by the PLL and is converted by the mixer (IC3) in the next stage to a signal between 13 and 43MHz. This signal passes the LPF and buffer amplifier (IC4) and is supplied to the PLL IC (IC5). Figure 1-2 shows the internal structure of the PLL IC (IC5).

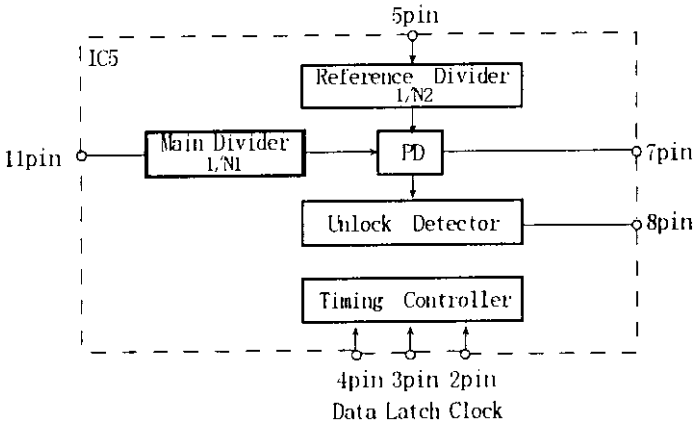


Figure 1-2 Internal Structure of IC5

The division ratio of the divider in IC5 is as follows:

$N_1 = 26 \sim 86$

$N_2 = 20$

The ratio is set by serial data from the CPU. The PLL reference frequency is 500kHz. A 10MHz signal is therefore supplied to pin 5 of IC5.
Figure 1-3 shows the relationship between the receiving frequency (fR), VCO frequency (fVCO), the frequency at pin 11 of IC5 (fIF), and the division ratio (N1) of the main divider.

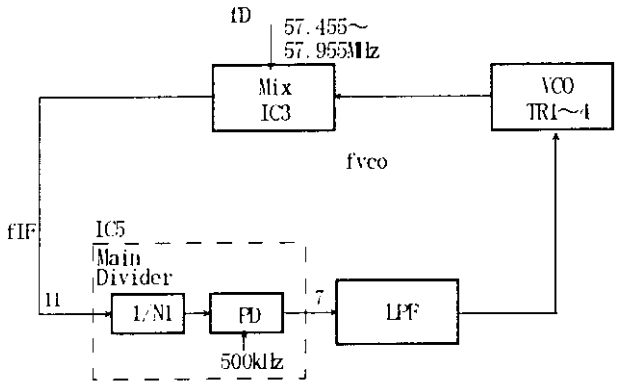


Figure 1-3 LOOP1 Configuration

F1 is the portion of the receiving frequency fR that is divisible by 500kHz. F2 is the remaining digits L1. For example, when fR is 2.154MHz, F1 is 2.0MHz and F2 is 0.154MHz.

$$f_{vco} = 70.455 + f_R$$
$$f_{vco} = f_{IF} + f_D$$
$$N_1 = 2 \times (13 + F_1)$$
$$f_{IF} = N_1 \times 0.5\text{MHz}$$
$$f_D = 57.455\text{MHz} + F_2$$

As an example, when fR=12.545MHz, N1, fIF, fD, and fvco are as follows:

$f_R = 12.545\text{MHz}$
$F1 = 12.5\text{MHz}$
$F2 = 0.045\text{MHz}$
$f_{vco} = 70.455\text{MHz} + 12.545\text{MHz}$
$= 83\text{MHz}$
$N_1 = 2 \times (13 + 12.5)$
$= 51$
$f_{IF} = 51 \times 0.5\text{MHz}$
$= 25.5\text{MHz}$
$f_D = 57.455\text{MHz} + 0.045\text{MHz}$
$= 57.500\text{MHz}$

1.2.5 CGK-160 REF/DDS UNIT

The REF/DDS unit includes the 20MHz STD OSC unit, the DDS unit, which is part of the synthesizer that generates the 70.555 to 100.454999MHz 1st local signal, the unit that generates the 70MHz 2nd local signal, and the audio amplifier.
The 20MHz STD OSC unit consists of a 20MHz crystal OSC built around TR2, and buffer amplifiers around TR3, TR4, TR6, and TR7, and IC2, which is a 1/2 divider. The respective reference frequencies for the synthesizers, and the DSP reference frequency are supplied from the OSC unit. The signal (20MHz) output from TR2 is supplied via the buffer amplifier (TR3) to pin 3 of IC2. This 1/2 divider creates a 10MHz signal from the 20MHz signal output from TR2. This signal is shaped by the LPF and is then supplied to the LOOP 1 unit.
The DDS unit consists of a high-speed DDS IC (IC1) and a BPF.
The DDS IC outputs according to the parallel data from the CPU a signal of between 2.545 to 2.045MHz based on the 20MHz reference signal supplied to pin 9 of IC1.
The unwanted component is eliminated from the 2.545 to 2.045MHz signal by the BPF and the signal is then supplied to the LOOP 1 unit (CGA-184).
In the case of the 70MHz 2nd local signal, the higher-harmonic component (x7) of the 10MHz signal derived from IC2 is separated out by the 70MHz tuning circuit(TR8) and BPF. The 2nd local signal is supplied to the 1st IF unit (CFH-71).
The demodulated signal supplied from the DSP unit passes via the analog switch (IC3), the pre-audio amp (IC5), where it is amplified, to the audio amplifier on the motherboard unit (CFQ-8350).

1.2.6 CHE-199 WB UNIT

The WB unit converts the 30MHz to 1999.999MHz receiving frequency into a 10.7MHz signal.
Variable-voltage tuning (electronic tuning using capacitance diodes) is used for the front end double tuning circuit, allowing continuous tuning to the receiving frequency. A bandpass filter is used for frequencies of 1104.8MHz and above. A wideband amplifier (GN1010) is used for the RF amplifier to improve sensitivity. The 1st mixer uses a wide band DBM to convert the 1st IF frequency to 268.7MHz or 806.1MHz. The 1st IF frequency is amplified by the IF amplifier, is input to the 2nd mixer, and converted to the 2nd IF frequency of 10.7MHz.

Receiving frequency	1st IF Frequency	2nd IF Frequency
30MHz～567.4MHz	806.1MHz	10.7MHz
567.4MHz～1642.2MHz	268.7MHz	10.7MHz
1642.2MHz～1999.999MHz	806.1MHz	10.7MHz

Except for WFM mode, the 2nd IF frequency is input to the RF TUNE unit (CFL-356), passes the double-tuning circuit, and is supplied to the RF amplifier circuit. Subsequently, the signals are converted in the same way as 30MHz signals and below. In WFM mode, the 2nd IF frequency passes via the 2nd IF filter to the WFM demodulator IC where it is converted to an analog signal. It is then supplied to the analog switch (IC3) of the REF/DDS unit (CGK-160).
The PLL synthesizer block comprises the VCO units for the 1st and 2nd local signals, and the VCO frequency-doubler circuit.
The 1st local signal, which ranges from 836.1 to 1373.5MHz, is obtained by doubling the VCO oscillation frequency. The 2nd local signals are 258.0MHz and 795.4MHz, generated by dedicated VCOs.

VCO1 418.05～473.25MHz (1st Lo=836.10～946.50MHz)
VCO2 473.25～535.80MHz (1st Lo=946.50～1071.60MHz)
VCO3 535.80～606.60MHz (1st Lo=1071.60～1213.20MHz)
VCO4 606.60～686.75MHz (1st Lo=1213.20～1373.50MHz)

Receiving frequency	1st Local Frequency	2nd Local Frequency
30MHz～567.4MHz	836.1～1373.5MHz	795.4MHz
567.4MHz～1104.8MHz	836.1～1373.5MHz	258.0MHz
1104.8MHz～1642.2MHz	836.1～1373.5MHz	258.0MHz
1642.2MHz～1999.999MHz	836.1～1193.899MHz	795.4MHz

1.2.7 CDE-860 DISPLAY UNIT and JACK UNIT

The DISPLAY and JACK units consist of the CPU, the data processing circuits for the panel switches, backup RAM, real-time clock oscillator, and the variable resistors connected to the control knobs on the panel.
The 8-bit CPU (IC6) runs using the clock supplied by a 31.9488MHz oscillator.
The EP-ROM (IC8) has a capacity of 1MB. The I/O controller (IC1 and IC15) is based on an IC developed by JRC. IC9 is a 16kB backup RAM.
IC2 processes the data for the rotary encoder (PG1) for the tuning knob and the rotary encoder (PG2) for the fine tuning knob.
LCD1 is an LCD module with built-in display driver.
IC10 is a real-time clock IC, which is supplied directly from the power supply circuit even when the power switch is OFF. A circuit built around IC18, IC19, TR3, and TR4 generates the voltage applied to the variable capacitance diodes in the double-tuning circuit of the RF TUNE unit. The voltage is varied between 5.47 and 20V in relation to the frequency of the receiving signal.
IC17 is an analog switch that switches between the AF signal and RTTY FINE TUNE voltage.
The JACK unit consists of the PHONES jack (J33) and RECORD jack (J34).

1.2.8 CFQ-8350 MOTHERBOARD, AVR UNIT, and CHASSIS

The motherboard consists of the connectors linking the respective units, the AF power AMP circuit (IC7), the RS-232C IC (IC6), and others.
The motherboard also includes the AC power rectifier diodes (CD6, 7, 8, and 9), the DC supply reverse current protection diode (CD4), the TIMER OUT relay (K1), the signal I/O connectors on the back panel, and the connectors for the panel unit.
The chassis consists of the CBD-1363AVR unit, voltage connectors (J1 and J2), and the power supply transformer (T1), etc. The speaker is mounted on the top cover.

EXHIBIT 6

BANDSWITCHING RANGES

30.000	-	108.000	MHz
108.001	-	280.000	MHz
280.000	-	567.400	MHz
567.401	-	1104.800	MHz
1104.801	-	1240.000	MHz
1240.001	-	2000.000	MHz