VHF/FM RADIO TELEPHONE JHS-500

Technical Description

1. RECEIVING CIRCUIT OPERATION:

1.1 Antenna Switching Circuit:

A signal received at the antenna terminal(J101) goes to the antenna switching circuit composed of pin diode D102 and D201 via the low pass filter. When a signal is received, D102 is ON, and D201 is OFF.

1.2 High Frequency Amplifier Circuit:

The high frequency signal from the antenna switching circuit is inputted to the transistor RF AMP(Q101) via D102. It is supplied to the 1st mixer AMP(Q102) after going through BPF which controls undesired signals. This 1st mixer is mixed with the receiving signal at the local oscillator(VCO: receiving signal + 46.025 MHz) and converted to 46.025 MHz 1st intermediate frequency.

1.3 1st Intermediate Frequency Amplifier Circuit

The 1st intermediate frequency signal generated in the mixer circuit is amplified at the 1st IF AMP (U101) after undesired signals are removed by the crystal filter(Z101).

1.4 2nd Intermediate Frequency Amplifier Circuit:

The 1st intermediate frequency signal is supplied to the 1st IF AMP(U101), which is composed of a local oscillating circuit, a mixer circuit, a limiter amplifier circuit, a remodulation circuit and a squelch circuit.

The 1st intermediate frequency signal is converted to 455 kHz 2nd intermediate frequency signal after being mixed with the output signal which is composed in the local oscillating circuit in IC(U101) and the crystal oscillator (Y101: 45.570 MHz).

The obtained signal is filtered by a ceramic filter (Z103,Z104) to discard the undesired signals, and then is amplified in the limiter amplifier circuit.

The amplified 2nd intermediate frequency signal is re-modulated by the

re-modulation circuit composed of a circuit in IC(U101) and a ceramic discriminate element (Z102).

Then it is outputted as a low frequency signal. This re-modulated low frequency signal obtains -6dB/oct response by passing through the de-emphasis circuit which is composed of LPE(U102), and goes into the low frequency amplifier.

1.5 Low Frequency Amplifier Circuit and Squelch Circuit:

The re-modulated low frequency signal is amplified by AMP(U403). Its volume can be controlled by the volume(VR501). Busy signal, generated in the squelch circuit in IC(U101), is processed to mute signal in CPU(U508). This signal switches the low frequency signal on and off by driving the transistor switch(Q506).

WX Alert Detection:

If 1050 Hz tone signal is contained in the receiving signals, it is detected by the tone detector(U503), processed in CPU, and outputted as an alert signal from CPU.

2. TRANSMITTING CIRCUIT OPERATION

2.1 Exciter Amplifier and Power Amplifier Circuit:

When the PTT switch of the microphone is pressed, the mode turns to transmitting, and frequency of PLL is set up to transmitting frequency. At the same time, transistors of the transmitting/receiving shift circuits(Q406,Q409 and Q411) are driven to operate VCO(Q301).

The high frequency signal of VCO (Q301) is amplified by the Buffer Amplifier(Q303) and the Exciter Amplifiers(Q201, Q202), and supplied to Power Module(U201). It is power- amplified to the maximum output of 25W in the Power Module(U201), and outputted from the Antenna Terminal(J101) via the Antenna Switching Circuit diodes(D102,D201).

2.2 FM Modulation Circuit:

Voice signal from the microphone is amplified by the amplifier(U401a), and gets pre-emphasis response of 6 dB/oct in the range of 300 Hz ～3 kHz. The amplitude of this signal is limited by the limiter circuit(D401), and its high frequency distortion is eliminated by LPFs(U402a,U402b). Then it is inputted to TX,VCO circuit as a

modulation signal. This modulation signal is supplied to a variable capacity diode (D303) attached to VCO circuit(Q301), and FM-modulated.

2.3 APC(Automatic Power Control):

A part of the power amplified by power module(U201) is converted to direct current signal voltage by diode (D202). This direct current voltage is amplified by direct current amplifiers(Q203,Q204,Q205), and controls power source voltage of the power module(U201). Output power is switched between 1w and 25w with 1w/25w switch (Q207) which is controlled by the direct current amplifier. VR201 and VR202 are used for fine tuning of 1w and 25w, respectively. Then the output power is outputted through the low pass filter circuit (L201,L202,L203,L212,C201,C202,C203,C204 and C244) which suppress spurious emissions.

3. PLL SYNTHESIZER

PLL IC(U301) oscillates 12.8 MHz frequency by crystal oscillator(Y301). This 12.8 MHz frequency is divided into 1/512 by the divider inside the IC to make 25 kHz frequency, the reference frequency of PLL control. Transmitting frequency and receiving frequency are set up respectively when data(DATA,CLK,STB) are sent from CPU(U508) to PLL IC(U301). This oscillating frequency of VCO is compared with the reference frequency to get the difference, which represents DC voltage transformation. The transformed DC voltage is supplied to the control diode of VCO(D301) through LPF for fine tuning of frequency.

4. DSC CALLING AND RECEIVING

4.1 FSK Modulation Section:

4.1.1 FSK space signal (FDS=16.8KHz) and mark signal (FDM=10.4KHz) are generated from CPU.

4.1.2 During DSC transmission, DSC data (XD) is transmitted from CPU. According to “H” or “L” of this data, the analog switch U503 switches the signal to “mark” or “space”.

4.1.3 Then the mark signals and the space signals are divided to 1/8 respectively by the divider U504 to make the output of the space signal 2100Hz and the mark signal 1300Hz. Higher harmonics contained in these outputted signals are attenuated by LPF to obtain FSK signals which are complied with CCITT V23. Then these FSK

signals are inputted to the modulation section.

4.1.4 Phase shift that occurs at switching by the analog switch U503 can beminimized by making the mark and space frequencies generated from CPU 8 times higher.

4.2 FSK Demodulation Section:

4.2.1 After demodulated in the receiving section, FSK signals are inputted to FSK demodulation IC U501 via buffer amplifier Q501.

4.2.2 VCO in the demodulation IC U501 constantly oscillates non-synchronized frequency of about 1700Hz. When the space signal 2100Hz and the mark signal 1300Hz are inputted to U501, VCO is locked at 2100Hz or 1300Hz, and at the same time, control voltage of VCO is fixed to the voltage corresponding to each frequency.

4.2.3 This VCO control voltage is compared with RF voltage of the comparator, then the demodulated FSK signals are outputted to CPU.