ADC
TELECOMMUNICATIONS

EXHIBIT IX

OPERATIONAL DESCRIPTION

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description

The BTS-7010 Broadband Booster can be subdivided further as follows:

QAM Modulator	- 100BastT Ethernet Input - 44 MHz QAM IF Output - Universal Card - Downstream Card - Host Card - Power Supply Card/s
QAM Upconverter	- 44 MHz IF Input - 53 to 857 MHz UHF Output - Input/Output Level Adjust - Automatic IF AGC - Agile (Selectable) Output Frequency - RS232/RS485 Remote Control - Internal High Stability Frequency Reference
Broadband Booster	- 222 to 408 MHz QAM Input - 2500 to 2690 MHz Output - Multiplexer Assembly - Downstream Switch Assembly - Upconverter Assembly - Power Amplifier Assembly - Bandpass Filter Assembly - Downstream Controller Assembly - 10 MHz Frequency Reference Assembly - Power Supply Assembly

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description

Wireless Modem Termination System (WMTS)

For complete description of WMTS see Exhibit III (BTS-7010, Wireless Modem Termination System).

The WMTS provides full duplex 100BaseT Ethernet interface to the network. The WMTS arranges the incoming Ethernet data frames, multiplexes (TDM) and modulates the downstream carrier to produce a 64 QAM, 44 MHz IF output signal that feeds the input of the BTS-7010 Broadband Booster.

The WMTS can support up to two downstream output channels per chassis. Single channel downstream operation requires the following cards:

Host Card

Two Universal Cards
- Unpopulated Universal Card (automatically functions as Carrier and Forward Card)
- Populated Universal Card (w/ Downstream Card)

Downstream Card

Power Supply Card (second power supply card may be added for redundancy)

A second downstream channel may be added with the addition of a second Universal Card and Second Downstream Card.

The input signal enters the system through a 100BaseT connector located on the front panel of the Carrier and Forward Card. This card manages the entire WMTS and runs an SNMP administrator management interface program. The signal is passed to the appropriate Downstream/Universal Card which sends the signal, still in digital format, to the Downstream Card. The Downstream Card converts the signal to the appropriate modulated format (64 QAM) and frequency (44 MHz).

The Host Card provides bus arbitration, system clock and timing. A second Host Card may by added for redundancy.

The Power Supply Card is an auto-ranging AC supply (90 – 264VRMS) from 47 – 63Hz. A second Power Supply Card may be added for redundancy.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Frequency Agile QAM Upconverter

For complete description of QAM Upconverter see Exhibit IV (BTS-7010, Frequency Agile QAM Upconverter).

The Wavecom MA4040D frequency agile upconverter is a fully agile IF upconverter designed for cable, MMDS and LMDS applications.

The MA4040D is a modular circuit card designed to be used in a MA4002D card chassis with up to 10 independent MA4040D frequency agile upconverters. The cards are powered with a common MA4011D power/control module.

The MA4040D upconverts a 44 MHz IF input signal to any selectable 6 MHz channel from 53 to 857 MHz. Front panel push buttons are used to select the output frequency which is variable in 12.5 KHz steps.

Using advanced design, the MA4040D maintains a phase noise specification that exceeds the DOCSIS requirements for 64/256 QAM. Low out of band noise performance and low spurious are achieved through high level mixing, a microwave frequency IF and multiple levels of filtering.

The MA4040D uses an automatic IF AGC circuit to correct for input level changes and provides a high level output of +61 dBmV. Local oscillators are frequency synthesized and locked to a common internal high stability reference.

The Power/Control Module contains a auto ranging switching power supply that operates from 100 to 240 VAC and local control via an LCD and 4 soft touch push buttons.

AN RF Output port, RF Sample Port and IF Input port are located on the rear of the card.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Broadband Booster

The BTS-7010 is a complete MDS/MMDS/ITFS multi-channel booster capable of operating as digital television/data transmitter in a N+1 redundant configuration. The unit is comprised of four main transmitters or Sectors and a back-up Sector. Each transmitter sector is comprised of a Multiplexer Assembly, , Upconverter Assembly, Power Amplifier Assembly, Bandpass Filter Assembly and Downstream Controller Assembly. The Back-up sector is comprised of a Downstream Switch Assembly, Back-up Upconverter Assembly, Back-up Amplifier Assembly, and Transfer Switch Assembly. Back-up operation is directed and controlled by the Automatic Back-up System (ABS) Controller Assembly.

System Monitoring is provided by the System Monitoring Assembly and a reference frequency is provided by the 10 MHz Reference Assembly.

Power to the system is provided by the Power Supply Assembly. The Power Supply Assembly is a dual output supply capable of operating in a redundant N+1, hot swap application with a second or third supply.

Each of the Assemblies are described in detail below.

Multiplexer Assembly

The 6MHz wide, 222 to 408 MHz IF output signal from the MA4040D Frequency Agile Upconverter is applied to one of four IF input jacks (J211, J212, J213, J214) on the rear of the BTS1.0 transmitter. These four jacks provide the inputs to each of the four transmitter sectors of the BTS1.0. Each of the four sectors are identical in design and function and therefore only one will be described.

This IF input signal is then fed to the Multiplexer Assembly (1113588) at Jack J1 pin 22. The IF (222-408 MHz) signal is filtered then split into two signals by IC splitter U1. One output (J34-11) is fed to the Downstream Switch in the back-up section of the unit. The main output (J34-5) is fed to the Upconverter Assembly.

Upconverter Assembly

The IF input from the Multiplexer is applied to the Upconverter at J4 and can range from +50 to +70 dBmV. The signal is filtered and applied to a PIN attenuator ALC circuit which automatically adjust the IF level into a high level IP3 mixer for optimal frequency conversion to the RF band. Fault detection of the IF signal level into the mixer is indicated through front panel LED illumination. These faults are also communicated to the Downstream Controller Assembly by providing low impeadance on rear connector Ji-8C. If the input signal has been lost, the IF ALC circuit will become muted. The IF ALC may be placed into the Manual (Manual1) or Automatic (ALC1) modes using front panel switch SW1. Placing SW1 into the Manual 1 mode allows manual adjustment of the gain through the IF stages leading to the mixer by adjusting front panel potentiometer R29. Placing SW1 into the ALC1 position enables automatic control of the IF level into the mixer by adjusting front panel potentiometer R33.

The RF output of the mixer is the upper side band product generated by mixing the IF signal with the LO signal. The RF signal is filtered and amplified then fed to an RF ALC circuit which adjust the output level based on the detected output level in the final amplification stage of the transmitter. This detected output level is an analog voltage in the range of 0 to 5 Volts and is applied to J1-25C. The detected level is amplified and adjusted in level by potentiometer R48 to produce 2 Volts at TP2 when the final amplifier output is at 100 %.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

The RF ALC circuit may be placed into the manual (Manual 2) or ALC (ALC 2) modes of operation with front panel switch SW2. Placing SW2 into the Manual 2 position allows for manual gain through the RF stages with front panel potentiometer R52. Placing SW2 into the ALC2 position enables automatic control of the RF levels detected in the final amplifier stage and can be set by varying front panel potentiometer R40. Muting of the RF output is performed under certain conditions. Muting under loss of input can occur under the conditions previously described in the IF Section. Muting can also occur by the communication of a mute command from the Down Stream Controller Assembly. The mute status is indicated by illumination of front panel LED DS3 (Mute) and is also communicated to external modules through a low impeadance pull down.

A 2278 MHz LO is generated in a two step process. First, a digital phase frequency detector is used to phase lock a voltage controlled crystal oscillator (VCXO) to a 10 MHz reference signal supplied from the 10 MHz Reference Assembly (1129658) at J1-32B. The VCXO produces a frequency of 94.916667 MHz. In the event the 10 MHz reference is lost, a hold over circuit will maintain the VCXO circuit close to 94.916667 MHz. Communication of this event is communicated to external modules through a low impedance pull down at J1-7C. In the second step of generating the LO, the output of the VCXO is used as the phase reference to a digital phase frequency detector which phase locks the 2278 MHz LO output of a voltage controlled ceramic resonator oscillator (VCRO). The LO frequency is then amplified and applied to the mixer. Should the phase lock loop (PLL) circuit become unlocked, front panel LED DS6 will illuminate Red. Communication of the unlocked PLL will also be provided as a low impeadance pull down to external modules at J1-1B.

Operating Status and control of the Upconverter Assembly is provided by a serial programmable Atmel microcontroller. The Atmel microcontroller operates at 3.6864 MHz. Various fault signals including Upconverter Input Fault, Upconverter Reference Fault, Upconverter Mute Indication, and Upconverter PLL Fault are reported by a digital latch IC (U83) which drives output jack J1C. A watchdog timer IC (U75) monitors the microcontroller chip select address line and will reset the Microcontroller if the status does not change after 2 seconds. A manual pushbutton (S1) reset is also provided.

Programming the micro is accomplished through serial programming port J39. The serial programmer will pull J39 pin 5 low to hold the microcontroller in reset during programming. A serial RS-485 transceiver IC (U74) provides I/O for the SCADA (supervisory control and data acquisition) monitoring and control system.

Power Amplifier Assembly

The Power Amplifier Assembly consist of a Power Amplifier Board (1165711), Input Signal Correction Board (1156444), Signal Cancellation Board (1156442), Correction Amplifier Board (1165714) Manual Control Board (1155954) and 8 Section Bias Protection Board (1586-3109). The Power amplifier assembly provides amplification of the RF signal as well as feed forward error cancellation.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

The RF input signal from the Upconverter Assembly enters through an OSP connector (J121) on the rear chassis of the Power Amplifier/Power Supply chassis and is fed to the RF input of the Power Amplifier Board. (J1). The RF signal is preamplified using a FET amplifier (Phoenix PA8003), with a gain of approximately 10 dB, then fed to a micro strip coupler which provides a -20 dB sample of the at RF signal at J2. This preamplifier (undistorted) signal is used by the feed forward correction section of the assembly (see Input Signal Correction Board description below). The unbalanced RF signal is then fed to a hybrid coupler (Z1) which converts the signal to a balanced RF signal to an FET amplifier Q2 (Fujitsu FLL600IQ-3). The FLL600IQ-3 is a 60 Watt GaAs FET that employs a push-pull design that offers ease of matching, better consistency and broader bandwidth. The amplified signal is then fed to a series of three hybrid couplers which provides balanced inputs to two additional FLL600IQ-3 FET amplifiers in quadrature (Q3 and Q4) which have a combined gain of approximately 10 dB. The RF output of the amplifiers are then converted to an unbalanced signal using three additional hybrid couplers (Z6, Z7, Z8) then to the main RF output of the board at J4. A –20 dB sample of the amplified signal is obtained using a stripling coupler This uncorrected (distorted) output sample (J3) is used by the Signal Cancellation Board (see Signal Cancellation Board description below) to generate the feed forward cancellation signal.

The DC biasing of the FET amplifiers is controlled and filtered by daughter boards which are soldered next to the amplifier devices. The DC bias drain to source currents are set by adjusting the negative gate to source voltages which are adjusted by potentiometers on the daughter boards.

An 8 Section Bias Protection Board distributes the –5VDC bias voltages and +10VDC drain voltages to the amplifier module as well as providing protection from an over current condition with board mounted fuses. The –5VDC bias voltage is generated on board using a voltage regulator (LM377T). This bias voltage is also used as an interlock signal which is fed to the Downstream Controller Assembly. If the bias voltage is lost, the control circuitry will immediately shut down the power supply, thereby removing the drain voltages from the amplifier modules and protecting the GaAs FET devices.

The input sample of the Power Amplifier Board is routed through a delay line then applied to the Input Signal Correction Board (J3). The purpose of this board is to process the undistorted preamplifier signal by adjusting the phase, gain, and shape of the RF input sample. The signal enters the Input Signal Correction Board at J3 and is applied to a series of 8 RF switches (U4 through U11) which provide the ability to apply any of 16 various lengths of delay line. The RF switches are selected by DIP switches on the Manual Control Board. The signal is then applied to a phase shift circuit comprised of two RF switches (U14 and U15) and two hybrid couplers (U13 and U18) which provides the ability to switch in either 0° or 180° phase shift. The signal is then applied to a PIN diode (CR3, CR4) shaping circuit which adjust the shape of the signal. A potentiometer on the Manual Control Board (R1) is used to set the control voltage into the PIN diode shaping circuit thereby adjusting the amount of shaping. The signal is then applied to a PIN diode attenuation circuit followed by a phase shift circuit then to the output of the board at J4. The amount of attenuation and phase shift is controlled by potentiometers on the Manual Control Board (R2 and R3).

The output of the Input Signal Correction Board is applied to the input of the Signal Cancellation Board (J3). The purpose of this board is to remove the information carrying component of the signal and process the correction (noise) signal to be used in the Correction Amplifier board.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

The phase shifted (180°), undistorted signal from the Input Signal Correction Board and the uncorrected (distorted) output sample of the Power Amplifier Board are applied to the input of the Signal Cancellation Board (J3 and J2 respectfully) where they are coupled using a micro-strip coupler. Combining these two signals cancels the information carrying component of the signal, leaving only the distortion of the output amplifier. An RF switch (U2) provides the ability to remove the power amplifier sample and terminate the coupler with 50 ohms for tuning purposes. The signal is then applied to delay a line switching circuit then to phase, gain and shape adjustment circuits similar to those described above for the Input Signal Correction Board. All adjustments and switch settings are performed on the Manual Control Board (R4, R5, R6 and SW2). The correction signal is then applied to the output of the board at J4.

The correction signal from the Signal Cancellation board is applied to the input of the Correction Amplifier Board. The purpose of this board is to cancel the distortion created by the output amplifier.

The correction signal is amplified using two FET amplifiers (Mini-Circuits ERA-5) then converted to a balanced signal using a hybrid coupler. The signal is then amplified by two additional amplifiers in quadrature (also ERA-5's). The signal is amplified once again using two FET amplifiers (Phoenix PA8003) in quadrature.

The RF output of the Power Amplifier is fed to J9 of the Correction Amplifier Board. The amplified correction signal and the Power Amplifier output signal are applied to a hybrid microstrip coupler where the two signals are coupled together, effectively canceling the distortion in the output signal. The RF output signal is fed to the output of the board at J10. A sample of the output signal is obtained using a microstrip coupler. The sample is applied to an RMS detector IC (U11) which provides a DC voltage proportional to the RF output level.

A voltage regulator IC (U8) is used to provide +5VDC to the RMS detector.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Bandpass Filter Assembly

The Bandpass Filter Assembly consist of a Bandpass Filter Module and Bandpass Filter Control Board. The Band Pass Filter Assembly provides filtering of the RF output signal as well as the capability to switch between the main RF input from the Power Amplifier Assembly or the auxiliary RF input from the Back-up Power Amplifier Assembly.

The main and auxiliary RF inputs enter the bandpass filter module at J2 and J1 respectfully and are applied to RF switch SW1. The unselected input is terminated into a 50 Ohm load. The selected signal is fed to a six pole bandpass filter (2500-2686 MHz), which passes the desired signal while attenuating unwanted harmonics and spurious frequencies, then to the RF output port J3. Two -20 dB directional couplers are used to obtain forward and reflective power samples of the RF signal. The forward sample is split into two signals. One signal is connected to the Reflected Sample port J7. The other signal is applied to a forward power measuring circuit consisting of an RMS detector (U1) and Hitite switch (U3). Any reflected power from antenna mismatch is diverted by a circulator to the Reflected Power Sample Port J6 and to a reflected power measuring circuit which consist of a Log detector (U2).

A serial programmable Atmel microcontroller located on the Bandpass Filter Control Board controls the RF switch via two MOSFET switches (Q20 and Q21). Relay status signals as well as the forward and reflected power levels from the power detectors are monitored by the microcontroller. The Bandpass Filter Control Board also provides forward and reflected power level calibration adjustments with on board potentiometers (R67 and R76).

Upstream/Downstream Switch Assembly

The Upstream/Downstream Switch Assembly consist of a Dual SP4T RF Switch Board and Upstream/Downstream Control Board (1125362). The Upstream/Downstream Switch Assembly functions as part of the back-up system in determining which of the four main RF inputs from the four Multiplexer Assemblies is routed to the Back-up Upconverter Assembly.

The four input signals from the Multiplexer Assemblies are applied to the Dual SP4T RF Switch Board at J2 (J2-22B, J2-25B, J2-28B, and J2-31B) and fed to the inputs of a SP4T RF switch (U2). The position of the switch is determined by the logic levels present on pins 9 and 10 of U1 (Control A and Control B). These control lines are driven by a serial programmable Atmel microcontroller located on the Upstream/Downstream Switch Control Board. The microprocessor receives the command for the proper switch setting from the Automatic Back-up System (ABS) Assembly which is also part of the back-up system. Switch setting may also be set through serial commands (J2-20B and J2-20C) from the SCADA (supervisory control and data acquisition) program. A front panel LED (labeled Back-up Enabled) located on the front panel of the assembly indicates that a back-up has been activated.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Downstream Controller Assembly

The Downstream Controller Assembly is comprised of a single circuit board – the Downstream Controller Board (1132140). The Downstream Controller Board provides monitoring and control of the transmitter and functions as an integral part of the system user interface (see System Monitoring Assembly) and automatic back-up system (see Automatic Back-up System Assembly).

The Downstream Controller Board consist of an 16-bit microcontroller (MC68HC705B16CFN) and associated control circuitry. The microcontroller monitors the operating status of the various assemblies of the transmitter. Critical faults for a particular assembly are reported by way of an interlock line.

The interlock signal from the Upconverter Assembly enters the board at J1-17A. The Upconverter interlock signal indicates the presence of one or more of the following faults: loss of input signal, +12 volt source too low, +9 volt source too low, -5 volt source too high, ALC voltage too high, PLL unlocked.

The interlock signal from the Power Amplifier Assembly enters the board at J1-1A. The Power Amplifier interlock signal indicates the presence of one or more of the following faults: device not installed, supply voltage below +10 volts, power supply faulted, output status faulted, over temperature.

The interlock signal from the Bandpass Filter Assembly enters the board at J1-1B. The Bandpass Filter interlock signal indicates the device is not installed or the supply voltage is below +10 volts.

After receiving an interlock fault, the Downstream Controller Board sends a Downstream Controller interlock (J1-7B) fault to the Automatic Back-up System (see Automatic Back-up System Assembly) which controls the back-up operation. The ABS then sends a back-up command on J1-27 instructing the Downstream Controller to place the Power Amplifier Assembly into standby and a second instruction to switch the Bandpass Filter Assembly to the Alternate position. The Downstream Controller board then sends a command (J1-23B) to the Back-up Downstream Controller which causes the back-up transmitter to go into the operate mode.

Back-up Upconverter Assembly

The Back-up Upconverter Assembly works as part of the back-up system and serves as a back-up upconverter should on of the four main upconverters fail. The output of the Upstream/Downstream switch Assembly provides the input to the Back-up Upconverter. The Back-up Upconverter Assembly is identical in design and function to the main Upconverter Assembly described above.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Back-up Power Amplifier Assembly

The Back-up Power Amplifier Assembly functions as part of the back-up system and serves as a back-up amplifier should on of the four main amplifiers fail. The output of the Back-up Upconverter Assembly provides the input to the Back-up Power Amplifier. The Back-up Power Amplifier Assembly is identical in design and function to the main Power Amplifier Assembly described above.

Downstream Transfer Switch Assembly

The Downstream Transfer Switch Assembly consist of a SP4T RF Transfer Switch, Downstream Transfer Switch Control Board (1121614) and Front Panel LED Board (1113710). The Downstream Transfer Switch Assembly functions as part of the back-up system by routing the output of the Back-up Power Amplifier to one of the four Bandpass Filter Assemblies.

The input signal from the Back-up Power Amplifier Assembly enters at J90 of the Bandpass Filter Chassis and is routed to the RF input of the SP4T RF switch. The switch position is selected by a serial programmable Atmel microcontroller, located on the Downstream Transfer Switch Control Board, which drives one of four FET switches (Q2, Q4, Q6, and Q8) which in turn energizes the appropriate coil in the RF switch. The microprocessor receives the command for the proper switch setting from the Automatic Back-up System (ABS) Assembly which is also part of the back-up system. The Front Panel LED Board located on the front panel of the assembly indicates current switch position. The output of the Downstream Transfer Switch Assembly is routed to the Bandpass Filter Assembly auxiliary input of the failed Sector.

Automatic Back-up System Assembly

The ABS Assembly is composed of a ABS Controller Board (1132142). The ABS Controller functions as part of the back-up system by monitoring the operating status of the four main transmitters and controlling the back-up process in the event of a fault.

The ABS Controller Board interfaces with the backplane using a 96 position connector (J1) then with external modules through three ribbon cable connections (J14, J16 and J22 of Control Module Backplane Board (1119953)). The ABS Controller Board consist of an 16-bit microcontroller (MC68HC705B16CFN) and associated control circuitry. The microcontroller monitors interlock lines from each of the Down Stream Controller Assemblies. The interlock line signals the presence of a critical transmitter fault. Upon receiving an interlock fault, the ABS begins the back-up process as described below.

Once the interlock fault is received by the microcontroller the micro will first check the priority level of the faulted sector. Priority level is fixed according to physical chassis location (left to right = highest to lowest priority). If no other transmitter sectors are currently being backed up the ABS will back up the faulted sector regardless of priority. However, if another sector is currently being backed up by ABS, the faulted sector will only be backed up if its priority is higher than the channel being backed up. Next the ABS will check the Load Enable signal from the Power Supply Assemblies. By monitoring this signal, the ABS can determine if the appropriate number of Power Supply Assemblies are installed and functioning before performing the back-up. Next, the ABS checks the Interlock signal of the Back-up Downstream Controller Assembly to insure no faults are present in the back-up transmitter.

The ABS then sends a standby command to both the faulted transmitter and back-up transmitter. After standby is verified, the ABS then sends control signals to place the Downstream Switch and Downstream Transfer Switch into proper switch position. The ABS then instructs the faulted transmitter to place the input switch in the Bandpass Filter assembly into the ABS position. Finally, an instruction is sent to place the back-up transmitter into operate.

System Monitoring Assembly

The System Monitoring Assembly is composed of a Front Panel LED Board (113713), LCD Display Board, Switch Board (1527-3406) and LCD Backplane Interface Board (1116295). The System Monitoring Assembly provides the user interface for the system with a front panel LCD display and push button switches.

The LCD Backplane Interface Board operates as the interface between the LCD Display Board, Switch Board and the chassis backplane (Control Module Backplane Board). Any one of the five Downstream Controller Boards in the system may write to the data bus that drives the LCD, but only one may write at any one time. To take control of the buss, the Downstream Controller Board will send a LCD buffer enable signal to a digital latch IC (pin 11 of U6). The digital latch IC will then send a confirmation data signal back to the controller indicating that it now has control of the buss. Five analog switch IC's (U1 through U5) operate in a de-multiplexer configuration by allowing only the Downstream Controller Board that is currently controlling the bus to write the LCD control signals (LCD Enable, R/W , Data or Instruction) to the LCD display. LED driver circuits (Q12 through Q21) are used to drive the LED's on the Front Panel LED board.

The Front panel LED Board indicates operating status of each of the four main transmitter sectors as well as the back-up transmitter. Green indicates no faults are present. Red indicates that a fault is present in that sector.

Power Supply Assembly

The Power Supply Assembly is composed of a 400W switching power supply (Astec MP4/2L/1L), 1200W Power Factor Corrected AC/DC converter Board (1112214) and Front Panel LED Board (1113710). The Power Supply Assembly provides the DC power to the BTS 1.0 system.

The Power Supply Assembly is designed to work in a redundant N+1 = 2+1 configuration. The chassis accepts up to three Power Supply Assemblies. Two supplies are required to supply system power for a fully loaded system. The third supply functions as a back-up supply operating in hot standby.

The AC input to the assembly is applied to a terminal block (TB2) which distributes the AC input to the two power supplies that make up the assembly.

The 400 W Switching Power Supply provides both a +12VDC output and a –12VDC output . Both outputs are fed to Oring diodes on the 100W PFC Board (TB2-1 and TB2-4) then to the output connector (J1) on the rear of the assembly. Voltage sense signals are fed back to the supply to compensate for any voltage drop across the diode (V1-1 and 4, V2-1 and 4).

The+12VDC and –12VDC output signals of the assembly are wired to terminal blocks in the rear of the Power Amplifier/Power Supply chassis that serve to combine the output signals from the three Power Supply Assemblies and also distribute the +12VDC and –12VDC to the system.

The 1200W PFC AC/DC Converter Board provides a +380VDC output which provides power to the Power Amplifier Assemblies. The AC input enters the board at J1 and is applied to AC line filters then to the input of an Astec APA100-101 PFC module. This module is capable of providing 1200W at +380VDC. The module output is fed to Oring diodes then to the output of the board at TB3. Operating status of the module is indicated through the Power Failure Warning (PFW) control signal which is reported to system control through transistor pull down (Q3) and to the Front Panel LED Board through transistor pull up (Q5 and Q6). Operating status of the 400 W Switching Supply is indicated through the DC OK signal which is applied to the board at J4 and is then routed to pull up/pull down circuits (Q8, Q9 and Q10) similar in function to those described above. Soon after application of AC input module will output a Load Enable signal indicating that the output has stabilized. This signal is also provided to system control through transistor (Q2) pull down.

The Front Panel LED Board provides visual operating status indication of both the 400W Switching Supply and 1200 W PFC module.

10 MHz Frequency Reference Assembly

The 10 MHz Frequency Reference Assembly consist of 10 MHz Reference Board (1136560), GPS Receiver (TrueTime model 87-664), 10 MHz Reference Generator Board (1519-3126) and Front Panel LED Board (1113710). The function of the 10 MHz Frequency Reference Assembly is to select one of three possible 10 MHz reference sources (external, GPS, or internal) and distribute the signal.

The GPS Receiver Input, External 10 MHz Reference Input and Internal 10 MHz Reference Input are applied to the 10 MHz Reference Board input jacks (J1, J2 and J8A-1A respectfully) Diode detector circuits are used to detect the presence of each of the three inputs. A serial programmable Atmel microcontroller monitors the signals from the detector circuits and selects the proper reference based on order of priority (external reference first, GPS reference second and internal reference third) by energizing the coil of latching relay K1 or K2. The selected reference signal is then amplified and split to provide 4 reference signals. The four reference signals are fed to the Control Module Backplane Board (1119948) output connectors (J10 through J13) before being distributed throughout the system.

There internal reference is provided by the 10 MHz Reference Generator Board (1519-3126). The 10 MHz Reference Generator Board uses a temperature oven controlled 40 MHz VCXO. The crystal frequency is divided down to 10 MHz by divider IC U4. Crystal tuning adjustments are provided by tuning capacitors (C2 and C3). Oven temperature control is provided by an on board potentiometer (R15).

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

The GPS reference is provided by a GPS receiver manufactured by TrueTime Inc (Model 87-664). The TrueTime GPS is capable of tracking up to six satellites and has an acquisition time of less than 2 minutes, frequency output accuracy less than 3×10^{-12}.

The Front Panel LED Board (1113713) provides LED status indication of each of the three reference sources (selected/not selected, present/not present, present but faulted) as well as lock indication of the GPS source.