EXHIBIT I

FCC TYPE ACCEPTANCE REPORT

ADC TELECOMMUNICATIONS

MODEL: BTS-7010

FCC ID-CJJ79XITS-7045

MULTI-CHANEL (BROADBAND) BOOSTER

Date Filed _____

This application is filed in compliance with
Part 2, Part 21, and Part 74
of the FCC Rules and Regulations.

ADC Telecommunications
102 Rahway Road
McMurray, PA 15317

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1.0 IDENTIFICATION OF APPLICANT AND EQUIPMENT

1.1 Applicant:

ADC Telecommunications
102 Rahway Road
McMurray, PA 15317-3345

The above name and address is printed on a label attached to the rear panel of the equipment.

1.2 Equipment and Model Number: BTS-7010

This information is provided on the front panel of the equipment.

1.3 ADC Telecommunications shall manufacture this product in quantities necessary to satisfy market demand.

2.0 TECHNICAL DESCRIPTION - MODEL BTS-7010

2.1 Introduction

The BTS-7010 is a complete MMDS/ITFS, originating signal digital broadband booster designed to operate with a maximum of four input signals and a nominal output power of 5.0 Watts (total average). The BTS-7010 broadband booster system is comprised of a Wireless Modem Termination System (Vyyo V300), QAM Upconverter (Wavecom MA4040D) and BTS-7010 Broadband Booster. The WMTS receives full duplex Ethernet data frames (100BaseT), multiplexes in TDM and modulates the signal to a 64 QAM, 44 MHz IF carrier. The QAM upconverter is a fully agile upconverter that upconverts the 44 MHz IF to the desired UHF channel from 222 MHz to 408 MHz. The QAM upconverter has an automatic AGC circuit that automatically corrects for input level changes and frequency synthesized local oscillators that are locked to a common internal high stability reference. The UHF output signal from the QAM upconverter is routed the BTS-7010 broadband booster. The signal is first applied to a multiplexer circuit that splits the signal with one half leading to the back-up portion of the system and the main signal leading to the upconverter for IF signal processing and upconversion to the MMDS/ITFS frequency range (2500.00 to 2690.00 MHz). The RF signal is then fed to an amplifier module for final amplification then filtered by a 200 MHz bandpass filter before exiting the system. The BTS-7010 utilizes ALC circuitry for automatic level control of the output signal to maintain a constant power level. The BTS-7010 broadband booster system is a 19-inch rack mount assembly supplied complete with cabinet.

Parameters and specifications for operation of this unit as a digital broadband booster are provided on the following pages, and a complete circuit description and alignment procedure are also included in this report. Refer to the overall system block diagram in the Engineering Data section of the report (Section 3.0) and the particular referenced schematics located in the instruction manual exhibits (Exhibit II (Broadband Booster), Exhibit III (Wireless Modem Termination System), and Exhibit IV (Frequency Agile QAM Upconverter)).

2.0 TECHNICAL DESCRIPTION

2.2 Technical Specifications

Type of Emissions: ..... BOOSTER
Frequency Range ..... (4 simultaneous channel operation maximum) 2500 to 2690 MHz
Output Power Rating: ..... 5.0 watts (total average)
DC voltage and total current of final amplifier stage ..... 12 volts DC at 38 amps
(Class A/B - Not RF power dependent)

2.3 Performance Specifications

Operating Frequency Range (4 simultaneous channel operation maximum) ..... 2500 to 2690 MHz
RF output - Nominal:
Power ..... 5.0 watts (total average)
Impedance ..... 50 ohms
Connector ..... Type N

Input (WMTS): ..... 100BaseT Ethernet Data Frames
Connector RJ-45

Out-of-Band Power ..... Per FCC Rules (21.908)
-25 dB max (at band edges)
-40 dB max (250.00 KHz above and 250.00 KHz below band edges)
-50 dB max (3.00 MHz above and 3.00 MHz below band edges)
-60 dB max (20.00 MHz above and 20.00 MHz below band edges)
-60 dB max (Harmonic Products)

Out-of-Band Power (Unoccupied Channel) ..... Per FCC Rules (21.908)
-25 dB max (at unoccupied channel edges)
-40 dB max (250.00 KHz above and 250.00 KHz below unoccupied channel edges)
-50 dB max (3.00 MHz above and 3.00 MHz below unoccupied channel edges)

Electrical Requirements

Power Line Voltage:
WMTS QAM Modulator ..... 110 to 230 VAC, 47 to 63 Hz
QAM Upconverter ..... 100 to 240 VAC, 50/60 Hz or
Broadband Booster ..... 208 to 240 VAC, 50/60 Hz or

Power Consumption:
WMTS QAM Modulator ..... 50 watts
QAM Upconverter ..... 40 watts
Broadband Booster (ea. Sector) ..... 675 watts

Environmental

Maximum Altitude:
WMTS QAM Modulator ..... 10,000 feet (3,048m)
QAM Upconverter ..... 10,000 feet (3,048m)
Broadband Booster ..... 12,000 feet (3,660m)

2.0 TECHNICAL DESCRIPTION

2.3 Technical Specifications – continued

Ambient Temperature:

WMTS QAM Modulator	0° to 40°C
QAM Upconverter	0° to 40°C
Broadband Booster	0° to 50°C

Mechanical

Dimensions (WxDxH):

WMTS QAM Modulator	19”x 21” x 8.75”
QAM Upconverter (Upconverter Card)	1” x 13 x 5.25”
Broadband Booster :	
Band Pass Filter Chassis	17.20” x 24.36” x 6.97”
Power Amplifier/Power Supply Chassis	17.20” x 24.36” x 17.47”
Upper/Lower Signal Processing Chassis	17.20” x 24.36” x 17.47”
Control Chassis	17.20” x 24.36” x 8.72”

Weight:

WMTS QAM Modulator	12 lbs. (5.45 kgs)
QAM Upconverter (Chassis with Power Supply and Upconverter Card)	19.2 lbs. (8.8 kgs)
Broadband Booster	165 lbs. (75 kgs)

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description

The BTS-7010 Broadband Booster can be subdivided further as follows:

QAM Modulator
- 100BastT Ethernet Input
- 44 MHz QAM IF Output
- Universal Card
- Downstream Card
- Host Card
- Power Supply Card/s

QAM Upconverter
- 44 MHz IF Input
- 53 to 857 MHz UHF Output
- Input/Output Level Adjust
- Automatic IF AGC
- Agile (Selectable) Output Frequency
- RS232/RS485 Remote Control
- Internal High Stability Frequency Reference

Broadband Booster
- 222 to 408 MHz QAM Input
- 2500 to 2690 MHz Output
- Multiplexer Assembly
- Downstream Switch Assembly
- Upconverter Assembly
- Power Amplifier Assembly
- Bandpass Filter Assembly
- Downstream Controller Assembly
- 10 MHz Frequency Reference Assembly
- Power Supply Assembly

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description

Wireless Modem Termination System (WMTS)

For complete description of WMTS see Exhibit III (BTS-7010, Wireless Modem Termination System).

The WMTS provides full duplex 100BaseT Ethernet interface to the network. The WMTS arranges the incoming Ethernet data frames, multiplexes (TDM) and modulates the downstream carrier to produce a 64 QAM, 44 MHz IF output signal that feeds the input of the BTS-7010 Broadband Booster.

The WMTS can support up to two downstream output channels per chassis. Single channel downstream operation requires the following cards:

Host Card

Two Universal Cards
- Unpopulated Universal Card (automatically functions as Carrier and Forward Card)
- Populated Universal Card (w/ Downstream Card)

Downstream Card

Power Supply Card (second power supply card may be added for redundancy)

A second downstream channel may be added with the addition of a second Universal Card and Second Downstream Card.

The input signal enters the system through a 100BaseT connector located on the front panel of the Carrier and Forward Card. This card manages the entire WMTS and runs an SNMP administrator management interface program. The signal is passed to the appropriate Downstream/Universal Card which sends the signal, still in digital format, to the Downstream Card. The Downstream Card converts the signal to the appropriate modulated format (64 QAM) and frequency (44 MHz).

The Host Card provides bus arbitration, system clock and timing. A second Host Card may by added for redundancy.

The Power Supply Card is an auto-ranging AC supply (90 – 264VRMS) from 47 – 63Hz. A second Power Supply Card may be added for redundancy.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Frequency Agile QAM Upconverter

For complete description of QAM Upconverter see Exhibit IV (BTS-7010, Frequency Agile QAM Upconverter).

The Wavecom MA4040D frequency agile upconverter is a fully agile IF upconverter designed for cable, MMDS and LMDS applications.

The MA4040D is a modular circuit card designed to be used in a MA4002D card chassis with up to 10 independent MA4040D frequency agile upconverters. The cards are powered with a common MA4011D power/control module.

The MA4040D upconverts a 44 MHz IF input signal to any selectable 6 MHz channel from 53 to 857 MHz. Front panel push buttons are used to select the output frequency which is variable in 12.5 KHz steps.

Using advanced design, the MA4040D maintains a phase noise specification that exceeds the DOCSIS requirements for 64/256 QAM. Low out of band noise performance and low spurious are achieved through high level mixing, a microwave frequency IF and multiple levels of filtering.

The MA4040D uses an automatic IF AGC circuit to correct for input level changes and provides a high level output of +61 dBmV. Local oscillators are frequency synthesized and locked to a common internal high stability reference.

The Power/Control Module contains a auto ranging switching power supply that operates from 100 to 240 VAC and local control via an LCD and 4 soft touch push buttons.

AN RF Output port, RF Sample Port and IF Input port are located on the rear of the card.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Broadband Booster

The BTS-7010 is a complete MDS/MMDS/ITFS multi-channel booster capable of operating as digital television/data transmitter in a N+1 redundant configuration. The unit is comprised of four main transmitters or Sectors and a back-up Sector. Each transmitter sector is comprised of a Multiplexer Assembly, , Upconverter Assembly, Power Amplifier Assembly, Bandpass Filter Assembly and Downstream Controller Assembly. The Back-up sector is comprised of a Downstream Switch Assembly, Back-up Upconverter Assembly, Back-up Amplifier Assembly, and Transfer Switch Assembly. Back-up operation is directed and controlled by the Automatic Back-up System (ABS) Controller Assembly.

System Monitoring is provided by the System Monitoring Assembly and a reference frequency is provided by the 10 MHz Reference Assembly.

Power to the system is provided by the Power Supply Assembly. The Power Supply Assembly is a dual output supply capable of operating in a redundant N+1, hot swap application with a second or third supply.

Each of the Assemblies are described in detail below.

Multiplexer Assembly

The 6MHz wide, 222 to 408 MHz IF output signal from the MA4040D Frequency Agile Upconverter is applied to one of four IF input jacks (J211, J212, J213, J214) on the rear of the BTS1.0 transmitter. These four jacks provide the inputs to each of the four transmitter sectors of the BTS1.0. Each of the four sectors are identical in design and function and therefore only one will be described.

This IF input signal is then fed to the Multiplexer Assembly (1113588) at Jack J1 pin 22. The IF (222-408 MHz) signal is filtered then split into two signals by IC splitter U1. One output (J34-11) is fed to the Downstream Switch in the back-up section of the unit. The main output (J34-5) is fed to the Upconverter Assembly.

Upconverter Assembly

The IF input from the Multiplexer is applied to the Upconverter at J4 and can range from +50 to +70 dBmV. The signal is filtered and applied to a PIN attenuator ALC circuit which automatically adjust the IF level into a high level IP3 mixer for optimal frequency conversion to the RF band. Fault detection of the IF signal level into the mixer is indicated through front panel LED illumination. These faults are also communicated to the Downstream Controller Assembly by providing low impeadance on rear connector Ji-8C. If the input signal has been lost, the IF ALC circuit will become muted. The IF ALC may be placed into the Manual (Manual1) or Automatic (ALC1) modes using front panel switch SW1. Placing SW1 into the Manual 1 mode allows manual adjustment of the gain through the IF stages leading to the mixer by adjusting front panel potentiometer R29. Placing SW1 into the ALC1 position enables automatic control of the IF level into the mixer by adjusting front panel potentiometer R33.

The RF output of the mixer is the upper side band product generated by mixing the IF signal with the LO signal. The RF signal is filtered and amplified then fed to an RF ALC circuit which adjust the output level based on the detected output level in the final amplification stage of the transmitter. This detected output level is an analog voltage in the range of 0 to 5 Volts and is applied to J1-25C. The detected level is amplified and adjusted in level by potentiometer R48 to produce 2 Volts at TP2 when the final amplifier output is at 100 %.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

The RF ALC circuit may be placed into the manual (Manual 2) or ALC (ALC 2) modes of operation with front panel switch SW2. Placing SW2 into the Manual 2 position allows for manual gain through the RF stages with front panel potentiometer R52. Placing SW2 into the ALC2 position enables automatic control of the RF levels detected in the final amplifier stage and can be set by varying front panel potentiometer R40. Muting of the RF output is performed under certain conditions. Muting under loss of input can occur under the conditions previously described in the IF Section. Muting can also occur by the communication of a mute command from the Down Stream Controller Assembly. The mute status is indicated by illumination of front panel LED DS3 (Mute) and is also communicated to external modules through a low impeadance pull down.

A 2278 MHz LO is generated in a two step process. First, a digital phase frequency detector is used to phase lock a voltage controlled crystal oscillator (VCXO) to a 10 MHz reference signal supplied from the 10 MHz Reference Assembly (1129658) at J1-32B. The VCXO produces a frequency of 94.916667 MHz. In the event the 10 MHz reference is lost, a hold over circuit will maintain the VCXO circuit close to 94.916667 MHz. Communication of this event is communicated to external modules through a low impedance pull down at J1-7C. In the second step of generating the LO, the output of the VCXO is used as the phase reference to a digital phase frequency detector which phase locks the 2278 MHz LO output of a voltage controlled ceramic resonator oscillator (VCRO). The LO frequency is then amplified and applied to the mixer. Should the phase lock loop (PLL) circuit become unlocked, front panel LED DS6 will illuminate Red. Communication of the unlocked PLL will also be provided as a low impeadance pull down to external modules at J1-1B.

Operating Status and control of the Upconverter Assembly is provided by a serial programmable Atmel microcontroller. The Atmel microcontroller operates at 3.6864 MHz. Various fault signals including Upconverter Input Fault, Upconverter Reference Fault, Upconverter Mute Indication, and Upconverter PLL Fault are reported by a digital latch IC (U83) which drives output jack J1C. A watchdog timer IC (U75) monitors the microcontroller chip select address line and will reset the Microcontroller if the status does not change after 2 seconds. A manual pushbutton (S1) reset is also provided.

Programming the micro is accomplished through serial programming port J39. The serial programmer will pull J39 pin 5 low to hold the microcontroller in reset during programming. A serial RS-485 transceiver IC (U74) provides I/O for the SCADA (supervisory control and data acquisition) monitoring and control system.

Power Amplifier Assembly

The Power Amplifier Assembly consist of a Power Amplifier Board (1165711), Input Signal Correction Board (1156444), Signal Cancellation Board (1156442), Correction Amplifier Board (1165714) Manual Control Board (1155954) and 8 Section Bias Protection Board (1586-3109). The Power amplifier assembly provides amplification of the RF signal as well as feed forward error cancellation.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

The RF input signal from the Upconverter Assembly enters through an OSP connector (J121) on the rear chassis of the Power Amplifier/Power Supply chassis and is fed to the RF input of the Power Amplifier Board. (J1). The RF signal is preamplified using a FET amplifier (Phoenix PA8003), with a gain of approximately 10 dB, then fed to a micro strip coupler which provides a -20 dB sample of the at RF signal at J2. This preamplifier (undistorted) signal is used by the feed forward correction section of the assembly (see Input Signal Correction Board description below). The unbalanced RF signal is then fed to a hybrid coupler (Z1) which converts the signal to a balanced RF signal to an FET amplifier Q2 (Fujitsu FLL600IQ-3). The FLL600IQ-3 is a 60 Watt GaAs FET that employs a push-pull design that offers ease of matching, better consistency and broader bandwidth. The amplified signal is then fed to a series of three hybrid couplers which provides balanced inputs to two additional FLL600IQ-3 FET amplifiers in quadrature (Q3 and Q4) which have a combined gain of approximately 10 dB. The RF output of the amplifiers are then converted to an unbalanced signal using three additional hybrid couplers (Z6, Z7, Z8) then to the main RF output of the board at J4. A –20 dB sample of the amplified signal is obtained using a stripling coupler This uncorrected (distorted) output sample (J3) is used by the Signal Cancellation Board (see Signal Cancellation Board description below) to generate the feed forward cancellation signal.

The DC biasing of the FET amplifiers is controlled and filtered by daughter boards which are soldered next to the amplifier devices. The DC bias drain to source currents are set by adjusting the negative gate to source voltages which are adjusted by potentiometers on the daughter boards.

An 8 Section Bias Protection Board distributes the –5VDC bias voltages and +10VDC drain voltages to the amplifier module as well as providing protection from an over current condition with board mounted fuses. The –5VDC bias voltage is generated on board using a voltage regulator (LM377T). This bias voltage is also used as an interlock signal which is fed to the Downstream Controller Assembly. If the bias voltage is lost, the control circuitry will immediately shut down the power supply, thereby removing the drain voltages from the amplifier modules and protecting the GaAs FET devices.

The input sample of the Power Amplifier Board is routed through a delay line then applied to the Input Signal Correction Board (J3). The purpose of this board is to process the undistorted preamplifier signal by adjusting the phase, gain, and shape of the RF input sample. The signal enters the Input Signal Correction Board at J3 and is applied to a series of 8 RF switches (U4 through U11) which provide the ability to apply any of 16 various lengths of delay line. The RF switches are selected by DIP switches on the Manual Control Board. The signal is then applied to a phase shift circuit comprised of two RF switches (U14 and U15) and two hybrid couplers (U13 and U18) which provides the ability to switch in either 0° or 180° phase shift. The signal is then applied to a PIN diode (CR3, CR4) shaping circuit which adjust the shape of the signal. A potentiometer on the Manual Control Board (R1) is used to set the control voltage into the PIN diode shaping circuit thereby adjusting the amount of shaping. The signal is then applied to a PIN diode attenuation circuit followed by a phase shift circuit then to the output of the board at J4. The amount of attenuation and phase shift is controlled by potentiometers on the Manual Control Board (R2 and R3).

The output of the Input Signal Correction Board is applied to the input of the Signal Cancellation Board (J3). The purpose of this board is to remove the information carrying component of the signal and process the correction (noise) signal to be used in the Correction Amplifier board.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

The phase shifted (180°), undistorted signal from the Input Signal Correction Board and the uncorrected (distorted) output sample of the Power Amplifier Board are applied to the input of the Signal Cancellation Board (J3 and J2 respectfully) where they are coupled using a micro-strip coupler. Combining these two signals cancels the information carrying component of the signal, leaving only the distortion of the output amplifier. An RF switch (U2) provides the ability to remove the power amplifier sample and terminate the coupler with 50 ohms for tuning purposes. The signal is then applied to delay a line switching circuit then to phase, gain and shape adjustment circuits similar to those described above for the Input Signal Correction Board. All adjustments and switch settings are performed on the Manual Control Board (R4, R5, R6 and SW2). The correction signal is then applied to the output of the board at J4.

The correction signal from the Signal Cancellation board is applied to the input of the Correction Amplifier Board. The purpose of this board is to cancel the distortion created by the output amplifier.

The correction signal is amplified using two FET amplifiers (Mini-Circuits ERA-5) then converted to a balanced signal using a hybrid coupler. The signal is then amplified by two additional amplifiers in quadrature (also ERA-5's). The signal is amplified once again using two FET amplifiers (Phoenix PA8003) in quadrature.

The RF output of the Power Amplifier is fed to J9 of the Correction Amplifier Board. The amplified correction signal and the Power Amplifier output signal are applied to a hybrid microstrip coupler where the two signals are coupled together, effectively canceling the distortion in the output signal. The RF output signal is fed to the output of the board at J10. A sample of the output signal is obtained using a microstrip coupler. The sample is applied to an RMS detector IC (U11) which provides a DC voltage proportional to the RF output level.

A voltage regulator IC (U8) is used to provide +5VDC to the RMS detector.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Bandpass Filter Assembly

The Bandpass Filter Assembly consist of a Bandpass Filter Module and Bandpass Filter Control Board. The Band Pass Filter Assembly provides filtering of the RF output signal as well as the capability to switch between the main RF input from the Power Amplifier Assembly or the auxiliary RF input from the Back-up Power Amplifier Assembly.

The main and auxiliary RF inputs enter the bandpass filter module at J2 and J1 respectfully and are applied to RF switch SW1. The unselected input is terminated into a 50 Ohm load. The selected signal is fed to a six pole bandpass filter (2500-2686 MHz), which passes the desired signal while attenuating unwanted harmonics and spurious frequencies, then to the RF output port J3. Two -20 dB directional couplers are used to obtain forward and reflective power samples of the RF signal. The forward sample is split into two signals. One signal is connected to the Reflected Sample port J7. The other signal is applied to a forward power measuring circuit consisting of an RMS detector (U1) and Hitite switch (U3). Any reflected power from antenna mismatch is diverted by a circulator to the Reflected Power Sample Port J6 and to a reflected power measuring circuit which consist of a Log detector (U2).

A serial programmable Atmel microcontroller located on the Bandpass Filter Control Board controls the RF switch via two MOSFET switches (Q20 and Q21). Relay status signals as well as the forward and reflected power levels from the power detectors are monitored by the microcontroller. The Bandpass Filter Control Board also provides forward and reflected power level calibration adjustments with on board potentiometers (R67 and R76).

Upstream/Downstream Switch Assembly

The Upstream/Downstream Switch Assembly consist of a Dual SP4T RF Switch Board and Upstream/Downstream Control Board (1125362). The Upstream/Downstream Switch Assembly functions as part of the back-up system in determining which of the four main RF inputs from the four Multiplexer Assemblies is routed to the Back-up Upconverter Assembly.

The four input signals from the Multiplexer Assemblies are applied to the Dual SP4T RF Switch Board at J2 (J2-22B, J2-25B, J2-28B, and J2-31B) and fed to the inputs of a SP4T RF switch (U2). The position of the switch is determined by the logic levels present on pins 9 and 10 of U1 (Control A and Control B). These control lines are driven by a serial programmable Atmel microcontroller located on the Upstream/Downstream Switch Control Board. The microprocessor receives the command for the proper switch setting from the Automatic Back-up System (ABS) Assembly which is also part of the back-up system. Switch setting may also be set through serial commands (J2-20B and J2-20C) from the SCADA (supervisory control and data acquisition) program. A front panel LED (labeled Back-up Enabled) located on the front panel of the assembly indicates that a back-up has been activated.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Downstream Controller Assembly

The Downstream Controller Assembly is comprised of a single circuit board – the Downstream Controller Board (1132140). The Downstream Controller Board provides monitoring and control of the transmitter and functions as an integral part of the system user interface (see System Monitoring Assembly) and automatic back-up system (see Automatic Back-up System Assembly).

The Downstream Controller Board consist of an 16-bit microcontroller (MC68HC705B16CFN) and associated control circuitry. The microcontroller monitors the operating status of the various assemblies of the transmitter. Critical faults for a particular assembly are reported by way of an interlock line.

The interlock signal from the Upconverter Assembly enters the board at J1-17A. The Upconverter interlock signal indicates the presence of one or more of the following faults: loss of input signal, +12 volt source too low, +9 volt source too low, -5 volt source too high, ALC voltage too high, PLL unlocked.

The interlock signal from the Power Amplifier Assembly enters the board at J1-1A. The Power Amplifier interlock signal indicates the presence of one or more of the following faults: device not installed, supply voltage below +10 volts, power supply faulted, output status faulted, over temperature.

The interlock signal from the Bandpass Filter Assembly enters the board at J1-1B. The Bandpass Filter interlock signal indicates the device is not installed or the supply voltage is below +10 volts.

After receiving an interlock fault, the Downstream Controller Board sends a Downstream Controller interlock (J1-7B) fault to the Automatic Back-up System (see Automatic Back-up System Assembly) which controls the back-up operation. The ABS then sends a back-up command on J1-27 instructing the Downstream Controller to place the Power Amplifier Assembly into standby and a second instruction to switch the Bandpass Filter Assembly to the Alternate position. The Downstream Controller board then sends a command (J1-23B) to the Back-up Downstream Controller which causes the back-up transmitter to go into the operate mode.

Back-up Upconverter Assembly

The Back-up Upconverter Assembly works as part of the back-up system and serves as a back-up upconverter should on of the four main upconverters fail. The output of the Upstream/Downstream switch Assembly provides the input to the Back-up Upconverter. The Back-up Upconverter Assembly is identical in design and function to the main Upconverter Assembly described above.

Back-up Power Amplifier Assembly

The Back-up Power Amplifier Assembly functions as part of the back-up system and serves as a back-up amplifier should on of the four main amplifiers fail. The output of the Back-up Upconverter Assembly provides the input to the Back-up Power Amplifier. The Back-up Power Amplifier Assembly is identical in design and function to the main Power Amplifier Assembly described above.

Downstream Transfer Switch Assembly

The Downstream Transfer Switch Assembly consist of a SP4T RF Transfer Switch, Downstream Transfer Switch Control Board (1121614) and Front Panel LED Board (1113710). The Downstream Transfer Switch Assembly functions as part of the back-up system by routing the output of the Back-up Power Amplifier to one of the four Bandpass Filter Assemblies.

The input signal from the Back-up Power Amplifier Assembly enters at J90 of the Bandpass Filter Chassis and is routed to the RF input of the SP4T RF switch. The switch position is selected by a serial programmable Atmel microcontroller, located on the Downstream Transfer Switch Control Board, which drives one of four FET switches (Q2, Q4, Q6, and Q8) which in turn energizes the appropriate coil in the RF switch. The microprocessor receives the command for the proper switch setting from the Automatic Back-up System (ABS) Assembly which is also part of the back-up system. The Front Panel LED Board located on the front panel of the assembly indicates current switch position. The output of the Downstream Transfer Switch Assembly is routed to the Bandpass Filter Assembly auxiliary input of the failed Sector.

Automatic Back-up System Assembly

The ABS Assembly is composed of a ABS Controller Board (1132142). The ABS Controller functions as part of the back-up system by monitoring the operating status of the four main transmitters and controlling the back-up process in the event of a fault.

The ABS Controller Board interfaces with the backplane using a 96 position connector (J1) then with external modules through three ribbon cable connections (J14, J16 and J22 of Control Module Backplane Board (1119953)). The ABS Controller Board consist of an 16-bit microcontroller (MC68HC705B16CFN) and associated control circuitry. The microcontroller monitors interlock lines from each of the Down Stream Controller Assemblies. The interlock line signals the presence of a critical transmitter fault. Upon receiving an interlock fault, the ABS begins the back-up process as described below.

Once the interlock fault is received by the microcontroller the micro will first check the priority level of the faulted sector. Priority level is fixed according to physical chassis location (left to right = highest to lowest priority). If no other transmitter sectors are currently being backed up the ABS will back up the faulted sector regardless of priority. However, if another sector is currently being backed up by ABS, the faulted sector will only be backed up if its priority is higher than the channel being backed up. Next the ABS will check the Load Enable signal from the Power Supply Assemblies. By monitoring this signal, the ABS can determine if the appropriate number of Power Supply Assemblies are installed and functioning before performing the back-up. Next, the ABS checks the Interlock signal of the Back-up Downstream Controller Assembly to insure no faults are present in the back-up transmitter.

The ABS then sends a standby command to both the faulted transmitter and back-up transmitter. After standby is verified, the ABS then sends control signals to place the Downstream Switch and Downstream Transfer Switch into proper switch position. The ABS then instructs the faulted transmitter to place the input switch in the Bandpass Filter assembly into the ABS position. Finally, an instruction is sent to place the back-up transmitter into operate.

System Monitoring Assembly

The System Monitoring Assembly is composed of a Front Panel LED Board (113713), LCD Display Board, Switch Board (1527-3406) and LCD Backplane Interface Board (1116295). The System Monitoring Assembly provides the user interface for the system with a front panel LCD display and push button switches.

The LCD Backplane Interface Board operates as the interface between the LCD Display Board, Switch Board and the chassis backplane (Control Module Backplane Board). Any one of the five Downstream Controller Boards in the system may write to the data bus that drives the LCD, but only one may write at any one time. To take control of the buss, the Downstream Controller Board will send a LCD buffer enable signal to a digital latch IC (pin 11 of U6). The digital latch IC will then send a confirmation data signal back to the controller indicating that it now has control of the buss. Five analog switch IC's (U1 through U5) operate in a de-multiplexer configuration by allowing only the Downstream Controller Board that is currently controlling the bus to write the LCD control signals (LCD Enable, R/W , Data or Instruction) to the LCD display. LED driver circuits (Q12 through Q21) are used to drive the LED's on the Front Panel LED board.

The Front panel LED Board indicates operating status of each of the four main transmitter sectors as well as the back-up transmitter. Green indicates no faults are present. Red indicates that a fault is present in that sector.

Power Supply Assembly

The Power Supply Assembly is composed of a 400W switching power supply (Astec MP4/2L/1L), 1200W Power Factor Corrected AC/DC converter Board (1112214) and Front Panel LED Board (1113710). The Power Supply Assembly provides the DC power to the BTS 1.0 system.

The Power Supply Assembly is designed to work in a redundant N+1 = 2+1 configuration. The chassis accepts up to three Power Supply Assemblies. Two supplies are required to supply system power for a fully loaded system. The third supply functions as a back-up supply operating in hot standby.

The AC input to the assembly is applied to a terminal block (TB2) which distributes the AC input to the two power supplies that make up the assembly.

The 400 W Switching Power Supply provides both a +12VDC output and a –12VDC output . Both outputs are fed to Oring diodes on the 100W PFC Board (TB2-1 and TB2-4) then to the output connector (J1) on the rear of the assembly. Voltage sense signals are fed back to the supply to compensate for any voltage drop across the diode (V1-1 and 4, V2-1 and 4).

The+12VDC and –12VDC output signals of the assembly are wired to terminal blocks in the rear of the Power Amplifier/Power Supply chassis that serve to combine the output signals from the three Power Supply Assemblies and also distribute the +12VDC and –12VDC to the system.

The 1200W PFC AC/DC Converter Board provides a +380VDC output which provides power to the Power Amplifier Assemblies. The AC input enters the board at J1 and is applied to AC line filters then to the input of an Astec APA100-101 PFC module. This module is capable of providing 1200W at +380VDC. The module output is fed to Oring diodes then to the output of the board at TB3. Operating status of the module is indicated through the Power Failure Warning (PFW) control signal which is reported to system control through transistor pull down (Q3) and to the Front Panel LED Board through transistor pull up (Q5 and Q6). Operating status of the 400 W Switching Supply is indicated through the DC OK signal which is applied to the board at J4 and is then routed to pull up/pull down circuits (Q8, Q9 and Q10) similar in function to those described above. Soon after application of AC input module will output a Load Enable signal indicating that the output has stabilized. This signal is also provided to system control through transistor (Q2) pull down.

The Front Panel LED Board provides visual operating status indication of both the 400W Switching Supply and 1200 W PFC module.

10 MHz Frequency Reference Assembly

The 10 MHz Frequency Reference Assembly consist of 10 MHz Reference Board (1136560), GPS Receiver (TrueTime model 87-664), 10 MHz Reference Generator Board (1519-3126) and Front Panel LED Board (1113710). The function of the 10 MHz Frequency Reference Assembly is to select one of three possible 10 MHz reference sources (external, GPS, or internal) and distribute the signal.

The GPS Receiver Input, External 10 MHz Reference Input and Internal 10 MHz Reference Input are applied to the 10 MHz Reference Board input jacks (J1, J2 and J8A-1A respectfully) Diode detector circuits are used to detect the presence of each of the three inputs. A serial programmable Atmel microcontroller monitors the signals from the detector circuits and selects the proper reference based on order of priority (external reference first, GPS reference second and internal reference third) by energizing the coil of latching relay K1 or K2. The selected reference signal is then amplified and split to provide 4 reference signals. The four reference signals are fed to the Control Module Backplane Board (1119948) output connectors (J10 through J13) before being distributed throughout the system.

There internal reference is provided by the 10 MHz Reference Generator Board (1519-3126). The 10 MHz Reference Generator Board uses a temperature oven controlled 40 MHz VCXO. The crystal frequency is divided down to 10 MHz by divider IC U4. Crystal tuning adjustments are provided by tuning capacitors (C2 and C3). Oven temperature control is provided by an on board potentiometer (R15).

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

The GPS reference is provided by a GPS receiver manufactured by TrueTime Inc (Model 87-664). The TrueTime GPS is capable of tracking up to six satellites and has an acquisition time of less than 2 minutes, frequency output accuracy less than 3×10^{-12}.

The Front Panel LED Board (1113713) provides LED status indication of each of the three reference sources (selected/not selected, present/not present, present but faulted) as well as lock indication of the GPS source.

2.0 TECHNICAL DESCRIPTION

2.5 Alignment Procedure

In the following procedure, the complete transmitter is adjusted for optimum performance, beginning with the start up procedure of the QAM modulator, followed by the QAM agile upconverter, then the digital transmitter, starting at the base band input and adjusting each circuit for its specified performance while observing the appropriate output parameters of the board or subassembly being adjusted.

Because of the broadband nature of most of the amplifier stages, this is a straightforward procedure, easily accomplished if base band, IF, and RF test equipment is available. In this procedure, the input signals are first connected and each circuit is adjusted in sequence by connecting the test equipment to the specified point.

Equipment Needed

Spectrum Analyzer
RF Power Meter
30 dB Directional Coupler
10 dB Directional Coupler
Volt Meter
50Ω Load

Adjust the spectrum analyzer for the following settings:

1. Resolution BW = 30 KHz
2. Video Averaging (ON)
3. Span = 20 MHz
4. Video Bandwidth = 30 kHz
5. Center Frequency = 44 MHz

The average power of a modulated QAM digital signal, with the specified analyzer settings, is +23dB higher than the displayed signal. The measurements in this alignment procedure will be given in average levels.

Example: Analyzer reading of –30 dBm
Average power = -30 dBm + 23 dBm = - 7 dBm.

2.0 TECHNICAL DESCRIPTION

2.5 Alignment Procedure - continued

WMTS (QAM MODULATOR TRAY)

Follow the steps listed in Sections 2.2.1 and 2.2.2 of Exhibit III to bring the WMTS modulator online.

The test described in the above sections involve a bi-directional “ping” test between a CPE (customer premise equipment) PC and the NMS (network management system) via the WMTS. Once this test is completed the front panel LED indicators on the WMTS are checked for proper operation.

This completes the set-up of the WMTS unit.

2.0 TECHNICAL DESCRIPTION

2.5 Alignment Procedure - continued

AGILE UPCONVERTER TRAY

Follow the steps listed below to bring the MA4040D Agile Upconverter online.

1. Turn on the tray by connecting the AC power cable to the power module and observing the front panel LEDs. The upconverter modules are configured using the LCD display and push buttons on the front panel of the power module.

2. Verify that the green power LED is illuminated on the front panel of the upconverter module. The power LED indicates that the module is installed correctly and that power is present.

3. Using the front panel push buttons, select the upconverter module that will be used for the test. The green Module Select LED will illuminate when selected.

4. Confirm that the Alarm LED is not illuminated. If illuminated check module and status codes on LCD. (Note: check manual for status code definitions)

5. Set the output frequency of the upconverter for channel A1 (222.00 MHz).

6. Set Auto IF to Enabled.

7. Using the front panel buttons select RF Pwr.

8. Using the arrow keys adjust the RF Pwr to approximately 55dBmv.

9. Using the front panel buttons select Output Enabled.

At this point the MA4040D Agile upconverter has been powered up and the output spectrum may be observed.

Using a spectrum analyzer verify the proper shape and center frequency (44 MHz) of the spectrum at the IF output port (J5). Verify that the power level corresponds to that set in step 7 above.

The upconverter circuitry requires no user adjustments.

2.0 TECHNICAL DESCRIPTION

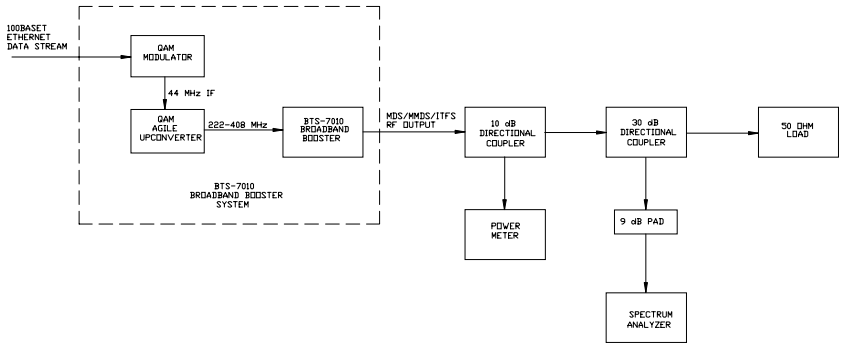
2.5 Alignment Procedure - continued

BTS-7010 BROADBAND BOOSTER

The various modules which make up the BTS-7010 set up at the factory for optimum performance using specially designed test fixtures. The internal circuits require no user adjustments and therefore this alignment procedure is presented on a system level.

1. Connect the output of the Agile Upconverter to the Sector #1 input (J231) on the rear of the Upper/Lower Signal Processing Chassis (note: this input is fed to the input of the Multiplexer Assembly).

2. Connect the RF output of the transmitter, J201 on the Band Pass Filter Chassis, to a spectrum analyzer and RF power meter using a directional couplers and suitable 50 Ohm load as shown below.



3. Connect AC power cord to AC input jack J220 on the rear of the Power Amplifier/Power Supply Chassis.

4. Place AC circuit breaker CB1 located on rear of Power Amplifier/Power Supply into the ON position.

5. Verify that the front panel power supply status LED's (±12VDC Switching Supply and +380VDC PFC Power Supply) are green (no fault).

6. Using the front panel push buttons located font panel of the System Monitoring Assembly, place Sector 1 transmitter into the Operate mode.

7. Connect external 10 MHz reference to J9 located on rear of Control Assembly chassis.

8. Verify that External Source Reference LED is illuminated on front panel of 10 MHz Reference Assembly.

2.0 TECHNICAL DESCRIPTION

2.5 Alignment Procedure - continued

9. Place switch SW1, located on the front panel of the Upconverter Assembly into the ALC1 position (note: ALC1 potentiometer adjust IF level into mixer).

10. Adjust front panel ALC1 potentiometer until both the Low Input and High Input LED's are green.

11. Place switch SW2, located on front panel of the Upconverter Assembly into the ALC2 position (note: ALC2 potentiometer adjust the RF output level).

12. Adjust front panel ALC2 potentiometer for rated output power as observed on the RF Power Meter.

13. Verify both inband and out-of-band performance of transmitter on spectrum analyzer (see specifications).

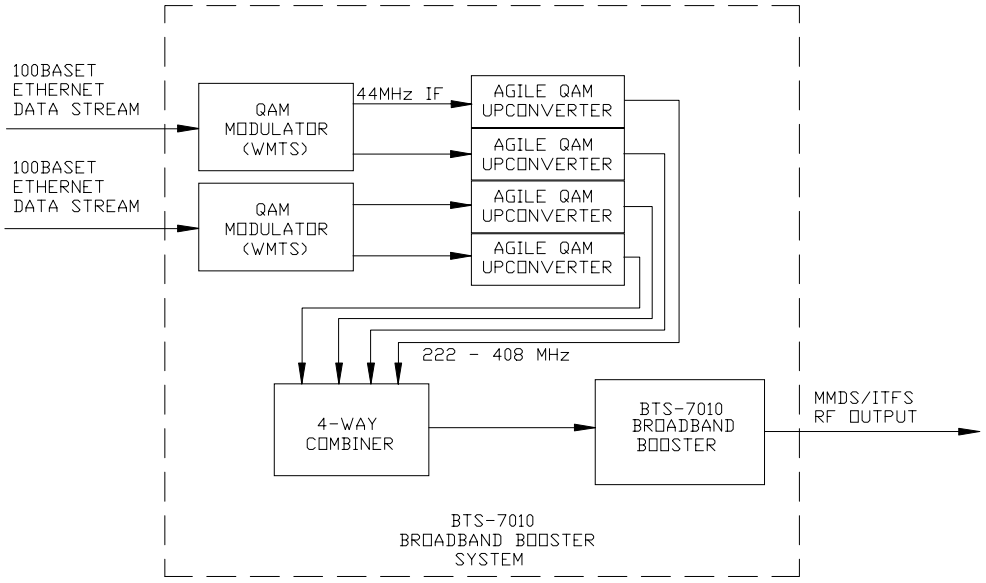
This completes the alignment/setup of the unit.

2.0 TECHNICAL DESCRIPTION

2.6 Block Diagrams

The following is a system block diagram for the BTS-7010 Broadband Booster. Detailed block diagrams and schematics are included in Exhibit II (BTS-7010 Broadband Booster).

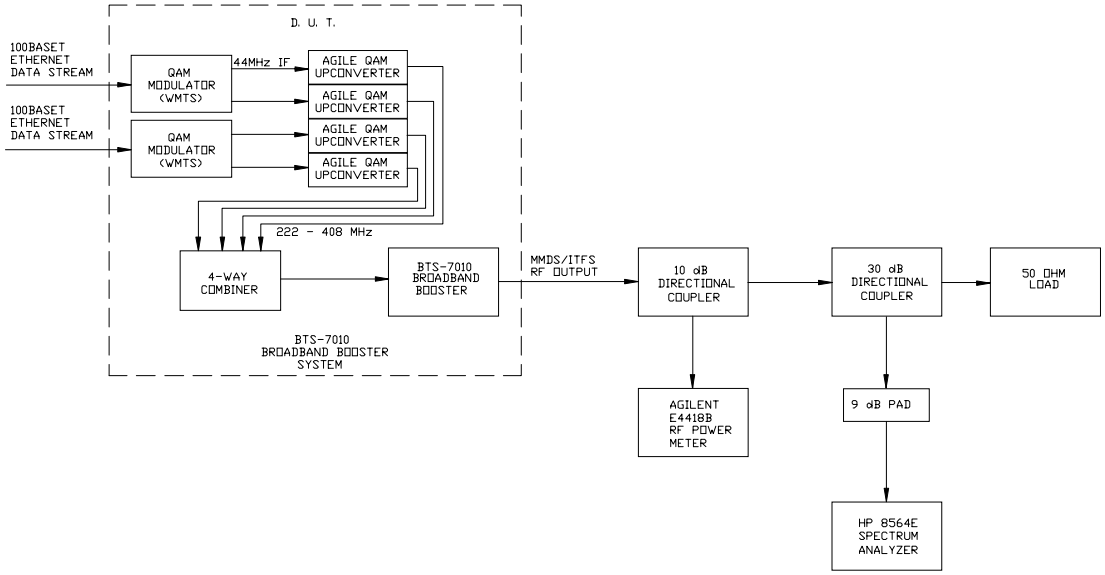
System Block Diagram:



3.0 ENGINEERING DATA

3.1 RF Power Measurements

The following block diagram illustrates the test equipment set-up for the following measurement:



Using the test set-up above, with four input signals present, the output power of the BTS-7010 was adjusted to the rated output power of 5.0 watts total average as observed on the power meter.

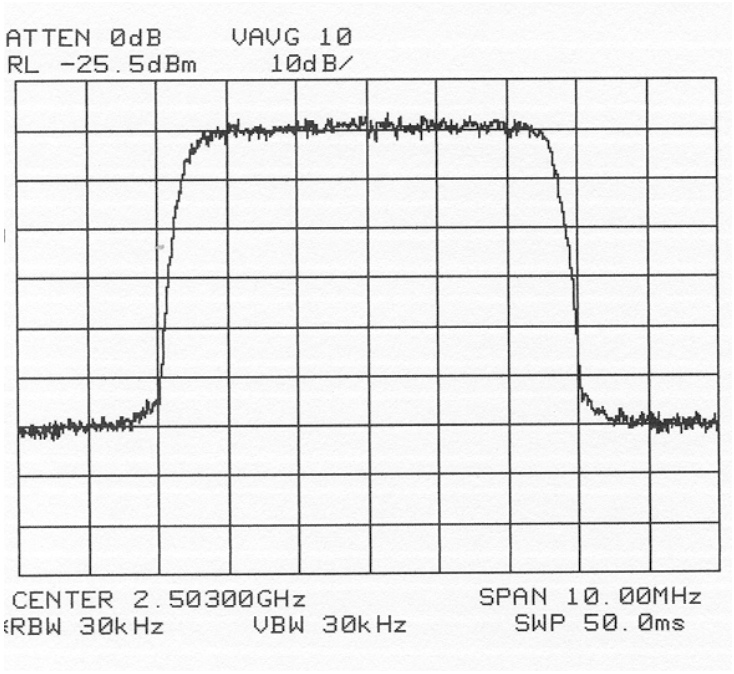
With the power level properly set to 5.0 watts (total average), all required test were performed and recorded in the following sections.

3.0 ENGINEERING DATA

3.2 Occupied Bandwidth

Using the test set-up shown in Section 3.1 above, with the booster operating at rated output power and with four input signals (A1, A3, G2 and G4).present, the analyzer was set to a span of 10 MHz and a reference level was established on the analyzer (see plot below). Then the analyzer was adjusted to a span of 190 MHz and the occupied bandwidth (2500.00 MHz – 2690.00 MHz) was observed and recorded below.

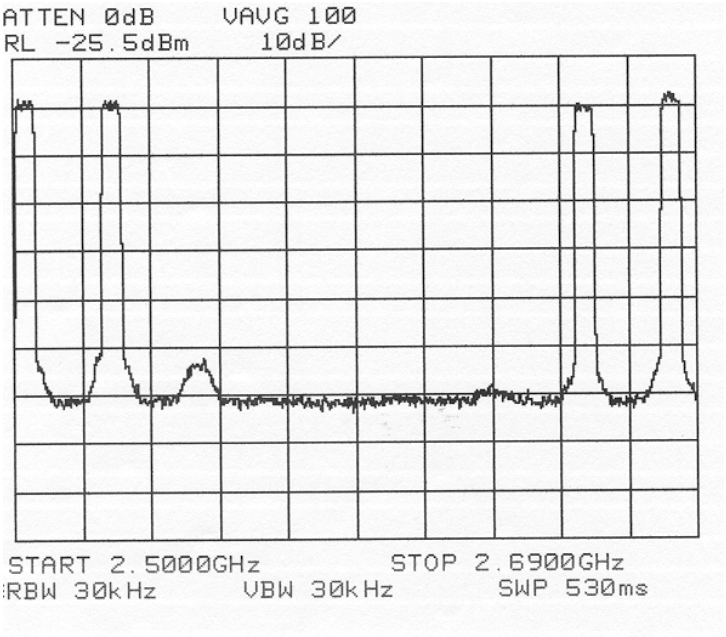
Reference Level Plot/10 MHz Span (5.0 Watts total average):



3.0 ENGINEERING DATA

3.2 Occupied Bandwidth

Occupied Bandwidth Plot/190 MHz Span (5.0 Watts total average)



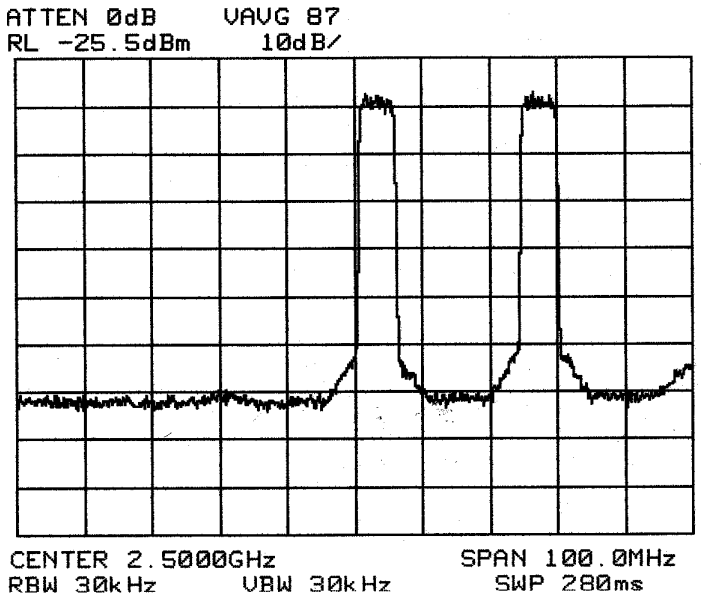
3.0 ENGINEERING DATA

3.3 Out-of-Band Power

Using the test set-up shown in Section 3.1 above, with the output power adjusted to 5.0 watts total average, the spectrum outside of the specified channel was observed and the data was taken on all products above the -65 dB noise floor of the spectrum analyzer. The spectral points were measured at the same resolution bandwidth used to establish the reference level on the analyzer. With the average in-band signal set as the reference, the spurious emissions were observed and recorded.

Spurious Emissions were observed on the analyzer using several different channel arrangements selected to represent worse case operating conditions in terms of measuring out-of-band emissions. The first measurement was performed with two channels placed at the lower band edge (A1 and A3), 24 MHz separation, and two channels placed at the upper band edge (G2 and G4) with 24 MHz separation. The second measurement was performed with four non-adjacent channels placed at the lower band edge (A1, A2, A3, and A4). The third and final measurement was performed with four non-adjacent channels placed at the upper band edge (G1, G2, G3, and G4).

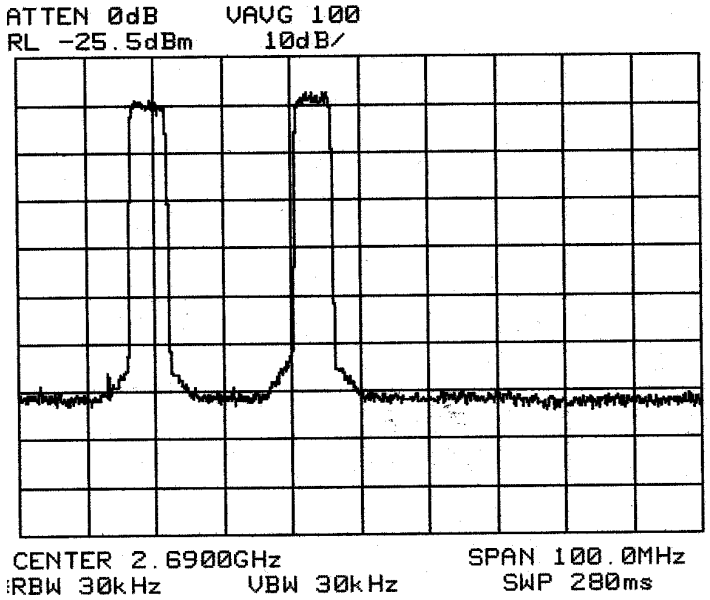
Spectrum Analyzer Plot (showing lower band edge)/Four Channels Present (A1, A3, G2 and G4):



3.0 ENGINEERING DATA

3.3 Out-of-Band Power - continued

Spectrum Analyzer Plot (showing upper band edge)/Four Channels Present (A1, A3, G2 and G4):

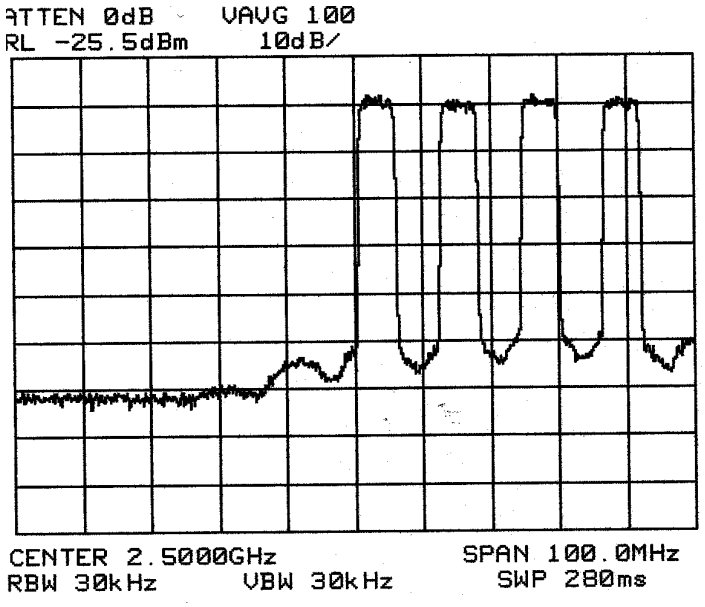


Frequency	Source	Level Observed
2503.00 MHz	center of channel (A1)	0 dB (Reference)
44.00 MHz	IF	-65.0 dB
2500.00 MHz	lower band edge	-50.3 dB
2499.75 MHz	-250.0 KHz below band edge	-51.6 dB
2497.00 MHz	-3.0 MHz below band edge	-58.6 dB
2480.00 MHz	-20.0 MHz below band edge	-61.5 dB
2690.00 MHz	upper band edge	-62.3 dB
2690.25 MHz	+250.0 KHz above band edge	-63.0 dB
2693.00 MHz	+3.0 MHz above band edge	-63.0 dB
2710.00 MHz	+20.0 MHz above band edge	-63.3 dB
5000 - 5380 MHz	2nd Harmonic frequencies	-65.0 dB (max)
7500 - -8070 MHz	3rd Harmonic frequencies	-65.0 dB (max)
10000 – 10760 MHz	4th Harmonic frequencies	-65.0 dB (max)
12500 – 13450 MHz	5th Harmonic frequencies	-65.0 dB (max)
15000 – 16140 MHz	6th Harmonic frequencies	-65.0 dB (max)
17500 – 18830 MHz	7th Harmonic frequencies	-65.0 dB (max)
20000 – 21520 MHz	8th Harmonic frequencies	-65.0 dB (max)
22500 – 24210 MHz	9th Harmonic frequencies	-65.0 dB (max)
25000 – 26900 MHz	10th Harmonic frequencies	-65.0 dB (max)

3.0 ENGINEERING DATA

3.3 Out-of-Band Power - continued

Spectrum Analyzer Plot (showing lower band edge)/Four Channels Present (A1, A2, A3 and A4):

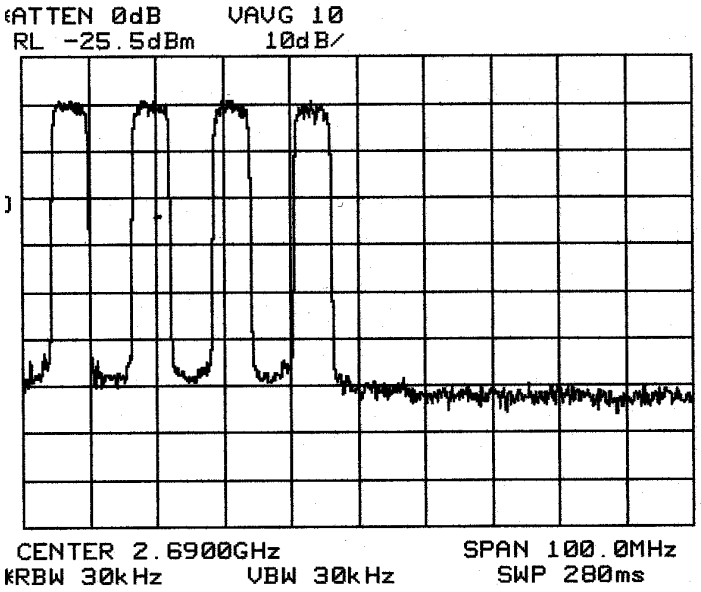


Frequency	Source	Level Observed
2503.00 MHz	center of channel (A1)	0 dB (Reference)
44.00 MHz	IF	-65.0 dB
2500.00 MHz	lower band edge	-53.5 dB
2499.75 MHz	-250.0 KHz below band edge	-53.5 dB
2497.00 MHz	-3.0 MHz below band edge	-58.3 dB
2480.00 MHz	-20.0 MHz below band edge	-61.8 dB
2690.00 MHz	upper band edge	-62.3 dB
2690.25 MHz	+250.0 KHz above band edge	-62.3 dB
2693.00 MHz	+3.0 MHz above band edge	-62.3 dB
2710.00 MHz	+20.0 MHz above band edge	-63.0 dB
5000 - 5380 MHz	2nd Harmonic frequencies	-65.0 dB (max)
7500 - -8070 MHz	3rd Harmonic frequencies	-65.0 dB (max)
10000 – 10760 MHz	4th Harmonic frequencies	-65.0 dB (max)
12500 – 13450 MHz	5th Harmonic frequencies	-65.0 dB (max)
15000 – 16140 MHz	6th Harmonic frequencies	-65.0 dB (max)
17500 – 18830 MHz	7th Harmonic frequencies	-65.0 dB (max)
20000 – 21520 MHz	8th Harmonic frequencies	-65.0 dB (max)
22500 – 24210 MHz	9th Harmonic frequencies	-65.0 dB (max)
25000 – 26900 MHz	10th Harmonic frequencies	-65.0 dB (max)

3.0 ENGINEERING DATA

3.3 Out-of-Band Power - continued

Spectrum Analyzer Plot (showing upper band edge)/Four Channels Present (G1, G2, G3 and G4):



Frequency	Source	Level Observed
2683.00 MHz	center of channel (G4)	0 dB (Reference)
44.00 MHz	IF	-65.0 dB
2500.00 MHz	lower band edge	-63.1 dB
2499.75 MHz	-250.0 KHz below band edge	-63.1 dB
2497.00 MHz	-3.0 MHz below band edge	-64.5 dB
2480.00 MHz	-20.0 MHz below band edge	-64.5 dB
2690.00 MHz	upper band edge	-59.5 dB
2690.25 MHz	+250.0 KHz above band edge	-59.5 dB
2693.00 MHz	+3.0 MHz above band edge	-61.0 dB
2710.00 MHz	+20.0 MHz above band edge	-61.7 dB
5000 - 5380 MHz	2nd Harmonic frequencies	-65.0 dB (max)
7500 - -8070 MHz	3rd Harmonic frequencies	-65.0 dB (max)
10000 – 10760 MHz	4th Harmonic frequencies	-65.0 dB (max)
12500 – 13450 MHz	5th Harmonic frequencies	-65.0 dB (max)
15000 – 16140 MHz	6th Harmonic frequencies	-65.0 dB (max)
17500 – 18830 MHz	7th Harmonic frequencies	-65.0 dB (max)
20000 – 21520 MHz	8th Harmonic frequencies	-65.0 dB (max)
22500 – 24210 MHz	9th Harmonic frequencies	-65.0 dB (max)
25000 – 26900 MHz	10th Harmonic frequencies	-65.0 dB (max)

3.0 ENGINEERING DATA

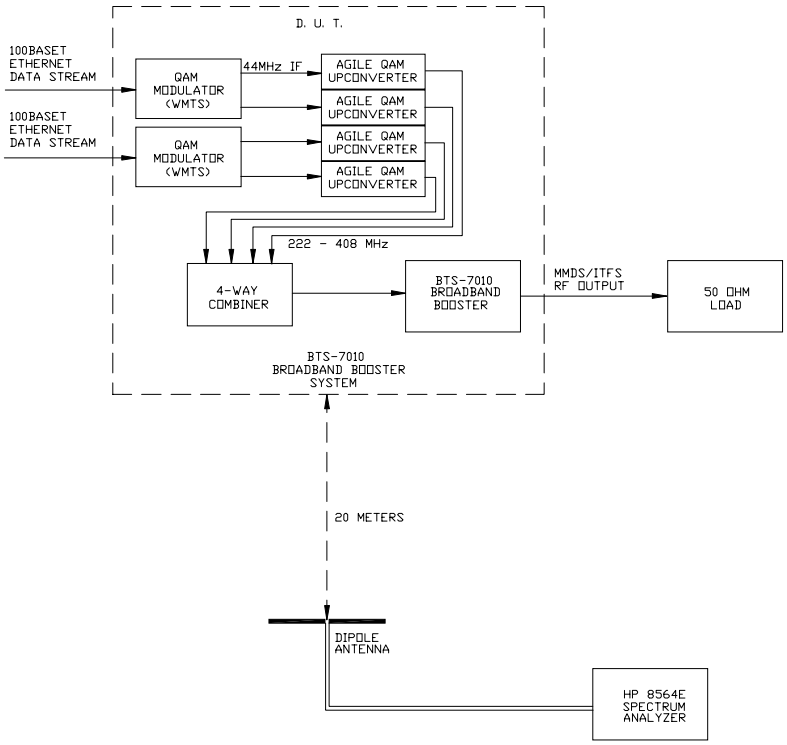
3.4 Radiated Emissions

Using the test set-up below, with four input signals present (A1, A3, G2, and G4) and operating at 5.0 watts (total average), the spectrum analyzer was moved 20 meters from the transmitter and connected to a dipole antenna cut to the carrier frequency of A1 (2503 MHz). This antenna was oriented to maximize the received level, and the data was recorded. The antenna was then cut to the remaining channel frequencies and the receive level was observed on the spectrum analyzer. The antenna was then cut to the IF frequency, and the second through the tenth harmonic frequencies and all signals received were maximized by antenna orientation, and their absolute levels were recorded.

With these various antennas the data was taken and recorded in the table on the following page.

Note: The spectrum analyzer had a maximum sensitivity of -100 dBm during this test.

Test Set-up:



3.0 ENGINEERING DATA

3.4 Radiated Emissions - continued

MEASURED LEVELS

Frequency	Source	Level Observed
44.00 MHz	IF	None Observed
2500 – 2690 MHz	operating band	-75 dB
5000 – 5380 MHz	2nd harmonic frequencies	None Observed
7500 – 8070 MHz	3rd harmonic frequencies	None Observed
10000 – 10760 MHz	4th harmonic frequencies	None Observed
12500 - 13450 MHz	5th harmonic frequencies	None Observed
15000 – 16140 MHz	6th harmonic frequencies	None Observed
17500 - 18830 MHz	7th harmonic frequencies	None Observed
20000 - 21520 MHz	8th harmonic frequencies	None Observed
22500 - 24210 MHz	9th harmonic frequencies	None Observed
25000 - 26900 MHz	10th harmonic frequencies	None Observed

3.0 ENGINEERING DATA

3.4 Radiated Emissions - continued

The measured levels were then compared to the following reference level:

If all of the transmitter's power (5.0 Watts) was radiated by an isotropic radiator, the power density at 20 meters would be:

$Pd = Pt/4\pi R^2 = 5.0/4\pi (20)^2 \cong 0.9947x10^{-3}$ w/m^2

Using a dipole transmitting antenna increases this by 1.64 to:

3.5 * $0.99474x10^{-3} = 1.6313 x10^{-3}$ w/m^2

If a dipole receive antenna of area $1.64 * \lambda^2/4\pi$ is used to receive the signal, the received level would be:

$1.6313 x10^{-3} * 1.64 * \lambda^2/4\pi = 2.689 x10^{-6}$w = - 55.7 dBw = -25.7 dBm

The receive levels were therefore at the following relative levels:

Frequency	Relative Measured Level (Ref = -25.7 dBm)
2509.00 MHz	**-49.3 dBc**

3.0 ENGINEERING DATA

3.5 Frequency Stability

TheBTS-7010 is designed to operate using either an internal 10MHz reference or external 10 MHz precise reference oscillator. The frequency stability of this reference source determines the frequency stability of the transmitter.

The frequency determining variables of the transmitter may be defined as follows:

F_{LO} = Desired local oscillator frequency
F_{IF} = Desired IF oscillator frequency
F_R = Desired external reference oscillator frequency
F_{RF} = Desired RF output frequency
E_{LO} = Local oscillator frequency offset error
E_{IF} = IF oscillator frequency offset error
E_R = External reference oscillator frequency offset error
E_{RF} = RF output frequency error

The PLL circuitry maintains a constant ratio between the external reference frequency and the output frequency of the oscillator. This ratio is defined below for both the LO and IF oscillators.

$G_{LO} = F_{LO}/F_R$
$G_{IF} = F_{IF}/F_R$

Any change in the external 10 MHz reference will effect a corresponding change in the output frequency such that the above ratios are maintained.

$G_{LO} = (F_{LO} + E_{LO})/(F_R + E_R) = F_{LO}/F_R$

$G_{IF} = (F_{IF} + F_{IF})/(F_R + E_R) = F_{IF}/F_R$

Solving for the change in output frequency yields:

$E_{LO} = E_R * (F_{LO}/F_R) = E_R * G_{LO}$

$E_{IF} = E_R * (F_{IF}/F_R) = E_R * G_{IF}$

The desired RF carrier frequency is equal to the LO frequency minus the IF frequency:

$F_{RF} = F_{LO} - F_{IF}$

The actual RF frequency, including any error introduced by the external reference, may be defined as follows:

$F_{RF} + E_{RF} = (F_{LO} + E_{LO}) - (F_{IF} + E_{IF})$
$F_{RF} + E_{RF} = (F_{LO} + F_{IF}) - (E_{LO} - E_{IF})$
$F_{RF} + E_{RF} = F_{RF} + (E_{LO} - E_{IF})$

3.0 ENGINEERING DATA

3.5 Frequency Stability - continued

Calculating for the error of the RF carrier yields:

$E_{RF} = (E_{LO} - E_{IF})$
$E_{RF} = E_R * G_{LO} - E_R * G_{IF}$
$E_{RF} = E_R (G_{LO} - G_{IF})$
$E_{RF} = E_R/F_R * (F_{LO} - F_{IF})$
$E_{RF} = E_R/F_R * F_{RF}$

Therefore, the error of the RF carrier is a function of the internal/external 10 MHz reference error.

The maximum RF frequency error for this service is ±1.0 kHz. The highest channel frequency for this service (G4 = 2683.00 MHz) represents the worst case condition. With these values the maximum allowable reference error ($E_{R(max)}$) can be calculated.

$E_{R(max)} = (E_{RF} * F_R) / F_{RF}$
$E_{R(max)} = 3.73$ Hz

The 10 MHz reference oscillator was placed in a Thermotron temperature test chamber, and the temperature was varied from -30°C to +50°C. The frequency of the oscillator was measured at 10°C increments up to +50°C. The oscillator output frequency was allowed a reasonable amount of time to stabilize at each temperature increment. As indicated in the following table, the reference oscillator showed a maximum error of 1.2 Hz over the stated temperature range.

OSCILLATOR TEMPERATURE STABILITY DATA

TEMP. (°C)	10.00 MHz Reference Oscillator	Reference Oscillator Error (E_R)	Output Frequency Error ($E_{RF} = E_R/F_R * F_{RF}$)
-30	10.0000012 MHz	1.2 Hz	322.0 Hz
-20	10.0000010 MHz	1.0 Hz	268.3 Hz
-10	10.0000008 MHz	0.8 Hz	214.6
0	10.0000005 MHz	0.5 Hz	134.2
+10	10.0000000 MHz	0.0 Hz	0.0
+20	10.0000000 MHz	0.0 Hz	0.0
+30	10.0000004 MHz	0.4 Hz	107.3
+40	10.0000001 MHz	0.1 Hz	26.8
+50	10.0000007 MHz	0.7 Hz	187.8

FREQUENCY STABILITY VS. LINE VOLTAGE

Line Voltage (VAC at 60 Hz)	10.00 MHz Reference Oscillator	Reference Oscillator Error (E_R)	Output Frequency Error ($E_{RF} = E_R/F_R * F_{RF}$)
95V	10.0000012 MHz	0.0 Hz	0.0 Hz
115V	10.0000010 MHz	0.0 Hz	0.0 Hz
135V	10.0000008 MHz	0.0 Hz	0.0 Hz

3.0 ENGINEERING DATA

3.5 Frequency Stability - continued

The 10 MHz Reference Assembly also provides an optional GPS precise reference
The required reference oscillator stability may be calculated as follows:

Stability = $E_{R(max)}/F_R$
Stability = 3.73 Hz/10 x 10^6 Hz = 0.373 x 10^{-6}

Therefore, the RF frequency error of the BTS 1.0 will not exceed $\pm$1.0 KHz when operated with a precise reference oscillator with a stability equal to or better than 0.373 x 10^{-6}.

Commercially available GPS precise reference oscillators, such as the TRAK Systems 8821 which has a frequency stability of 1 x 10^{-11} over a temperature range of -10 to 50 °C, and a line voltage/frequency range from 85 to 265 VRMS/48 to 440 Hz (see TRAK Systems 8821 specifications on the following pages), insure a frequency stability within the tolerance specified in the Rules and Regulations for this service.

TRAK SYSTEMS DIVISION OF TRAK MICROWAVE

GPS Clock

Model 8821A (1-3/4") and B (3-1/2")

- **Accurate Time and Frequency with Just One Satellite**
- **Parallel Tracking of Six Satellites**
- **Oscillator Disciplined to GPS**
- **Choice of Oscillator Options**
- **5 MHz, 10 MHz, 1.544 MHz, or 2.048 MHz Outputs**
- **PC Software Disk for Setup and Output**
- **1 PPS Output Sync Within 1 Microsecond of GPS**
- **IRIG B Modulated and DC Output Options**
- **Form - C Relay and TTL Status Outputs**
- **Dual RS-232 Ports**
- **85 - 265 Vac or 100 - 370 Vdc Operation (24 or 48 Vdc Optional)**

The Model 8821 GPS Clock is a reduced-cost version of TRAK Systems' extremely successful Model 8812 and 8820 GPS Station Clocks. This versatile unit incorporates a six-channel parallel GPS receiver, a disciplined crystal oscillator, and a precise time and frequency generator in a single assembly. Phase offset of the 1 PPS output, referenced to UTC, is typically less than one microsecond when one or more satellites are being tracked.

The unit operates from 85 - 265 Vrms, 48-440 Hz or 100-370 Vdc, voltage ranging is automatic. No strapping or switchover is required. Optional power inputs include 24 Vdc and 48 Vdc.

The Model 8821 incorporates automatic oscillator calibration by GPS, automatic leap second correction and built-in calendar for automatic leap year updates. By using the remote setup feature, the operator may set up for automatic daylight savings time corrections. These features, a very high MTBF, and an RS-232 remote status monitoring feature virtually eliminate the need for site visits for setup, calibration, and maintenance.

The unit is supplied with a monitor and control application program for DOS-based computers. Program is normally supplied on a 3-½ inch floppy disk.

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MODEL 8821 SPECIFICATIONS

Internal Oscillator Options

E4A (Standard Model 8821A OCXO)

Accuracy while Tracking: (one-hour averaging)	<1 X 10^{-11}
Aging rate when coasting*:	<5 X 10^{-9}/day
1 PPS coasting drift*: (first 8 hours)	<6 µs/hour
Phase noise @ 10 Hz offset	<-100 dBc
Phase noise @ 100 Hz offset	<-130 dBc
Phase noise @ 1 KHz offset	<-135 dBc
Phase noise @ 10 KHz offset	<-140 dBc
Harmonic distortion	<-40 dBc
Non-Hormonic distortion	<-100 dBc

B7A (Standard Model 8821B OCXO)

Accuracy while Tracking: (one-hour averaging)	<1 X 10^{-11}
Aging rate when coasting*:	<5 X 10^{-10}/day
1 PPS coasting drift*: (first 8 hours)	<500 ns/hour
Phase noise @ 10 Hz offset	<-105 dBc
Phase noise @ 100 Hz offset	<-125 dBc
Phase noise @ 1 KHz offset	<-140 dBc
Phase noise @ 10 KHz offset	<-145 dBc
Harmonic distortion	<-30 dBc
Non-Hormonic distortion	<-100 dBc

Other Frequencies

Option B7 also available for output of 1.544 MHz, 2.048 MHz, or 5 MHz from the Model8821B.

Synchronization

The position of the antenna is determined by measuring the pseudo-range to four satellites and computing the position of these satellites using ephemeris data.

*Coasting factors apply only if there has been an antenna or receiver failure or if antenna is blocked from view of all satellites.

The receiver basic specifications are as follows:

Receiver Description:	L1 C/A code pseudo-ranging
Channels:	Six independent, continuous tracking channels
Frequency:	1575.42 MHz
Acquisition Time:	Typically less than two minutes

Navigation Outputs

Latitude, longitude, and height with a position accuracy of ± 30 meters, 2 drms (without SA) are available on the RS-232 ports.

Tracking Modes

In its default tracking mode, the Model 8821 automatically tracks one to six satellites, as available, on a stationary platform.

Two other modes, one for use on a moving platform and the other for use with an operator-entered fixed position, can be selected.

Timekeeping

The Model 8821 normally accumulates Universal Time (UTC). By command, this may be changed to local time. When local time is used, automatic daylight savings time adjustments are made at preprogrammed dates. Leap second and leap year adjustments are made automatically. Time is available on the RS-232 ports with a resolution of one millisecond.

Optional IRIG B Output**

Format:	Modulated IRIG B 122
Level:	3 Vpp nominal
Drive:	Will drive 50 ohms
Mod. Ratio:	Adjustable 2:1 to 6:1
Phase:	Modulated code on-time mark adjustable to within ± 10 microseconds of on-time reference.

** Rate and IRIG B outputs are a single option. Not available separately

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Optional Rate/DC Code Output**

Frequency: One of the following may be selected: 1 PPH, 6 PPH, 12 PPH, 1 PPM, or 1 PPS - 1 MPPS in decade steps. IRIG B DC may be output in place of a selected rate.

Levels: TTL

Drive: 50 ohms

Coherence: Within one microsecond of UTC

Connector: BNC

1 PPS Output

Levels: TTL

Pulsewidth: 100 microseconds

Drive: 50 ohms

Coherence: Within one microsecond of UTC

Connector: BNC

High Rate Output (Sinewave)

Frequency: Same as internal oscillator (10 MHz standard, others optional)

Level: 1 Vrms ± 10%

Drive: 50 ohms

Coherence: Phase coherent to 1 PPS

Connector: BNC

Optional Output Frequencies

Other available frequency outputs (Model 8821B only) include 5 MHz, 1.544 MHz, and 2.048 MHz.

Optional TTL Rate Output

TTL levels on High Rate Output in place of sinewave. Drive is 50 ohms.

Status Output

Three contacts of a Form-C relay provide tracking status output on a 9-pin connector. Contact rating is 1/2 amp. Also on this connector is status at TTL logic levels.

Remote Setup and Status

The following is a partial list of setup and status commands via the RS-232 Port.

Set/Request UTC/LOCAL
Set/Request local time offset
Set/Request daylight savings dates
Set/Request output rate
Set/Request local position
Set/Request minimum tracking elevation
Request time output
Request navigation data
Request tracking/locked status
Request time offset data
Request leap second status
Request satellites being tracked
Request firmware version

Time/Status Display (option)

The unit can be ordered with an LED display of time and status.

Power Supply

The unit operates on 85-265 Vrms, 48-440 Hz, or 100-370 Vdc. Power required is 25 watts nominal. Options available for 24 or 48 Vdc in place of ac.

Internal Battery

An internal lithium battery maintains GPS module stored data and coarse timekeeping during time that no external power is applied.

Physical

Model 8821A chassis is 19" wide X 1.72" high X 9" deep. Model 8821B chassis is 3.47 inches high. Weight is 9 pounds.

Antenna unit is 4.25 inches in diameter X 6.5 inches high. Weight is 7 ounces. It is connected to the main chassis via a coaxial cable. A 50 foot cable with TNC connectors is supplied. Optional lead-in systems with coaxial cables and in-line amplifiers are available to 2500 feet. Refer to application note AN-3A for complete details.

Temperature

Main unit: -10 to + 50° C
Antenna: -40 to + 70° C

See Page 2 for notes.

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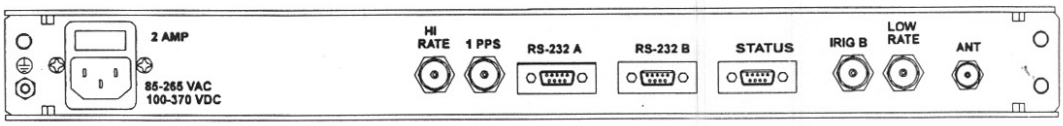
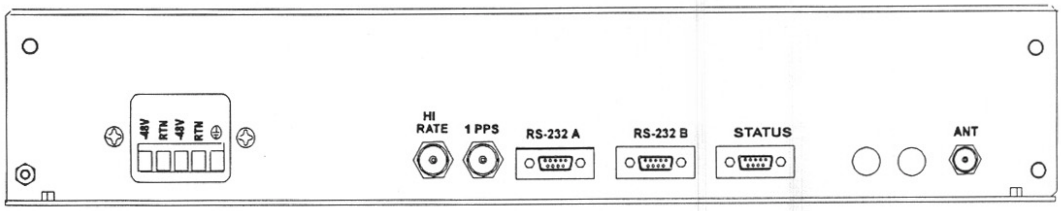
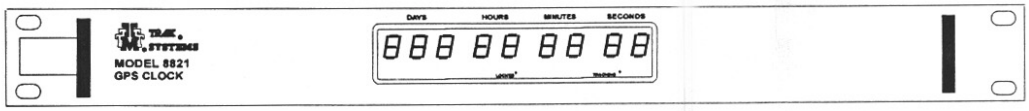
Typical Views



Model 8821A Rear Panel (with Code/Low Rate Option)



Model 8821B Rear Panel (with 48 Vdc Power Option)



Model 8821A with Display Option

Specification subject to change without notice.

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3.0 ENGINEERING DATA

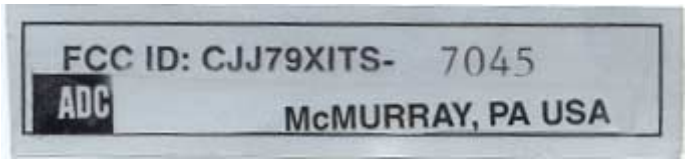
3.6 Test Equipment

MODEL	MANUFACTURER	DESCRIPTION	SERIAL #
8564E	Hewlett Packard	Spect. Analyzer 9 KHz-40 GHz	Rental
8595E	Hewlett Packard	Spect. Analyzer 9 kHz- 6.5GHz	3543A01613
3003-30	Narda	30 dB Directional Coupler	779
3003-10	Narda	10 dB Directional Coupler	09049
E4418B	Agilent	RF Power Meter	GB39513814
E Series	Hewlett Packard	30 Watt Power Head	E9301B
1992	Racal-Dana	Frequency Counter	950304
8135	Bird	50 Ohm Termination	8520
79	Fluke	Digital Multimeter	56660032
SM-27	Thermotron	Temperature Test Chamber	31290

4.0 IDENTIFICATION LABELS/LABEL PLACEMENT AND PHOTOGRAPHS

4.1 FCC Identification Label:

Note: The following Identification Labels and Label Placement Drawings can also be found in the Exhibit V attachment.

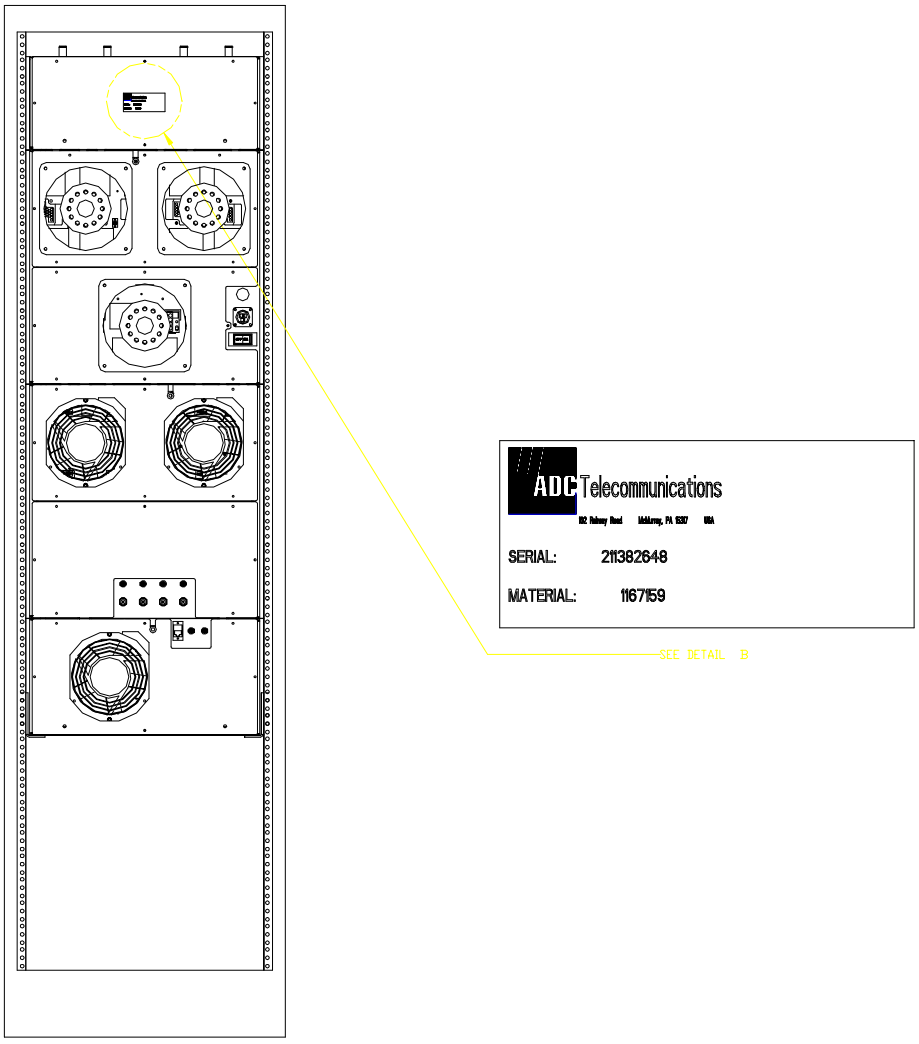


4.2 Manufacturer's Identification Label:

4.0 IDENTIFICATION LABELS/LABEL PLACEMENT AND PHOTOGRAPHS

4.3 Label Placement Drawings

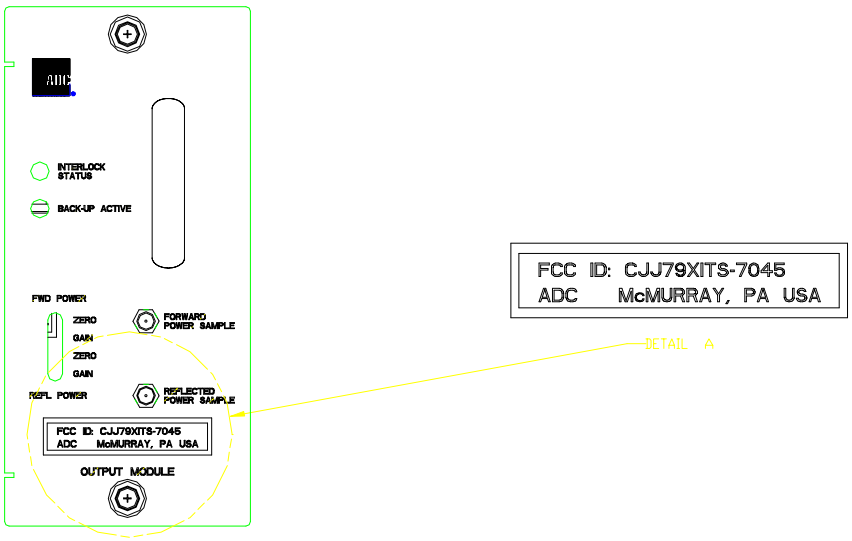
Manufacturer Identification Label Placement Drawing (rear panel – Band Pass Filter Chassis):



4.0 IDENTIFICATION LABELS/LABEL PLACEMENT AND PHOTOGRAPHS

4.3 Label Placement Drawings- continued

FCC Identification Label Placement Drawing (fronts panel – Bandpass Filter Module)



4.0 IDENTIFICATION LABELS/LABEL PLACEMENT AND PHOTOGRAPHS

4.4 Photograph List

External Photos:

Note: The following external photos can be found in the Exhibit VI attachment:

4.4.1 Front view, Complete BTS-7010 Broadband Booster System .

4.4.2 Rear view, Complete BTS-7010 Broadband Booster System .

4.4.3 Front view, Band Pass Filter Chassis

4.4.4 Rear view, Band Pass Filter Chassis

4.4.5 Front view, Power Amplifier/Power Supply Chassis

4.4.6 Rear view, Power Amplifier/Power Supply Chassis

4.4.7 Front view, Upper/Lower Signal Processing Chassis

4.4.8 Rear view, Upper/Lower Signal Processing Chassis

4.4.9 Front view, Control Chassis

4.4.10 Rear view, Control Chassis

Internal Photos:

Note: The following internal photos can be found in the Exhibit VII attachment:

4.4.11 Inside view (sled assembly), Band Pass Filter Module

4.4.12 Inside view (sled assembly), Downstream Output Switch Module

4.4.13 Inside view (sled assembly), Power Amplifier Module

4.4.14 Inside view (sled assembly), Power Supply Module

4.4.15 Inside view (sled assembly), Upconverter Module

4.4.16 Inside view (sled assembly), Upstream/Downstream Output Switch Module

4.4.17 Inside view (sled assembly), Downstream Controller Module

4.4.18 Inside view (sled assembly), 10 MHz Reference Module

4.4.19 Inside view (sled assembly), System Monitoring Module

5.0 CERTIFICATION OF TEST DATA

This equipment has been tested in accordance with the requirements contained in the appropriate Commission regulation. To the best of my knowledge, these tests were performed using measurement procedures consistent with industry or Commission standards and demonstrate that the equipment complies with the appropriate standards. Each unit manufactured, imported or marketed, as defined in the Commission's regulations, will conform to the sample(s) tested within the variations that can be expected due to quantity production and testing on a statistical basis. I further certify that the necessary measurements were made by ADC Telecommunications, 102 Road, McMurray, Pennsylvania 15317.

David Urban 8/21/01

Dave Urban, Chief Engineer

Todd Anderson 8/21/01

Todd Anderson, Engineer