ADC
TELECOMMUNICATIONS

EXHIBIT VIII

SCHEMATICS Part 2 of 2
BTS-7010

IF SECTION

MIXER SECTION

RF SECTION

J4 OSP
−14 ~+16 DBM
222 − 408 MHz

A

−1 DB
BPF
222 − 408 MHz

−1 DB

+13 DB

−6 ~ −36 DBM
IF PIN ATTENUATOR

+13 DB

−1 DB
BPF
222 − 408 MHz

−2 DB

B
−5 DBM
222 − 408 MHz

IF ALC VOLT

−20 DB

−3 DB

−2 DB

IF
RF
LO

−3 DB

−2 DB
BPF
2500 − 2686 MHz

C
−22 DBM
2500 − 2686 MHz

2278 TRAP

−15.5 DB
−15.5 DB
−15.5 DB
−15.5 DB

−16 ~ −6 DB
RF PIN ATTENUATOR

−20 DB

−3 DB

D
−0 DBM
2500 − 2686 MHz

J20 OSP

−3 DB

−20 DB

−3 DB

LO SAMPLE

+18 DB
+18 DB

RF ALC VOLT.

RF SAMPLE

+12V
−12V

POWER DISTRIBUTION CIRCUITRY

IF AUTOMATIC LEVEL CONTROL

IF LEVEL

IF DETECTOR

RF AUTOMATIC LEVEL CONTROL

IF ALC REF. ADJ.
IF MANUAL GAIN ADJ
ALC MODE 1

INNER LOOP MON
INEER LOOP ALC
OUTER LOOP AMP
OUTER LOOP MON

RF DETECTION SIGNAL CIRCUIT

RF LEVEL

RF LEVEL
ALC VOLTAGE
ALC VOLTAGE
MUTE CONTROL
ALC MODE 2
RF ALC REFERENCE ADJ.
RF MANUAL GAIN ADJ.

ALC VOLTAGE

I/P LEVEL

J1

PLL FAULT
SS (1..6)
10MHz REFERENCE FAULT
INPUT FAULT
MUTE INDICATOR
MUTE COMMAND
ALC VOLTAGE
INTERLOCK
MAC
SCADA

MICRO CONTROLLER UNIT

ALC VOLTAGE
MUTE CONTROL
ALC MODE 2
IF ALC REFERENCE ADJ.
IF MANUAL GAIN ADJ.
ALC MODE 1
LED CONTROL LINES

G
LO SAMPLE SMA
−3 DBM, 2278MHz

F
RF SAMPLE SMA
−23 DBM, 2500−2686 MHz

ALC MODE 2

ALC MODE 1

RF MANUAL GAIN ADJ.

RF ALC REFERENCE ADJ.

IF ALC REFERENCE ADJ.

IF MANUAL GAIN ADJ.

MODULE FRONT PANEL CONTROLS

LO GENERATOR SECTION

VCXO HOLD OVER
VCXO VOLTAGE
REF. DETECT
PLL LOCK DET 1
PLL PROG LINES
PLL LOCK DET 2

+15 DB

10MHz REFERENCE

PLL FOR REFERENCE OSCILLATOR

PLL FOR LO OSCILLATOR

CRO VOLTAGE

CRO LO OSCILLATOR (2278 MHz)

.3 PF

+18 DB

CRO PHASE

−3 DB

REFERENCE OSCILLATOR SECTION

E
VCXO SAMPLE
1 DBM
94.91667 MHz

VCXO REFERENCE OSCILLATOR (94.91667 MHz)

VCXO VOLTAGE
VCXO PHASE

LOW I/P FAULT LED
HIGH I/P FAULT LED
MUTE FAULT LED
ALC FAULT LED
10 MHz FAULT LED
PLL FAULT LED

REV	ECO	DATE	APV

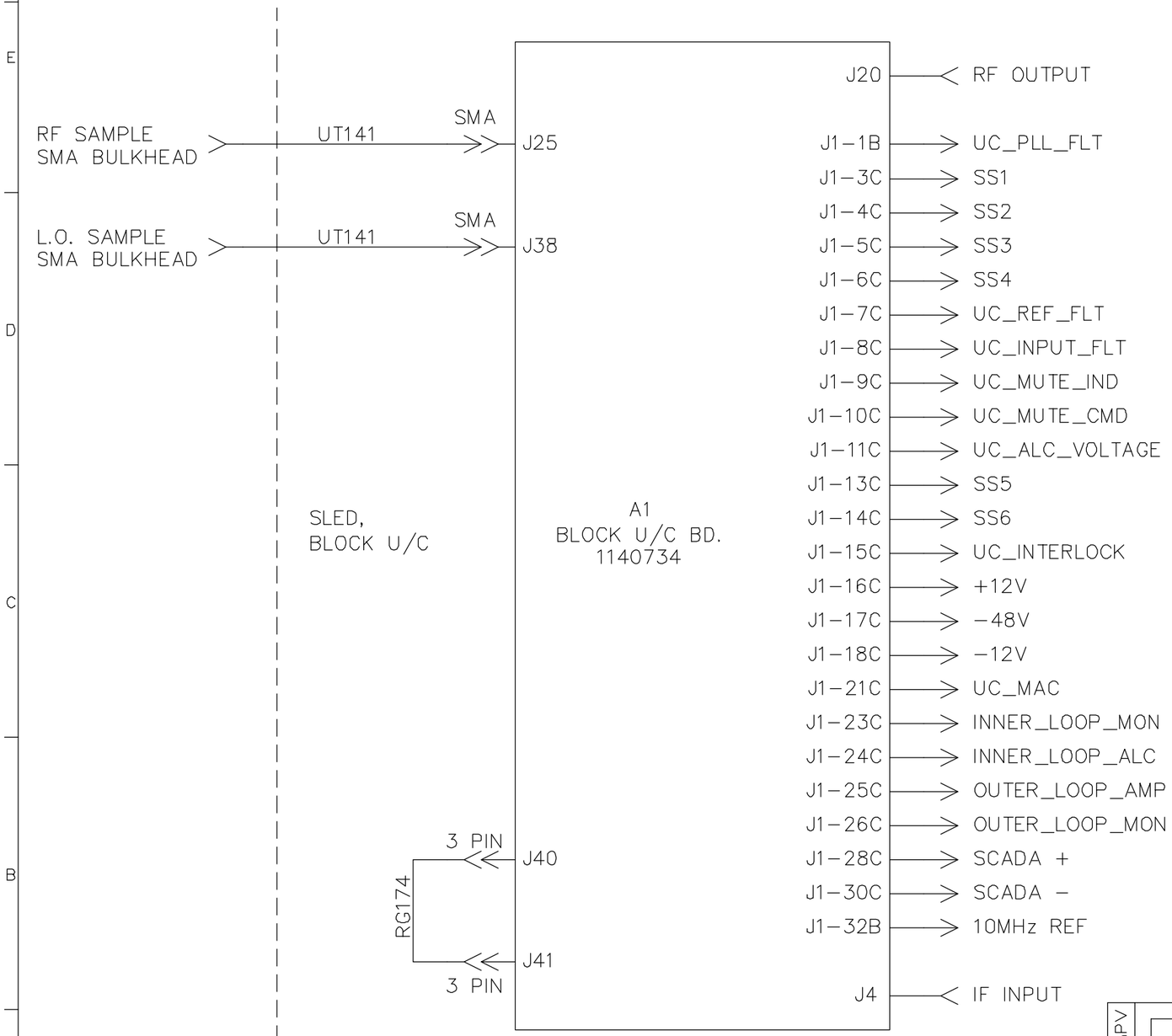
THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION.

MATERIAL
−−−−−

FINISH
−−−−−

TITLE
B/D, BLOCK U/C, V2, AXITY BTS

DWN	JKF	5/10/01	DWG. NO. 1175458 REV A0
CHK	BKW	5/15/01	
REL	BKW	5/15/01	D SCALE 1=1 SHEET 1 OF 1



REV	ECO	DATE	APV

REV ECO DATE APV

ADC

MATERIAL
−−−−−

FINISH
−−−−−

TITLE I/C, BLOCK U/C, 2.5 − 2.7 GHz, AXITY BTS

DWN	JKF	2/6/01	DWG. NO. 1152963	REV A0
CHK	BKW	2/21/01		
REL	BKW	2/21/01	B SCALE −−−	SHEET 1 OF 1

CIRCUIT DESCRIPTION: 1140734 AXITY BTS UPCONVERTER

The 1140734 Axity BTS Upconverter converts the down stream signal in the 222-408 MHz IF band to the 2500-2686 MHz RF band using an LO frequency of 2278MHz. The circuit primarily consists of four sections: IF, RF, LO generation, and control.

IF SECTION

The broad band IF input signal applied to J4 can range from +50 to +70 dBmV across the 222 to 408 MHz frequency band, and an Automatic Level Control (ALC) circuit automatically adjusts the IF level into a high IP3 mixer for optimal frequency conversion to the RF band. Bandpass filtering of the IF signal is also provided and fault detection of the IF signal level into the mixer is indicated through red illumination of the front panel LEDs, DS1 (LOW I/P FAULT) and DS2 (HIGH I/P FAULT). These faults can also be communicated to external modules by providing a low impedance on the rear connector at pin J1-8C. The detected level is also compared against an independent threshold level for determining if the input signal has been lost. In the event that the input signal has been lost the RF ALC circuit will become muted. The IF ALC circuit can be placed into the manual or automatic modes with the front panel switch SW1. Placing SW1 into the MANUAL 1 position and varying the potentiometer R29 on the front panel allows for manual adjustment of the gain through the IF stages leading into the mixer. The MANUAL 1 position also disables all muting features of the circuit, and manual operation is indicated by the amber illumination of LED DS3 (MUTE). Placing SW1 into the ALC1 position enables automatic control of the IF level into the mixer which can be set by varying the potentiometer R33 on the front panel.

RF SECTION

The broadband RF signal provided at J20 is the upper side band mixing product of the IF signal with the LO signal. Band pass filtering and amplification are performed on the RF signal to produce the desired result, and an ALC circuit automatically adjusts the RF level at J20 based on detected output levels from one or two stages of external amplification. The externally detected RF output level from the first stage of amplification is an analog voltage in the range of 0~5 volts and is applied to J1-24C. It is amplified and level adjusted with the potentiometer R59 to produce 1.8 volts at TP4 when the final amplifier output power is at 100%. Likewise, the externally detected RF output of the optional second stage of amplification is also an analog voltage in the range of 0~5 volts and is applied to J1-25C. It is amplified and level adjusted with potentiometer R48 to produce 2 volts at TP2 when the final amplifier output power is at 100%. Buffered outputs of the externally detected RF output levels of the first and second stages of amplification are provided on the rear connector at pins J1-23C and J1-26C respectively. The RF ALC circuit can be placed into the manual or automatic modes with the front panel switch SW2. Placing SW2 into the MANUAL 2 position and varying the potentiometer R52 on the front panel allows for manual adjustment of the gain through the RF stages. The MANUAL 2 position also disables all muting features of the circuit, and manual operation is indicated by the amber illumination of LED DS3 (MUTE). Placing SW2 into the ALC2 position enables automatic control of the RF levels detected from the external amplifier stages, and can be set by varying the potentiometer R40 on the front panel. A buffered output of the ALC control voltage is provided to external modules through the rear connector at pin J1-11C, and an ALC fault is indicated by the red illumination of LED DS4 (ALC FAULT). Muting of the RF output is performed under certain conditions. Muting from a loss of input can occur under the conditions previously described in the IF section. Muting can also occur by the communication of a mute condition from an external module through the interface connection J1-10C. Shorting this connection to ground potential will cause the RF output to become muted. The mute status will be indicated by the red illumination of the LED DS3 (MUTE) and is also communicated to external modules by providing a low impedance on the rear connector at pin J1-9C.

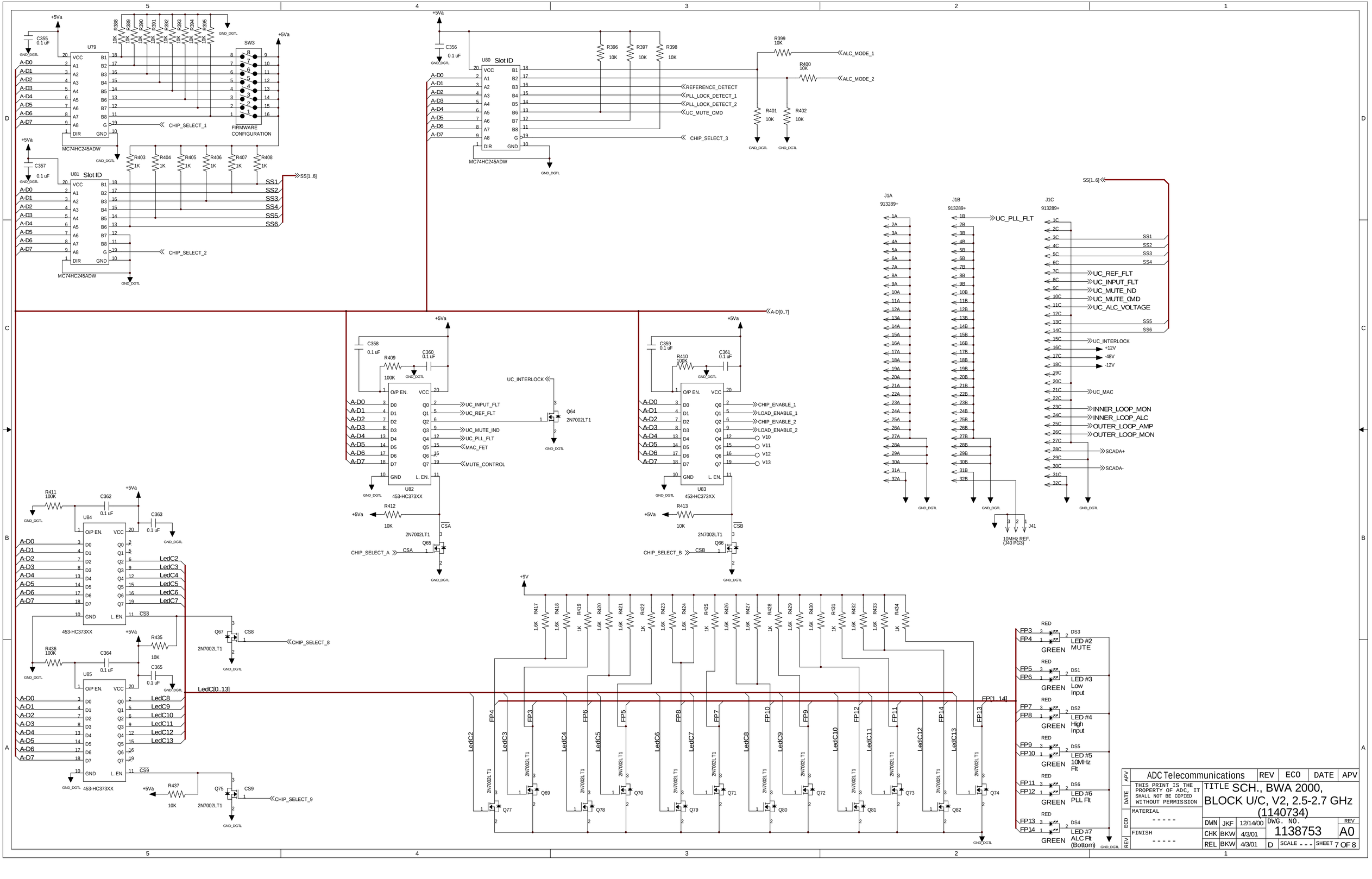
LO GENERATION

The 2278 MHz LO is generated in a two step process. In the first step, a digital phase frequency detector is used to phase lock a voltage controlled crystal oscillator (VCXO) to a 10 MHz reference signal supplied from an external source through the connection at J1-32B. When locked, the VCXO will produce a frequency of 94.916667 MHz. In the event the 10 MHz reference is lost, LED DS5 (10 MHZ) will be illuminated red, and a hold over circuit will keep the VCXO operating close to 94.916667 MHz. Communication of this event to external modules is also provided as a low impedance on the rear connector at pin J1-7C. In the second step, the output of the VCXO is used as the phase reference to a digital phase frequency detector which will phase lock the 2278 MHz LO output of a voltage controlled ceramic resonator oscillator (VCRO). The LO signal is then amplified, and applied to the mixer. In the event that the phase lock loop (PLL) circuits have gone out of lock, LED DS6 (PLL) will be illuminated red. Communication of this event to external modules is provided as a low impedance on the rear connector at pin J1-1B. If the 2278MHz oscillator is phase locked and the 94.916667MHz oscillator is operating from the hold over circuit, then LED DS6 (PLL) will be illuminated amber.

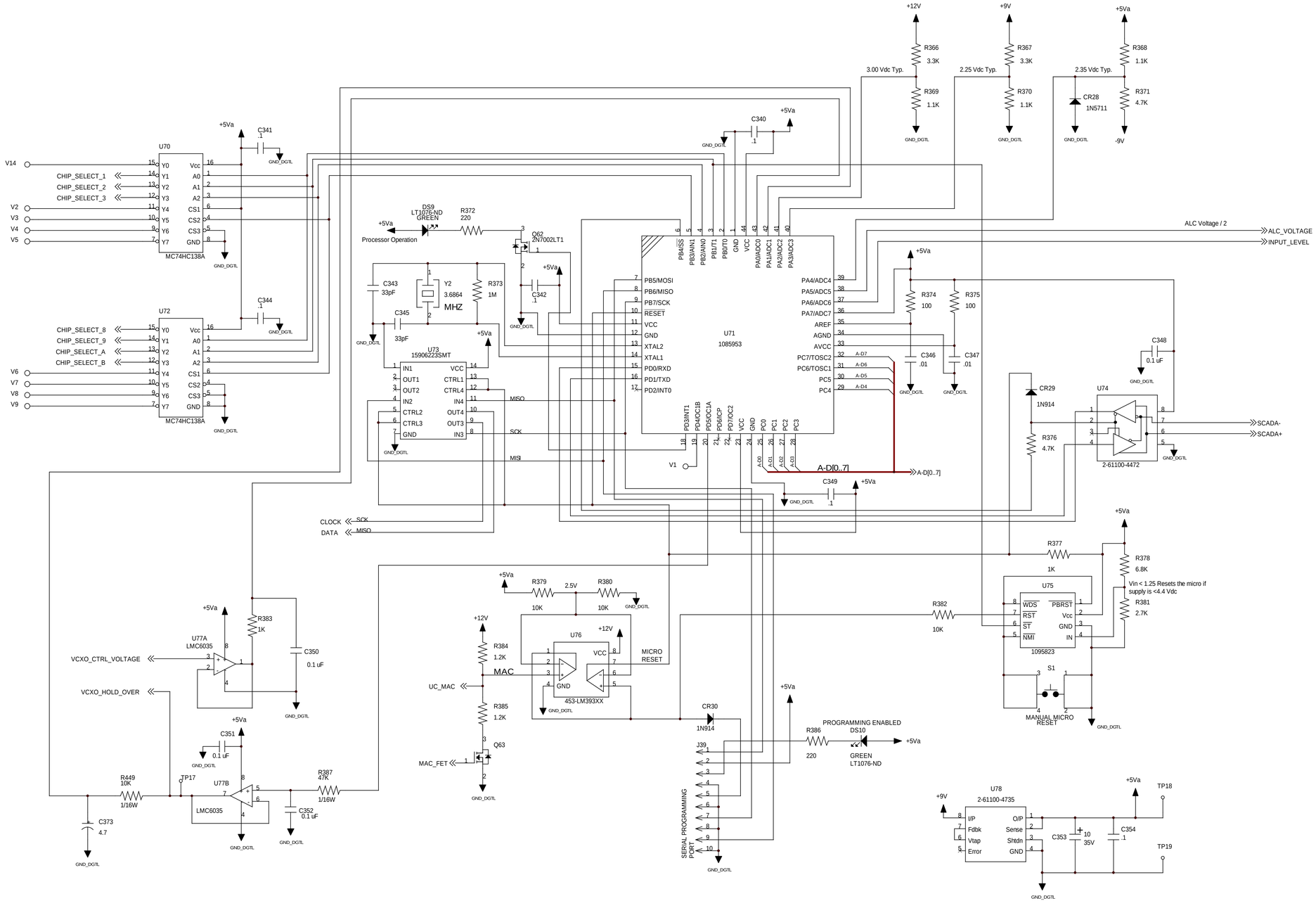
CONTROL

U70 and U72 are used for device select. These parts are used by the microcontroller (U71) to selectively communicate with U79, U81, U80, U84, U85, U82, and U83. U71 is the serial programmable Atmel microcontroller. The controller operates at 3.6864 MHz. The Micro Access and Control (MAC) line is used to indicate current device status. If this device is not installed or it is not powered, pin 21C of backplane connector J1 is about ground potential. If this device is installed and operating properly this control line is held at about +12 Vdc through a 1.2 Kohm resistor. If a fault needs to be reported, two 1.20 Kohm resistors are used to set the MAC line at about +6 Vdc. If the system controller needs to reset this device, it will hold the MAC line (pin 21C of J1) at about 0.0 Vdc. U75 is a watchdog timer IC that monitors PB1 of the micro. If the chip select address line does not change state after about 2 seconds, the reset line (pin 7) is sent low otherwise this line is held at +5 Vdc. J39 is the programming port used to install the micro's firmware. J39 pin 5 is used by the serial programmer to hold the microcontroller in reset. If J39 pin 5 is low or the watchdog reset line is low, or the MAC line is held low, the microcontroller is reset by pin 7 of U76. U74 is the serial RS-485 transceiver IC. Pin 2 is used for data direction. During a microcontroller reset, this part is set to receive mode. During normal operation, the microcontroller set this devices data flow direction. U73 is an analog switch used to disconnect the serial lines during programming of U71. U77B is used to provide an analog output signal to the circuitry of PLL #1. This signal must match the VCXO Control value whenever a 10 MHz source is present. If the 10 MHz source is removed, the output of U77B will be adjusted to make the VCXO Control value read the same value as when the external source was present. U78 is a precise low dropout SMT voltage regulator used to regulate the system +5 Vdc. U79 is used for digital input signals. This part is used to the firmware configuration DIP switch. This switch may be used to implement different features of the firmware. U81 is used for digital input signals. This part is used to read the slot ID pins of J1. The programming of the SS1-6 lines on the backplane board is used by the firmware to set the device SCADA address. U80 is used for digital input signals. This part is used to monitor system conditions such as ALC Mode Switch #1 & #2, the presence of a 10 MHz reference, the lock condition of PLL circuits, and a Mute command input signal from the backplane. U84 and U85 are used for digital output signals. These parts are used to control the front panel LEDs. Since green LEDs are expected to be normal, a FET is used to shunt current away from the LED when it is to be off. To reduce parts, the red LED is wired the same as the green LED except less current is used. U82 and U83 are used for digital output signals. U82 is used to set system outputs. U83 is used to set control lines for the serial PLL chips.

APV	ADC Telecommunications	REV	ECO	DATE	APV	
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH., BWA 2000, BLOCK U/C, V2, 2.5-2.7 GHz (1140734)				
ECO	MATERIAL -----	DWN	JKF	12/14/00	DWG. NO. 1138753	REV A0
REV	FINISH -----	CHK	BKW	4/3/01		
		REL	BKW	4/3/01	D	SCALE --- SHEET 8 OF 8



APV	ADC Telecommunications	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH., BWA 2000, BLOCK U/C, V2, 2.5-2.7 GHz (1140734)			
ECO	MATERIAL -----	DWN JKF 12/14/00	DWG. NO. 1138753		REV A0
REV	FINISH -----	CHK BKW 4/3/01			
		REL BKW 4/3/01	D	SCALE ---	SHEET 7 OF 8



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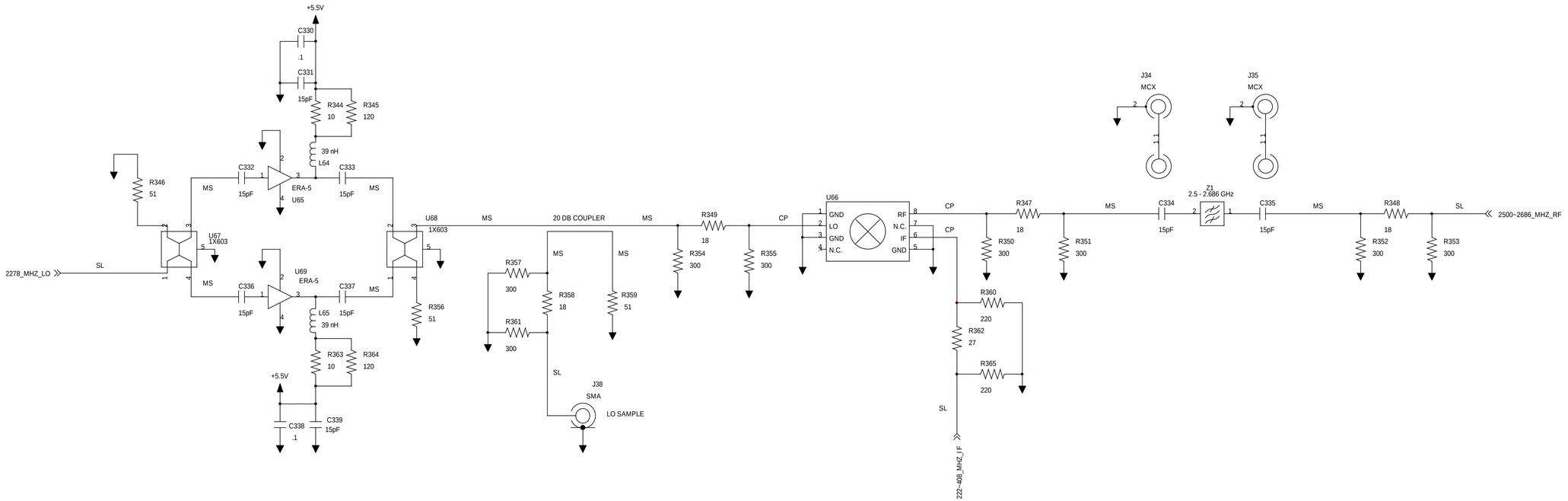
ECO	MATERIAL -----	DWN	JKF	12/14/00	DWG. NO. 1138753	REV A0
REV	FINISH -----	CHK	BKW	4/3/01		
		REL	BKW	4/3/01	D	SCALE - - - SHEET 6 OF 8



APV	ADC Telecommunications	REV	ECO	DATE	APV
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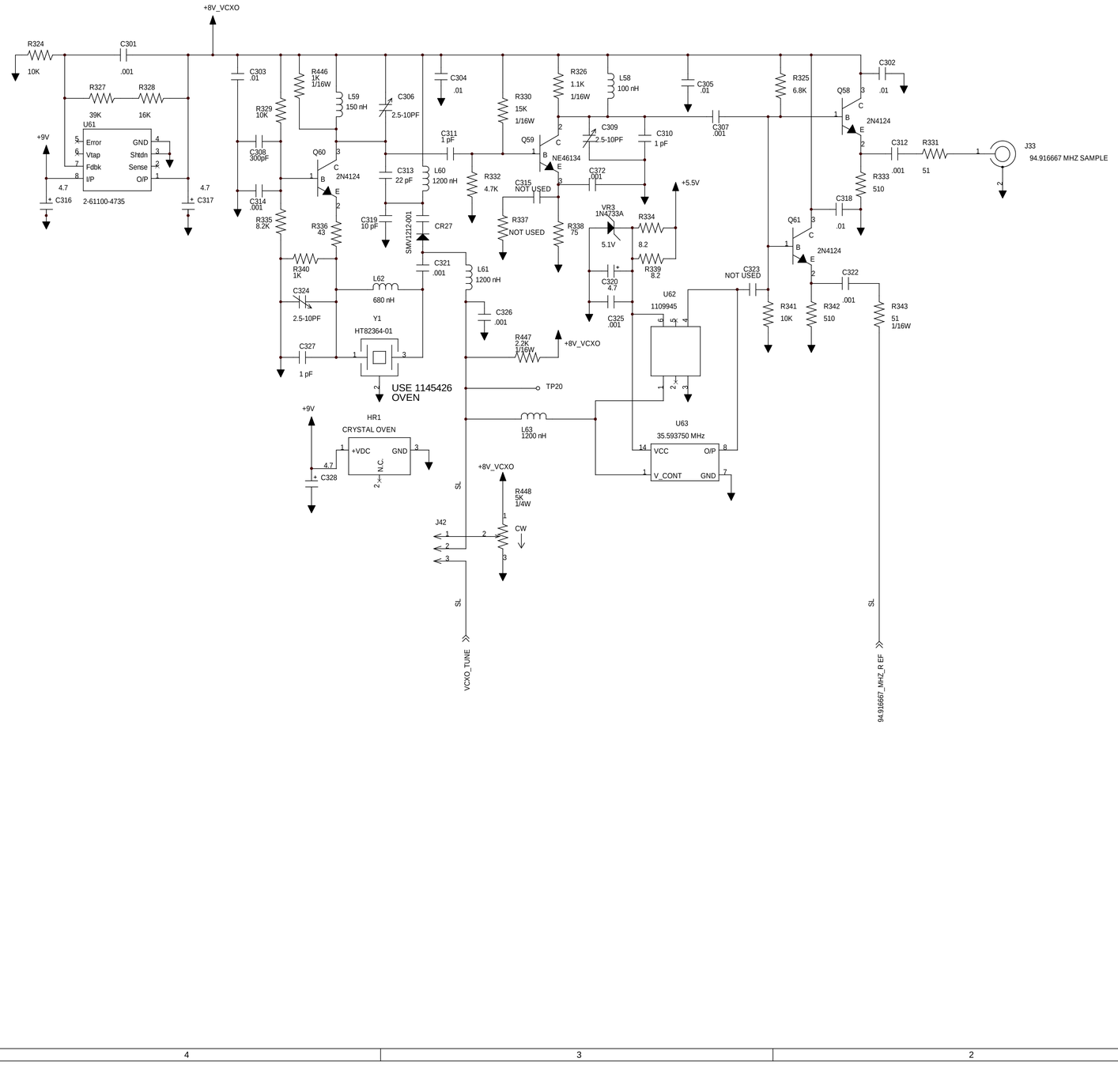
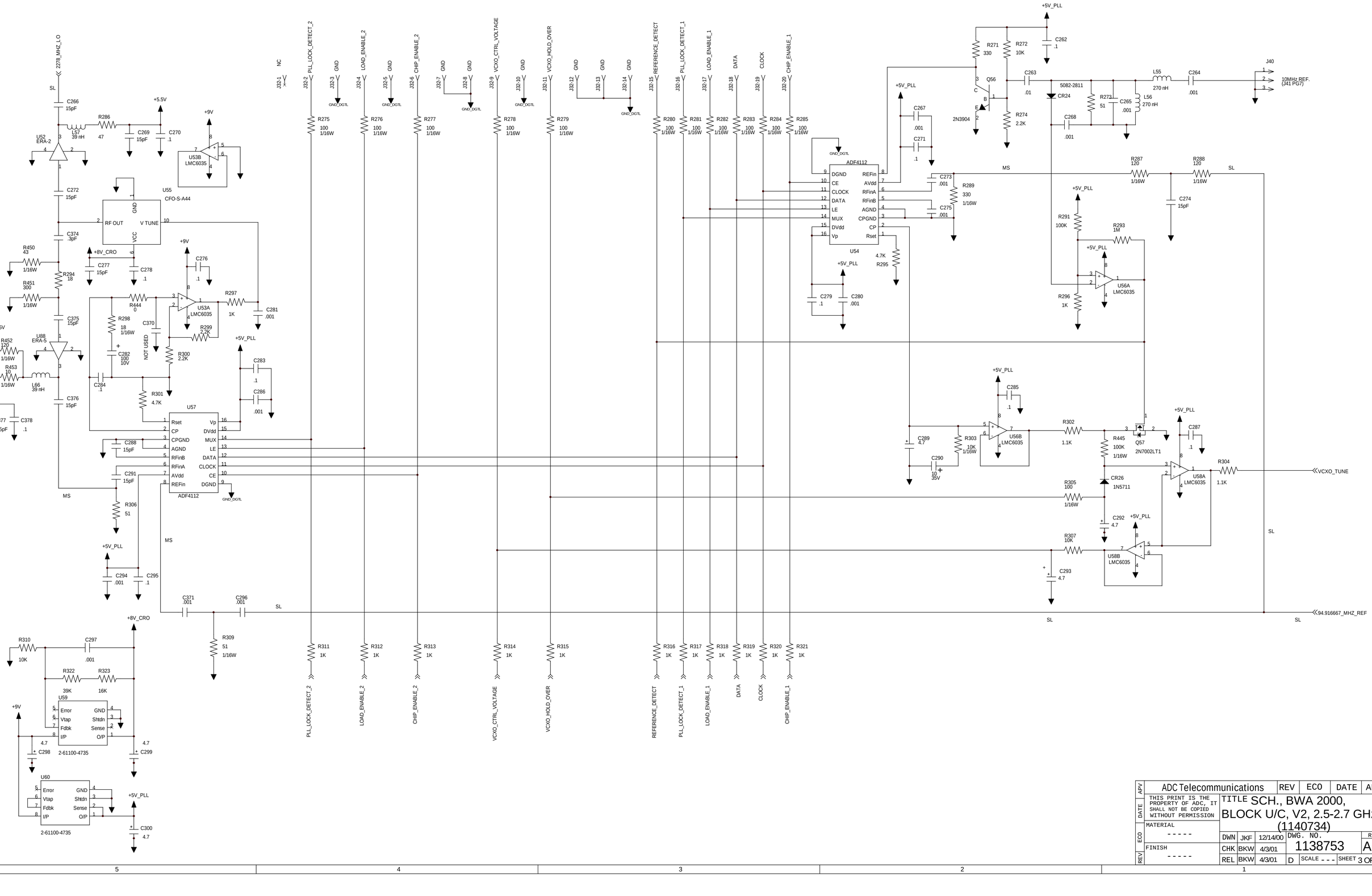
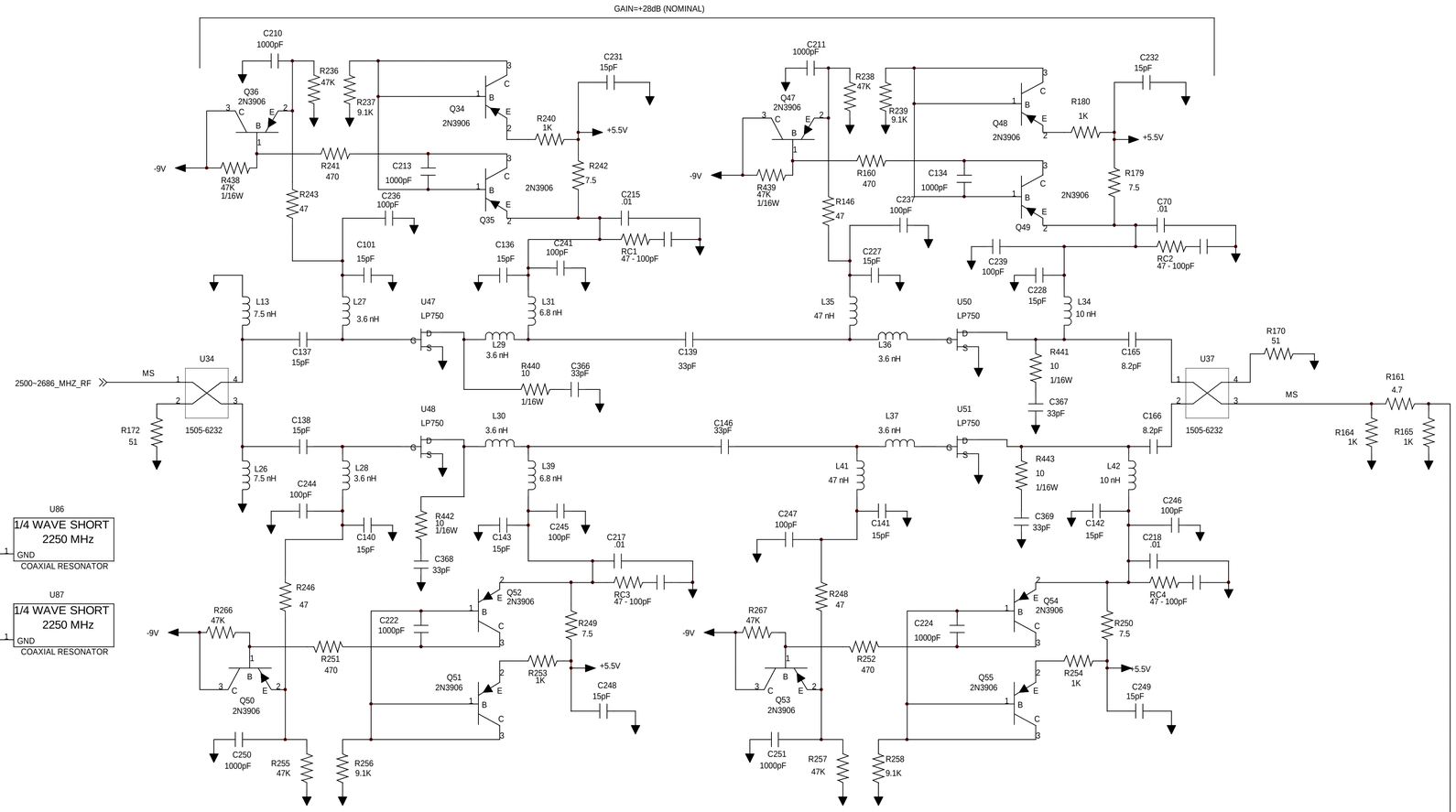
ECO	MATERIAL -----	DWN JKF 12/14/00	DWG. NO. 1138753		REV A0
REV	FINISH -----	CHK BKW 4/3/01			
		REL BKW 4/3/01	D	SCALE ---	SHEET 5 OF 8



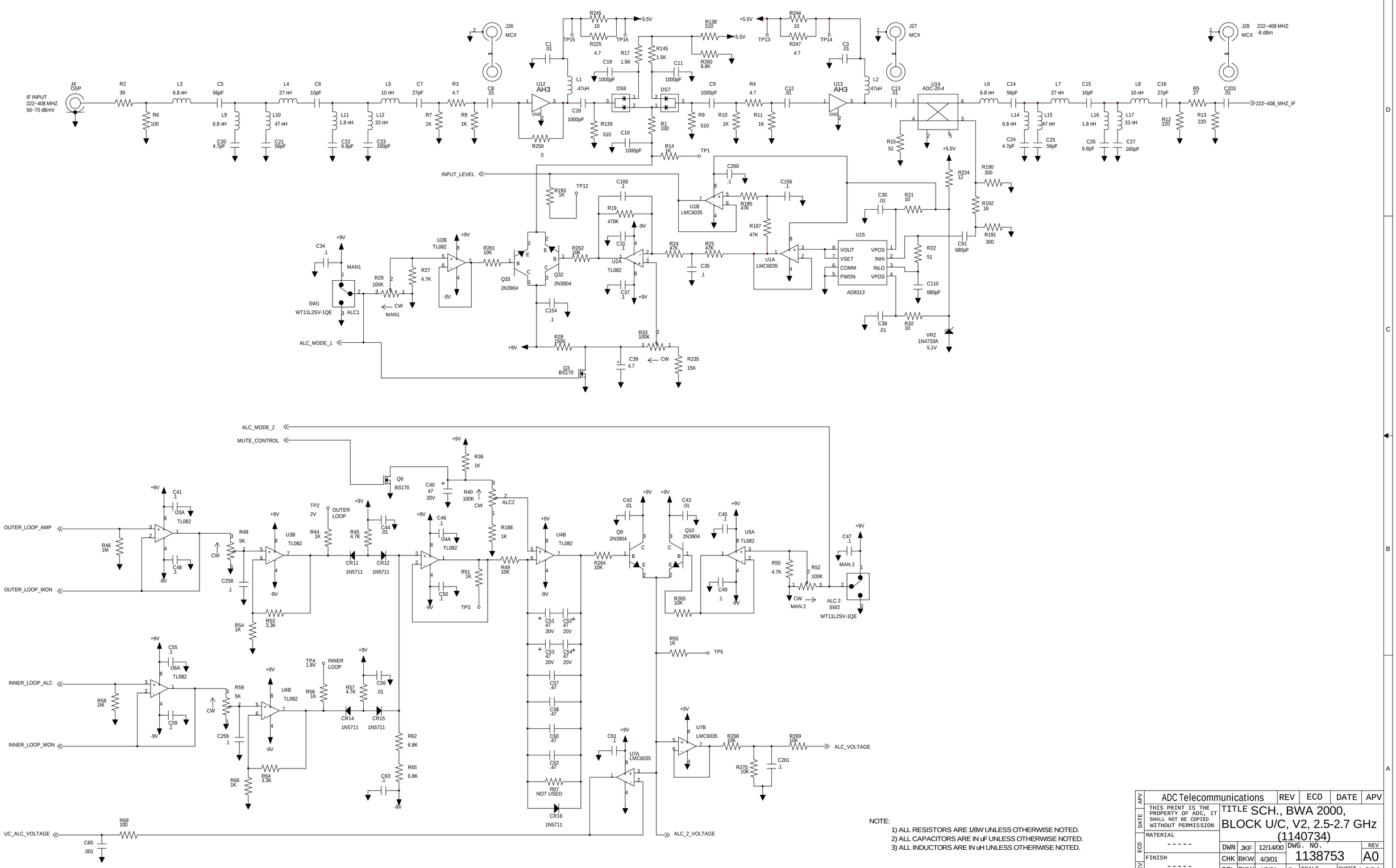
APV	ADC Telecommunications		REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH., BWA 2000, BLOCK U/C, V2, 2.5-2.7 GHz (1140734)				
ECO	MATERIAL -----		DWN	JKF	12/14/00	DWG. NO. 1138753 REV A0
	FINISH -----		CHK	BKW	4/3/01	
REV			REL	BKW	4/3/01	D SCALE - - - SHEET 4 OF 8



APV	ADC Telecommunications		REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH., BWA 2000, BLOCK U/C, V2, 2.5-2.7 GHz (1140734)				
ECO	MATERIAL -----	DWN JKF 12/14/00	DWG. NO. 1138753			REV A0
REV	FINISH -----	CHK BKW 4/3/01				
		REL BKW 4/3/01	D	SCALE ---	SHEET 3 OF 8	



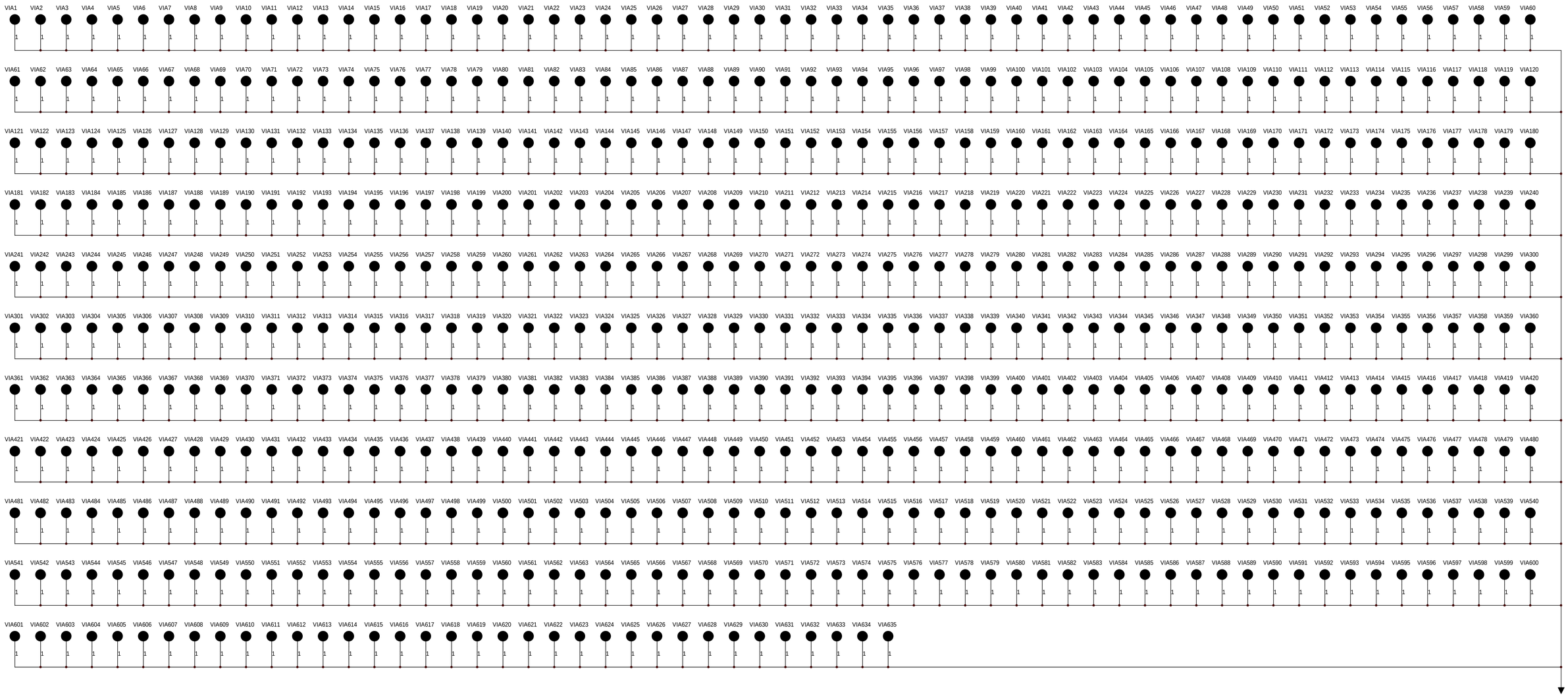
APV	ADC Telecommunications	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH., BWA 2000, BLOCK U/C, V2, 2.5-2.7 GHz (1140734)			
ECO	MATERIAL -----	DWN JKF 12/14/00	DWG. NO. 1138753		REV A0
REV	FINISH -----	CHK BKW 4/3/01			
		REL BKW 4/3/01	D	SCALE - - -	SHEET 2 OF 8



NOTE:

1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.

APV	ADC Telecommunications	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH., BWA 2000, BLOCK U/C, V2, 2.5-2.7 GHz (1140734)			
ECO	MATERIAL -----	DWN	JKF	12/14/00	DWG. NO. 1138753 REV A0
REV	FINISH -----	CHK	BKW	4/3/01	
		REL	BKW	4/3/01	D SCALE --- SHEET 1 OF 8



APV	ADC Telecommunications		REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE <TITLE> {TITLE1} {TITLE2}				
ECO	MATERIAL -----	DWN	{N}	{DATE}	DWG. NO. {DWG NO.}	REV {REV}
REV	FINISH -----	CHK				
		REL			D	SCALE --- SHEET 1 OF 1

J1–13A,B,C– 20A,B,C = NC

A1
MULTIPLEXER BD.

UPSTREAM BPF
41–53 MHz

DOWNSTREAM BPF
222–408 MHz

SPLITTER/
COUPLER

DOWNSTREAM SIGNAL OUTPUT
TO MAIN UPCONVERTER
222–408 MHz
–10dBM NOMINAL PER CARRIER
J1–5B

DOWNSTREAM SIGNAL OUTPUT
TO BACKUP UPCONVERTER
222–408 MHz
–10dBM NOMINAL PER CARRIER
J1–11B

COMMON NETWORK COAXIAL CABLE
TO BROADBAND ROUTER
41–53 MHz, –10dBM NOMINAL PER CARRIER/ 222–408 MHz, 0 dBM NOMINAL PER CARRIER
J1–22B

UPSTREAM SIGNAL INPUT
FROM MAIN DOWNCONVERTER
41–53 MHz
0 dBM NOMINAL PER CARRIER
J1–31B

SPLITTER/
COUPLER

UPSTREAM SIGNAL INPUT
FROM BACKUP DOWNCONVERTER
41–53 MHz
0 dBM NOMINAL PER CARRIER
J1–28B

NOTE: LEVELS OF CARRIERS ARE BASED UPON UPCONVERTER AND DOWNCONVERTER NOMINAL LEVELS, THE MULTIPLEXER BOARD ITSELF CAN FILTER SIGNALS UP TO 25dBM.

ADC Telecommunications

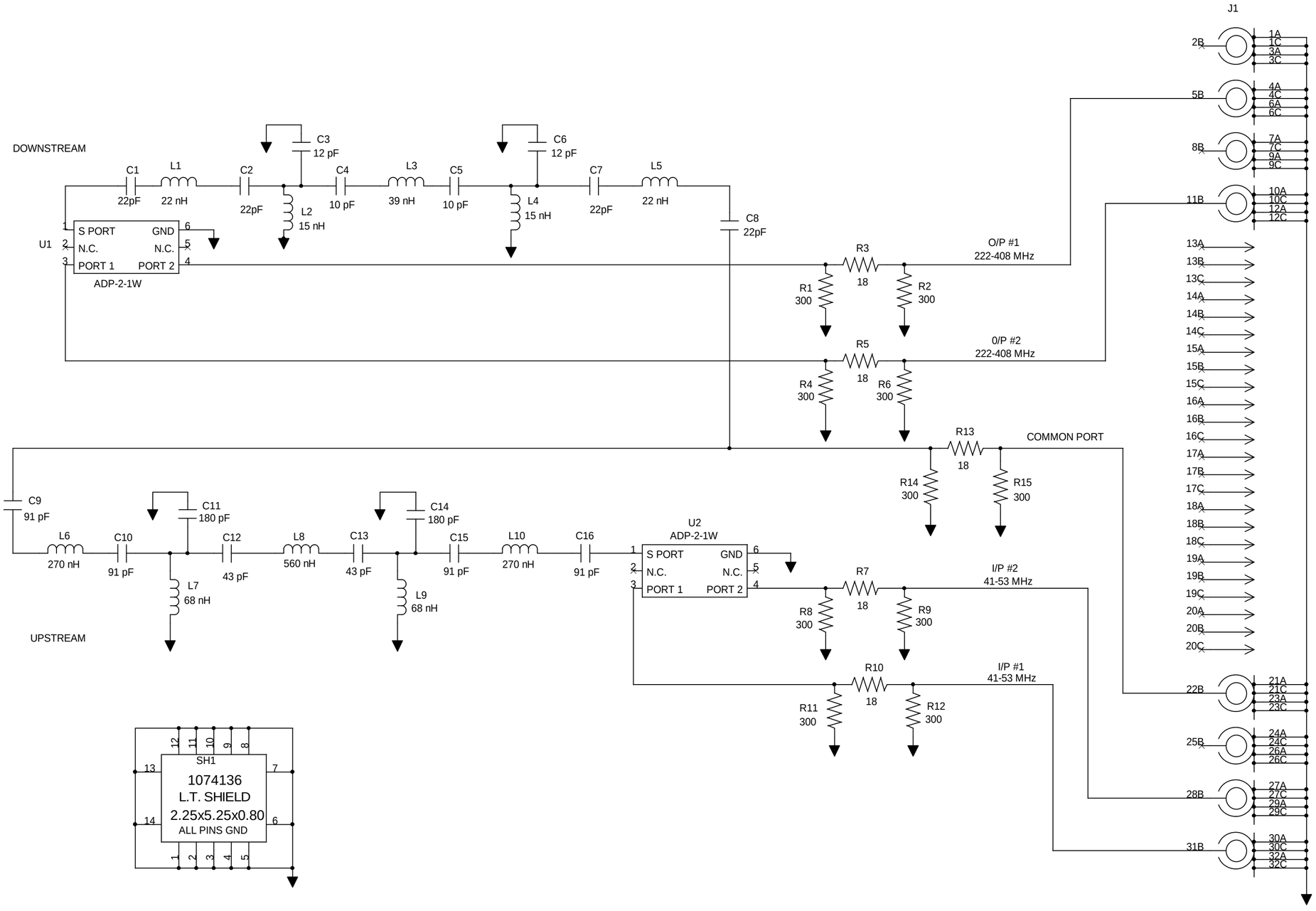
REV	ECO	DATE	APV

MATERIAL
–––––

FINISH
–––––

TITLE B/D, MULTIPLEXER ASSEMBLY

			DWG. NO.	REV
DWN	SAK	1/20/00	1090775	A0
CHK	JCM	11/1/00		
REL	JCM	11/1/00	C SCALE –––	SHEET 1 OF 1



CIRCUIT DESCRIPTION

THE UPSTREAM AND DOWNSTREAM SIGNALS ON THE COMMON NETWORK INTERFACE CABLE ARE FILTERED AND SEPARATED INTO (2) DISCRETE SIGNALS (UPSTREAM, 41-53 MHz & DOWNSTREAM, 222-408 MHz) THE DOWNSTREAM SIGNAL IS SENT TO A SPLITTER (U1) WHICH PROVIDES ONE SIGNAL TO THE MAIN UPCONVERTER AND ONE SIGNAL TO THE BACKUP UPCONVERTER. BOTH UPSTREAM SIGNALS (FROM MAIN & BACKUP DOWNCONVERTERS) ARE COMBINED THROUGH U2 AND SENT TO THE UPSTREAM BANDPASS FILTER. THE OUTPUT OF THE UPSTREAM BANDPASS FILTER IS THEN SENT TO THE COMMOM NETWORK CABLE OF THE BROADBAND ROUTER.

ADDED CIRCUIT DISCRIPTION			RJB
C0	20073657	11/1/00	JCM
J1 WAS 1113708 (10 COAX CONNECTOR) C1,C2,C7,C8 WERE 1114135, 20pF L1,L15 WERE 1114096, 27nH. L3 WAS. 1114097, 47nH.			RJB
B0	20070579	9/29/00	JCM

ADC Telecommunications	REV	ECO	DATE	APV

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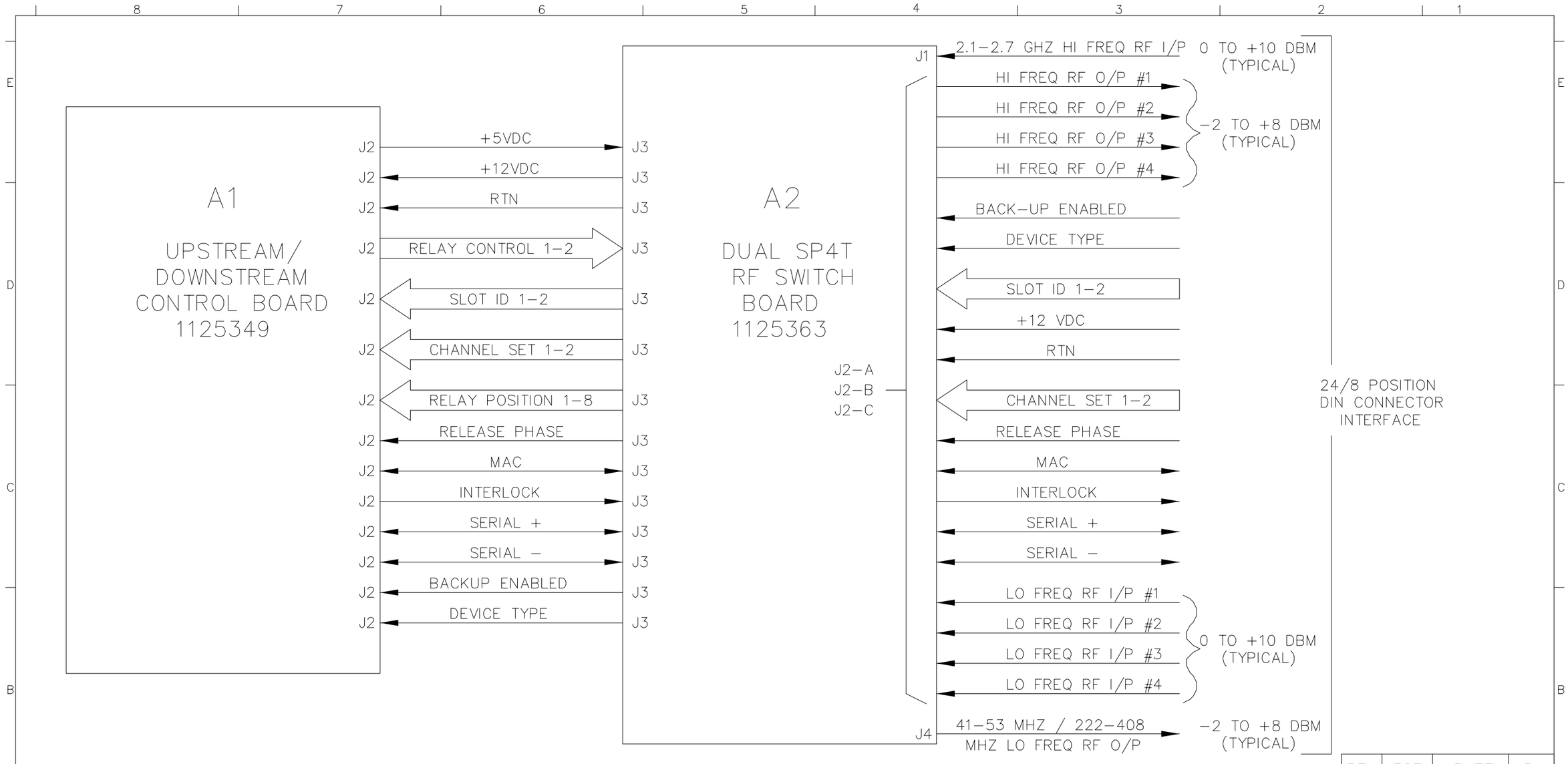
MATERIAL -----

FINISH -----

TITLE SCH MULTIPLEXER

DWN	RJB	5/24/00	DWG. NO. 1113588	REV C0
CHK	JCM	7/21/00		
REL	JCM	7/21/00	C	SCALE - - - SHEET 1 OF 1



REV	ECO	DATE	APV

REV			
ECO			
DATE			
APV			

ADC

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MATERIAL ----

FINISH ----

TITLE
B/D,
UPSTREAM / DOWNSTREAM
SWITCH ASSY

DWN	WB	11/29/00	DWG. NO.	REV
CHK	DEZ	12/20/00	1144128	A0
REL	DEZ	12/20/00	B SCALE---SHEET 1 OF 1	

12/20/2000 03:02:20 PM, kwizes

26 POSITION RIBBON CABLE

A1
UPSTREAM/ DOWNSTREAM CONTROL BOARD
1125349
KEY: J2-21

J2-1	RELAY CONTROL 1	J3-1
J2-2	+5VDC	J3-2
J2-3	RELAY CONTROL 2	J3-3
J2-4	BACK-UP ENABLED	J3-4
J2-5	RELAY POSITION 1	J3-5
J2-6	DEVICE TYPE	J3-6
J2-7	RELAY POSITION 2	J3-7
J2-8	SLOT 1D1	J3-8
J2-9	RELAY POSITION 3	J3-9
J2-10	SLOT 1D2	J3-10
J2-11	RELAY POSITION 4	J3-11
J2-12	CHANNEL SET 1	J3-12
J2-13	RELAY POSITION 5	J3-13
J2-14	CHANNEL SET 2	J3-14
J2-15	RELAY POSITION 6	J3-15
J2-16	+12VDC	J3-16
J2-17	RELAY POSITION 7	J3-17
J2-18	RELEASE PHASE	J3-18
J2-19	RELAY POSITION 8	J3-19
J2-20	MAC	J3-20
J2-21	KEY	J3-21
J2-22	INTERLOCK	J3-22
J2-23	GND	J3-23
J2-24	GND	J3-24
J2-25	SERIAL -	J3-25
J2-26	SERIAL +	J3-26

A2
DUAL SP4T
RF SWITCH BOARD
1125363
KEY: J3-21

J1 (OSP)	2.1-2.7 GHz HI FREQ RF I/P	
J2-2B	HI FREQ RF O/P #4	
J2-5B	HI FREQ RF O/P #3	
J2-8B	HI FREQ RF O/P #2	
J2-11B	HI FREQ RF O/P #1	
J2-13A	BACK-UP ENABLED	
J2-13B	DEVICE TYPE	
J2-13C	SLOT 1D1	
J2-14A	N.C.	
J2-14B	N.C.	
J2-14C	SLOT 1D2	
J2-15A	N.C.	
J2-15B	N.C.	
J2-15C	CHANNEL SET 1	
J2-16A	N.C.	
J2-16B	N.C.	
J2-16C	CHANNEL SET 2	
J2-17A	+12VDC	
J2-17B	+12VDC	
J2-17C	RELEASE PHASE	
J2-18A	N.C.	
J2-18B	MAC	
J2-18C	INTERLOCK	
J2-19A	GND	
J2-19B	GND	
J2-19C	GND	
J2-20A	GND	
J2-20B	SERIAL -	
J2-20C	SERIAL +	
J2-22B	LO FREQ RF I/P #4	
J2-25B	LO FREQ RF I/P #3	
J2-28B	LO FREQ RF I/P #2	
J2-31B	LO FREQ RF I/P #1	
J4 (OSP)	41-53 MHz/ 222-408 MHz LO FREQ RF O/P	

24/8 POSITION DIN CONNECTOR INTERFACE

REV	ECO	DATE	APV

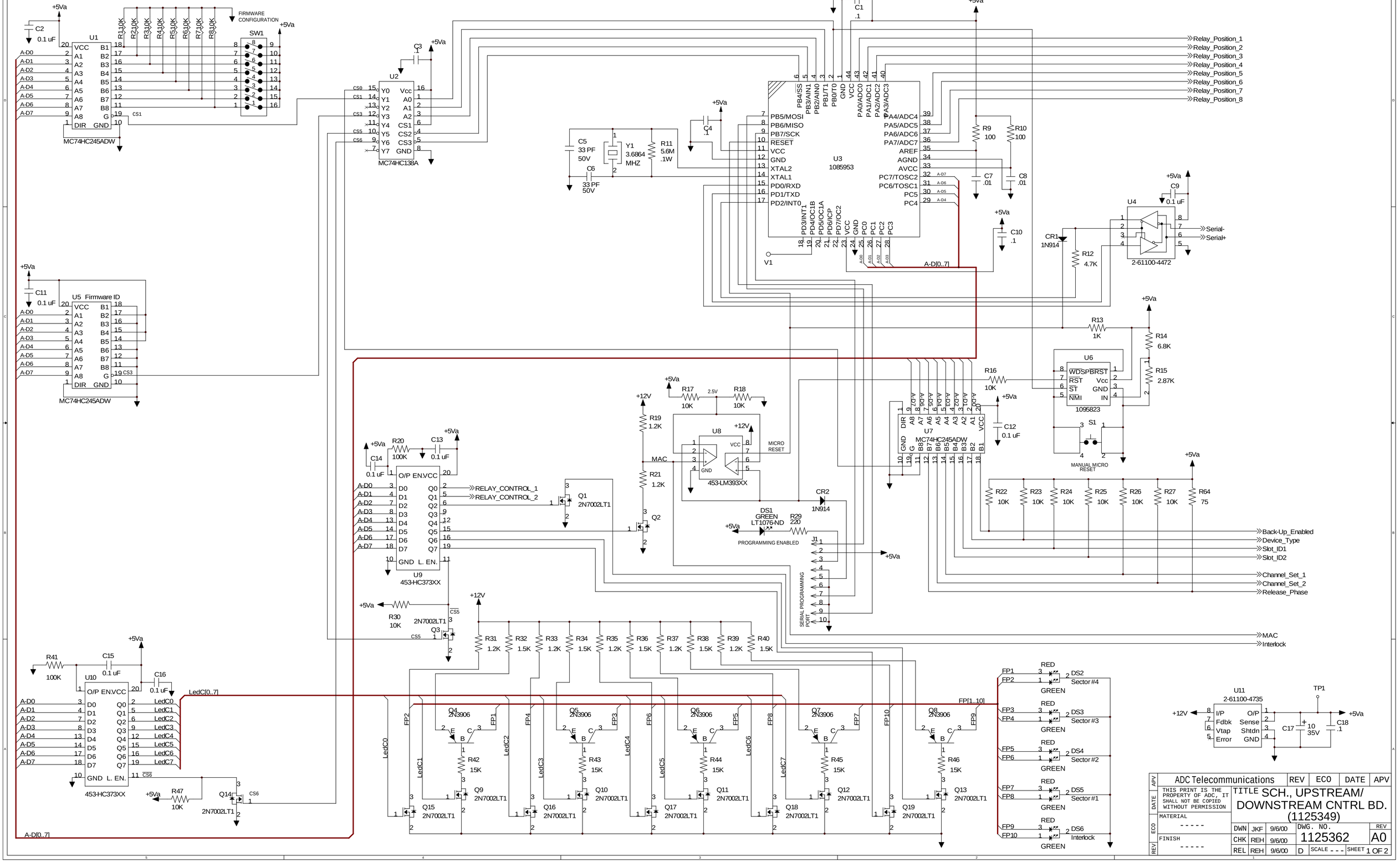
MATERIAL ---

FINISH ---

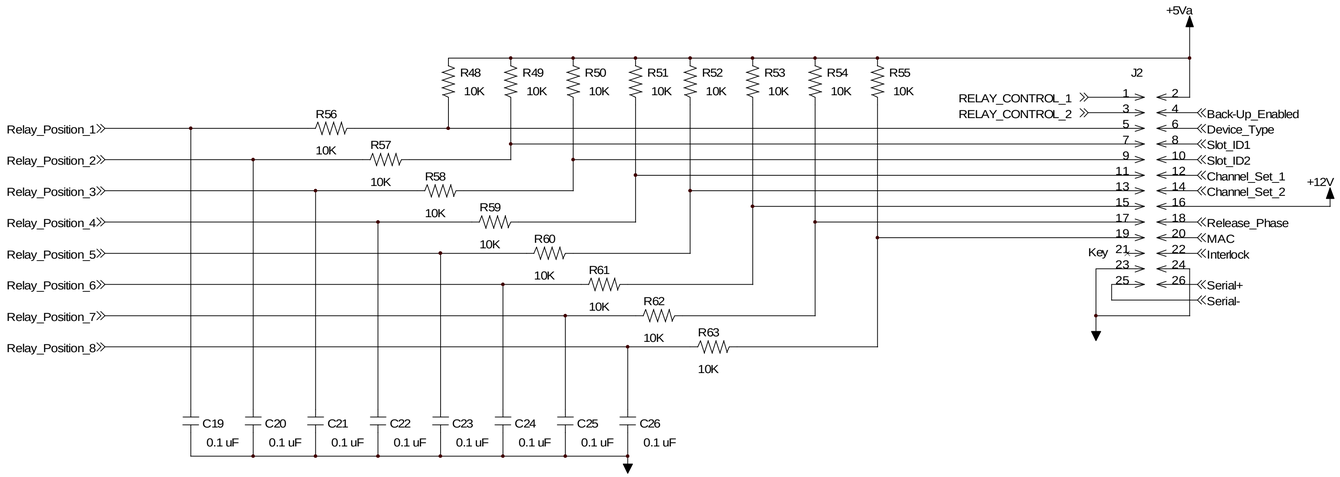
TITLE I/C, UPSTREAM/ DOWNSTREAM SWITCH ASS'Y

DWN	RJB	8/23/00	DWG. NO. 1126654	REV A0	
CHK	DEZ	12/20/00			
REL	DEZ	12/20/00	C	SCALE ---	SHEET 1 OF 1

12/20/2000 8:13 PM kilzes



APV	ADC Telecommunications	REV	ECO	DATE	APV	
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH., UPSTREAM/ DOWNSTREAM CNTRL BD. (1125349)				
ECO	MATERIAL -----	DWN	JKF	9/6/00	DWG. NO. 1125362	REV A0
REV	FINISH -----	CHK	REH	9/6/00		
		REL	REH	9/6/00	D SCALE --- SHEET 1 OF 2	



Circuit Description:

This board controls two low power four to one RF switches. J2 provides the interface between this board and the switches located on the Dual SP4T FR Switch Board (1125367). J2 of the Dual SP4T FR Switch Board provides control interfaces the chassis back plane area.

The Micro Access and Control (MAC) line is used to indicate current device status. If this device is not installed or it is not powered, pin 13A of Jx on the back plane is about ground potential. If this device is installed and operating properly this control line is held at about +12 Vdc through a 1.2 Kohm resistor. If a fault needs to be reported, two 1.20 Kohm resistors are used to set the MAC line at about +6 Vdc. If the system controller needs to reset this device, it will hold the MAC line (pin 13A of J2 on 1125367 or pin 4 of J2 on this board) at about 0.0 Vdc.

U3 is the serial programmable Atmel microcontroller. The controller operates at 3.6864 MHz. This controller monitors the switch position indicators. Any RF port that is not selected is internally terminated within the switch (U1 and U2 of the Dual SP4T FR Switch Board). Since three of the four ports will be terminated, six of the eight resistors of R1 through R8 will be connected to ground through the termination resistor. Since this control board provides a 10 Kohm pull-up resistor on each sense resistor, six of the eight resistor connected to J2 will be at about 2.5 Vdc and the enabled RF channels that are connected to RF common will be at about +5 Vdc

U6 is a watchdog timer IC that monitors PB0 of the micro. If the chip select address line does not change state after about 2 seconds, the reset line (pin 7) is sent low otherwise this line is held at +5 Vdc.

J1 is the programming port used to install the micro's firmware. J1 pin 5 is used by the serial programmer to hold the microcontroller in reset. If J1 pin 5 is low or the watchdog reset line is low, or the MAC line is held low, the microcontroller is reset by pin 7 of U8.

U4 is the serial RS-485 transceiver IC. Pin 2 is used for data direction. During a microcontroller reset, this part is set to receive mode. During normal operation, the microcontroller set this devices data flow direction.

U2 is used for device select. This part is used by the microcontroller to selectively communicate with U7, U1, U5, U10, or U9.

U7 is used for digital input signals. This part is used to monitor the control input lines of this board. The Back-up Enabled line is used to tell this board that the ABS back-up path is enabled. The Device Type lines are used to tell this device if it is backing up upstream data or downstream data. This signal is used to determine the device's SCADA serial address. The Slot 1 and Slot 2 ID lines are also used to determine the device's SCADA address. The Channel Set 1 and 2 lines are used to set the switch position in a BWA2000 Release 1.x implementation. In later releases, the switch position will be set through SCADA commands. The Release Phase line is used to indicate if the switch position is to be set by the Channel Set lines or by SCADA commands; 0 = SCADA commands set switch position while 1 = Channel Set lines.

U1 is used for digital input signals. This part is used to the firmware configuration DIP switch. This switch is used to implement different features of the firmware.

U5 is used for digital input signals. This part is used to specify the desired firmware operation. It is intended that all BWA devices operate using the same firmware. By monitoring these lines, the firmware can determine which type of board it is controlling.

U9 is used for digital output signals. This part is used to control the switch control lines, the Interlock signal, one of the front panel LEDs and the MAC fault notification FET.

U10 is used for digital output signals. This part is used to control the front panel LEDs. Since green LEDs are expected to be normal, a FET is used to shunt current away from the LED when it is to be off. A red LED is not normal therefore a few extra parts are used to only apply power to the LED when is should be on.

U11 is a precise low dropout SMT voltage regulator used to regulate the system +5 Vdc.

APV	ADC Telecommunications	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE SCH., UPSTREAM/ DOWNSTREAM CNTRL BD. (1125349)			
ECO	MATERIAL -----	DWN JKF 9/6/00	DWG. NO. 1125362	REV A0	
		CHK REH 9/6/00			
REV	FINISH -----	REL REH 9/6/00	D	SCALE ---	SHEET 2 OF 2

Circuit Description:

This board contains two low power four to one RF relays. J3 provides the interface between this board and the upstream/downstream switch control board (1125362). J1, J2, and J4 provide the interface between this board and the chassis backplane area.

U1 is a SP4T RF switch. Control pins 9 and 10 are used to select which position is connected to RF common (pin 1). Any RF port that is not selected is internally terminated within U1. Since the switch can not pass DC current, there is no easy way of detecting if a specified path is really engaged.

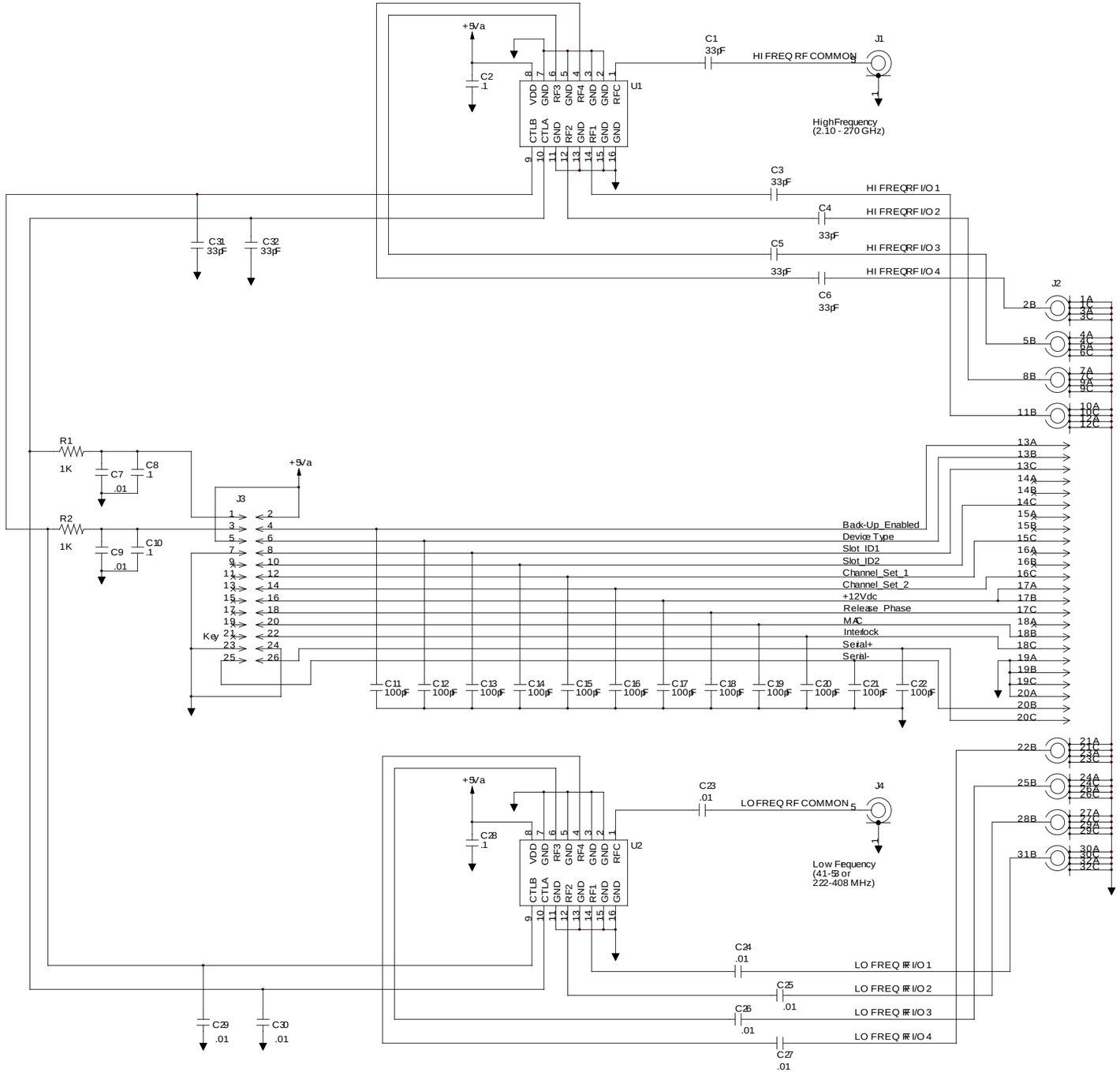
U2 is a second SP4T RF switch. Control pins 9 and 10 are used to select which position is connected to RF common (pin 1). Any RF port that is not selected is internally terminated within U2.

C1, C3 through C6 are DC blocking capacitors. Their values are selected to pass the high frequency (2.150 - 2.162 GHz) RF signals. C23 through C27 are DC blocking capacitors. Values are selected to pass the lower frequency (41 - 53 MHz or 222 - 408 MHz) RF signals.

C2, C11 through C22, and C28 through C32 are RF bypass capacitors which remove unwanted RF signals from DC biaslines. R1 & R2 along with C7 through C10 perform a similar function as low pass filters.

The control lines of J2 pins 13A through 20C are passed on to the upstream/downstream switch control board (1125362) and are described on that board's circuit description.

Pins 5 and 7 of J3 are wired to allow the upstream/downstream switch control board (1125362) determine which board it is controlling. The upstream/downstream switch control board (1125362) may also be used to control the redundant low noise amplifier RF section of a BWA2000 LNA.



CHANGED ALL 15PF CAPS TO 33PF.	JKF	DEZ	APV	ADC Telecommunications	REV	ECO	DATE	APV
	BD	12/1/00	DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION				
	REV	20076142	ECO	MATERIAL -----	TITLE	SCH., DUAL SP4T RF SWITCH BOARD (1125363)		
				FINISH -----	DWN	JKF	9/7/00	DWG. NO. 1125367 REV B0
					CHK	REH	9/22/00	
					REL	REH	9/22/00	D SCALE --- SHEET 1 OF 1

U/C #1
D1
J32A

Holes are needed for OSP Connectors
J30 is IF Input from MUX
J31 is RF Output to PA

913642

J32B

UC_PLL_Flt_S1

10MHz

10 MHz Ref I/P #1
SMB

R1
0 ohm

J33
50 Ohm

J32C

SS1
SS2
SS3
SS4

UC_Ref_Flt_S1
UC_Input_Flt_S1
UC_Mute_Ind_S1
UC_Mute_Cmd_S1
UC_ALC_S1

SS5
SS6

UC_Interlock_S1
System +12Vdc
System -48Vdc
System -12Vdc

UC_MAC_S1

PA_FWR_PWR_S1

PA_ALC_O/P_S1
not monitored

SCADA S+

SCADA S-

U/C #2
D3
J38A

Holes are needed for OSP Connectors
J36 is IF Input from MUX
J37 is RF Output to PA

913642

J38B

UC_PLL_Flt_S2

10MHz

10 MHz Ref I/P #2
SMB

R2
0 ohm

J39
50 Ohm

J38C

SS1
SS2
SS3
SS4

UC_Ref_Flt_S2
UC_Input_Flt_S2
UC_Mute_Ind_S2
UC_Mute_Cmd_S2
UC_ALC_S2

SS5
SS6

UC_Interlock_S2
System +12Vdc
System -48Vdc
System -12Vdc

UC_MAC_S2

PA_FWR_PWR_S2

PA_ALC_O/P_S2
not monitored

SCADA S+

SCADA S-

U/C #5
D5
J44A

Holes are needed for OSP Connectors
J42 is IF Input from MUX
J43 is RF Output to PA

913642

J44B

UC_PLL_Flt_S5

10MHz

10 MHz Ref I/P #5
SMB

J45
50 Ohm

J44C

SS1
SS2
SS3
SS4

UC_Ref_Flt_S5
UC_Input_Flt_S5
UC_Mute_Ind_S5
UC_Mute_Cmd_S5
UC_ALC_S5

SS5
SS6

UC_Interlock_S5
System +12Vdc
System -48Vdc
System -12Vdc

UC_MAC_S5

PA_FWR_PWR_S5

PA_ALC_O/P_S5
not monitored

SCADA S+

SCADA S-

DS SW
D6
J47

2B — unused
5B — unused
8B — unused
11B — unused

DS_Switch_Enabled
Device Type — 0 = Downstream
Slot_ID1
Slot_ID2
DS_Switch_Pos_S1
DS_Switch_Pos_S2
System +12Vdc
Release_Phase
DS_SW_MAC
DS_SW_Interlock
SCADA S-
SCADA S+

Holes are needed for OSP Connectors
J46 is Unused RF Input
J48 is IF Output to U/C #5 (Back-Up)

U/C #3
D7
J51A

Holes are needed for OSP Connectors
J49 is IF Input from MUX
J50 is RF Output to PA

913642

J51B

UC_PLL_Flt_S3

10MHz

10 MHz Ref I/P #3
SMB

R3
0 ohm

J52
50 Ohm

J51C

SS1
SS2
SS3
SS4

UC_Ref_Flt_S3
UC_Input_Flt_S3
UC_Mute_Ind_S3
UC_Mute_Cmd_S3
UC_ALC_S3

SS5
SS6

UC_Interlock_S3
System +12Vdc
System -48Vdc
System -12Vdc

UC_MAC_S3

PA_FWR_PWR_S3

PA_ALC_O/P_S3
not monitored

SCADA S+

SCADA S-

U/C #4
D9
J57A

Holes are needed for OSP Connectors
J55 is IF Input from MUX
J56 is RF Output to PA

913642

J57B

UC_PLL_Flt_S4

10MHz

10 MHz Ref I/P #4
SMB

R4
0 ohm

J58
50 Ohm

J57C

SS1
SS2
SS3
SS4

UC_Ref_Flt_S4
UC_Input_Flt_S4
UC_Mute_Ind_S4
UC_Mute_Cmd_S4
UC_ALC_S4

SS5
SS6

UC_Interlock_S4
System +12Vdc
System -48Vdc
System -12Vdc

UC_MAC_S4

PA_FWR_PWR_S4

PA_ALC_O/P_S4
not monitored

SCADA S+

SCADA S-

Signal Processing Backplane Upper
to Power Amp Backplane

PA_FWR_PWR_S1 — J62-1
J62-2
PA_FWR_PWR_S2 — J62-3
J62-4
J62-5
J62-6
PA_FWR_PWR_S3 — J62-7
J62-8
J62-9
PA_FWR_PWR_S4 — J62-10
J62-11
J62-12
PA_FWR_PWR_S5 — J62-13
J62-14
J62-15
PA_MAC_S1 — J62-16
PA_MAC_S2 — J62-17
PA_MAC_S3 — J62-18
PA_MAC_S4 — J62-19
PA_MAC_S5 — J62-20
J62-21
V1 — J62-22
J62-23
V2 — J62-24
J62-25
V3 — J62-26
J62-27
V4 — J62-28
J62-29
V5 — J62-30
J62-31
V6 — J62-32
V7 — J62-33
V8 — J62-34

Signal Processing Backplane Upper to
Signal Processing Backplane Lower

UC_Interlock_S1 — J61-1
UC_ALC_S1 — J61-2
UC_Mute_Cmd_S1 — J61-3
UC_Mute_Ind_S1 — J61-4
UC_Input_Flt_S1 — J61-5
UC_Ref_Flt_S1 — J61-6
UC_PLL_Flt_S1 — J61-7
UC_Interlock_S2 — J61-8
UC_ALC_S2 — J61-9
UC_Mute_Cmd_S2 — J61-10
UC_Mute_Ind_S2 — J61-11
UC_Input_Flt_S2 — J61-12
UC_Ref_Flt_S2 — J61-13
UC_PLL_Flt_S2 — J61-14
UC_Interlock_S3 — J61-15
UC_ALC_S3 — J61-16
UC_Mute_Cmd_S3 — J61-17
UC_Mute_Ind_S3 — J61-18
UC_Input_Flt_S3 — J61-19
UC_Ref_Flt_S3 — J61-20
UC_PLL_Flt_S3 — J61-21
UC_Interlock_S4 — J61-22
UC_ALC_S4 — J61-23
UC_Mute_Cmd_S4 — J61-24
UC_Mute_Ind_S4 — J61-25
UC_Input_Flt_S4 — J61-26
UC_Ref_Flt_S4 — J61-27
UC_PLL_Flt_S4 — J61-28
UC_Interlock_S5 — J61-29
UC_ALC_S5 — J61-30
UC_Mute_Cmd_S5 — J61-31
UC_Mute_Ind_S5 — J61-32
UC_Input_Flt_S5 — J61-33
UC_Ref_Flt_S5 — J61-34
UC_PLL_Flt_S5 — J61-35
J61-36
UC_MAC_S1 — J61-37
UC_MAC_S2 — J61-38
UC_MAC_S3 — J61-39
UC_MAC_S4 — J61-40
UC_MAC_S5 — J61-41
V11 — J61-42
V12 — J61-43
V13 — J61-44
V14 — J61-45
DS_SW_MAC — J61-46
PA_MAC_S1 — J61-47
PA_MAC_S2 — J61-48
PA_MAC_S3 — J61-49
J61-50
DS_SW_Interlock — J61-51
DS_Switch_Pos_S1 — J61-52
DS_Switch_Pos_S2 — J61-53
DS_Switch_Enabled — J61-54
PA_MAC_S4 — J61-55
PA_MAC_S5 — J61-56
J61-57
SCADA S+ — J61-58
J61-59
SCADA S- — J61-60

J63 SCADA
GND 9
GND 10
SCADA S+
SCADA S-
95123-2881

System +12Vdc — J64 — 55556-4
J65 — 55556-4
System -48Vdc — J67 — 55556-4
System -12Vdc — J66 — 55556-4

UC_MAC_S[1..5]

SAP Numbers:
ASSY: 1149590
SCH: 1149605
PCB: 1149603

CHANGED 75 OHM (1077156) TO 50 OHM (1158860) CONNECTOR PWN

B0	20083150	02/21/01
REV	ECO	DATE

REV	ECO	DATE	APV
B0	20083150	02/21/01	REH

ADC Telecommunications

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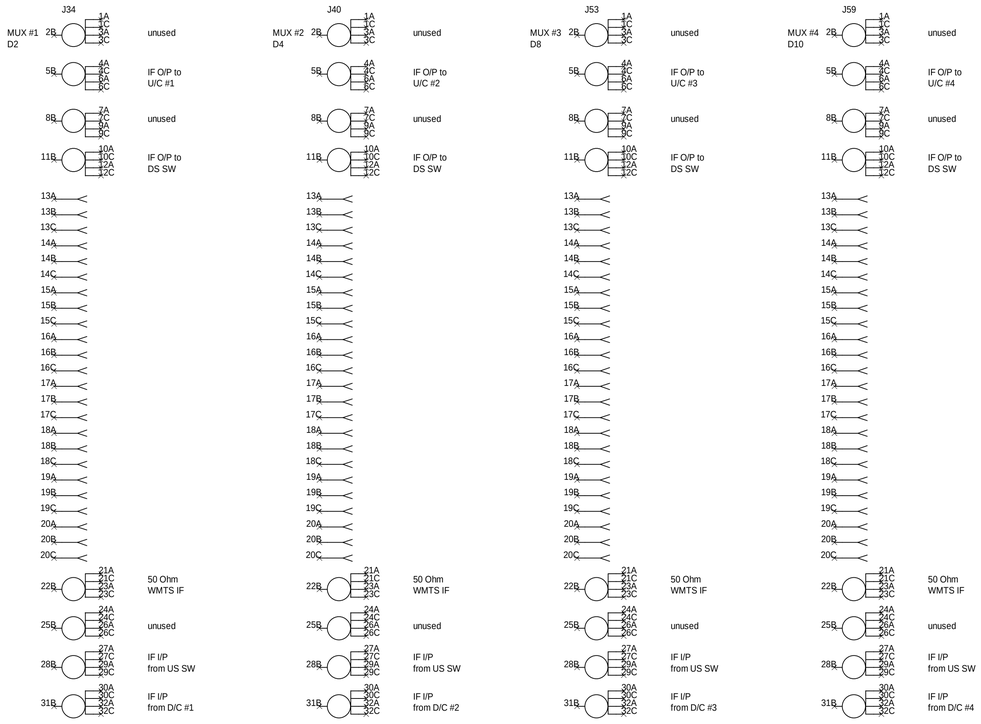
TITLE SCHEMATIC
BTS, RF UPPER
BACKPLANE

MATERIAL

FINISH

DWN	PWN	01/16/01	DWG. NO. 1149605 REV B0
CHK	REH	01/31/01	
REL	REH	01/31/01	D SCALE --- SHEET 1 OF 2



APV	**ADC Telecommunications**	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE	SCHEMATIC BTS, RF UPPER BACKPLANE		
ECO	MATERIAL -----	DWN	PWN 01/16/01	DWG. NO. 1149605	REV B0
REV	FINISH -----	CHK	REH 01/31/01		
		REL	REH 01/31/01	D	SCALE --- SHEET 2 OF 2


LNA #1
E1
J73A
Holes are needed for the OSP RF ports
J70 is Input from US Antenna
J71 is Output to D/C #1
J72 is Output to US SW
J73B
Add hole for OSP port
J74 RF Input from LNA #1).
Add hole for feed through RF port
J75-2B (IF Output to MUX #1).
J73C
LNA #2
E3
J80A
Holes are needed for the OSP RF ports
J77 is Input from US Antenna
J78 is Output to D/C #2
J79 is Output to US SW
J80B
Add hole for OSP port
J81 (RF Input from LNA #2).
Add hole for feed through RF port
J82-2B (IF Output to MUX #2).
J80C
US SW
E5
J88
RF Input from LNA #4
RF Input from LNA #3
RF Input from LNA #2
RF Input from LNA #1
Holes are needed for the OSP RF ports
J87 is RF Output to D/C #5 (Back-Up)
J89 is IF Input from D/C #5 (Back-Up)
US_Switch_Enabled
Device Type
1 = Upstream
Slot_ID1
Slot_ID2
US_Switch_Pos_S1
US_Switch_Pos_S2
System_+12Vdc
Release_Phase
US_SW_MAC
US_SW_Interlock
SCADA_S-
SCADA_S+
IF Output to MUX #4
IF Output to MUX #3
IF Output to MUX #2
IF Output to MUX #1
Add hole for OSP port
J84 (RF Input from US SW).
Add hole for feed through RF port
J85-2B (IF Output to US SW).
LNA #3
E7
J93A
Holes are needed for the OSP RF ports
J90 is Input from US Antenna
J91 is Output to D/C #3
J92 is Output to US SW
J93B
Add hole for OSP port
J94 (RF Input from LNA #3).
Add hole for feed through RF port
J95-2B (IF Output to MUX #3).
J93C
LNA #4
E9
J100A
Holes are needed for the OSP RF ports
J97 is Input from US Antenna
J98 is Output to D/C #4
J99 is Output to US SW
J100B
Add hole for OSP port
J101 RF Input from LNA #4).
Add hole for feed through RF port
J102-2B (IF Output to MUX #4).
J100C
System_+12Vdc
System_-12Vdc
SCADA_S-
SCADA_S+
System_-48Vdc
LNA_Interlock_S1
LNA_Interlock_S2
LNA_Interlock_S3
LNA_Interlock_S4
LNA_MAC_S1
LNA_MAC_S2
LNA_MAC_S3
LNA_MAC_S4
SS1
SS2
SS3
SS4
SS5
SS6
D/C #1
E2
J75
D/C #2
E4
J82
D/C #5 (Back-Up)
E6
J85
D/C #3
E8
J95
D/C #4
E10
J102
IF Output
to MUX
IF Output
to US
SW
unused board mount
straight RF connector
unused
DC_Interlock_S1
DC_Disable_S1
DC_MAC_S1
DC_Interlock_S2
DC_Disable_S2
DC_MAC_S2
DC_Interlock_S5
DC_Disable_S5
DC_MAC_S5
DC_Interlock_S3
DC_Disable_S3
DC_MAC_S3
DC_Interlock_S4
DC_Disable_S4
DC_MAC_S4
10 MHz
REF I/P
10 MHz Ref I/P #1
10 MHz Ref I/P #2
10 MHz Ref I/P #5
10 MHz Ref I/P #3
10 MHz Ref I/P #4
SMB
10MHz
R1
R2
R3
R4
0 ohm
J76
J83
J86
J96
J103
50 Ohm
DC_Disable_S[1..4]
Signal Processing Backplane Lower
to Control Backplane
UC_Interlock_S1 J104-1
UC_ALC_S1 J104-2
UC_Mute_Cmd_S1 J104-3
UC_Mute_Ind_S1 J104-4
UC_Input_Flt_S1 J104-5
UC_Ref_Flt_S1 J104-6
UC_PLL_Flt_S1 J104-7
UC_Interlock_S2 J104-8
UC_ALC_S2 J104-9
UC_Mute_Cmd_S2 J104-10
UC_Mute_Ind_S2 J104-11
UC_Input_Flt_S2 J104-12
UC_Ref_Flt_S2 J104-13
UC_PLL_Flt_S2 J104-14
UC_Interlock_S3 J104-15
UC_ALC_S3 J104-16
UC_Mute_Cmd_S3 J104-17
UC_Mute_Ind_S3 J104-18
UC_Input_Flt_S3 J104-19
UC_Ref_Flt_S3 J104-20
UC_PLL_Flt_S3 J104-21
UC_Interlock_S4 J104-22
UC_ALC_S4 J104-23
UC_Mute_Cmd_S4 J104-24
UC_Mute_Ind_S4 J104-25
UC_Input_Flt_S4 J104-26
UC_Ref_Flt_S4 J104-27
UC_PLL_Flt_S4 J104-28
UC_Interlock_S5 J104-29
UC_ALC_S5 J104-30
UC_Mute_Cmd_S5 J104-31
UC_Mute_Ind_S5 J104-32
UC_Input_Flt_S5 J104-33
UC_Ref_Flt_S5 J104-34
UC_PLL_Flt_S5 J104-35
LNA_Interlock_S1 J104-36
LNA_Interlock_S2 J104-37
LNA_Interlock_S3 J104-38
LNA_Interlock_S4 J104-39
DC_Interlock_S1 J104-40
DC_Disable_S1 J104-41
DC_Interlock_S2 J104-42
DC_Disable_S2 J104-43
DC_Interlock_S3 J104-44
DC_Disable_S3 J104-45
DC_Interlock_S4 J104-46
DC_Disable_S4 J104-47
DC_Interlock_S5 J104-48
DC_Disable_S5 J104-49
J104-50
DS_SW_Interlock J104-51
DS_Switch_Pos_S1 J104-52
DS_Switch_Pos_S2 J104-53
DS_Switch_Enabled J104-54
J104-55
US_SW_Interlock J104-56
US_Switch_Pos_S1 J104-57
US_Switch_Pos_S2 J104-58
US_Switch_Enabled J104-59
J104-60
Signal Processing Backplane Lower to
Signal Processing Backplane Upper
UC_Interlock_S1 J105-1
UC_ALC_S1 J105-2
UC_Mute_Cmd_S1 J105-3
UC_Mute_Ind_S1 J105-4
UC_Input_Flt_S1 J105-5
UC_Ref_Flt_S1 J105-6
UC_PLL_Flt_S1 J105-7
UC_Interlock_S2 J105-8
UC_ALC_S2 J105-9
UC_Mute_Cmd_S2 J105-10
UC_Mute_Ind_S2 J105-11
UC_Input_Flt_S2 J105-12
UC_Ref_Flt_S2 J105-13
UC_PLL_Flt_S2 J105-14
UC_Interlock_S3 J105-15
UC_ALC_S3 J105-16
UC_Mute_Cmd_S3 J105-17
UC_Mute_Ind_S3 J105-18
UC_Input_Flt_S3 J105-19
UC_Ref_Flt_S3 J105-20
UC_PLL_Flt_S3 J105-21
UC_Interlock_S4 J105-22
UC_ALC_S4 J105-23
UC_Mute_Cmd_S4 J105-24
UC_Mute_Ind_S4 J105-25
UC_Input_Flt_S4 J105-26
UC_Ref_Flt_S4 J105-27
UC_PLL_Flt_S4 J105-28
UC_Interlock_S5 J105-29
UC_ALC_S5 J105-30
UC_Mute_Cmd_S5 J105-31
UC_Mute_Ind_S5 J105-32
UC_Input_Flt_S5 J105-33
UC_Ref_Flt_S5 J105-34
UC_PLL_Flt_S5 J105-35
J105-36
UC_MAC_S1 J105-37
UC_MAC_S2 J105-38
UC_MAC_S3 J105-39
UC_MAC_S4 J105-40
UC_MAC_S5 J105-41
V11 J105-42
V12 J105-43
V13 J105-44
V14 J105-45
DS_SW_MAC J105-46
PA_MAC_S1 J105-47
PA_MAC_S2 J105-48
PA_MAC_S3 J105-49
J105-50
DS_SW_Interlock J105-51
DS_Switch_Pos_S1 J105-52
DS_Switch_Pos_S2 J105-53
DS_Switch_Enabled J105-54
PA_MAC_S4 J105-55
PA_MAC_S5 J105-56
J105-57
SCADA_S+ J105-58
J105-59
SCADA_S- J105-60
J107 SCADA
GND
GND
95123-2881
J108
J109
J110
J69
55556-4
SAP NUMBERS:
ASSY: 1149601
SCH: 1149606
PCB: 1149604
ADC Telecommunications
REV ECO DATE APV
THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION
TITLE SCHEMATIC BTS, RF, LOWER BACKPLANE
MATERIAL -----
FINISH -----
DWN PWN 01/24/01
CHK REH 01/31/01
REL REH 01/31/01
DWG. NO. 1149606
REV B0
D
SCALE ---
SHEET 1 OF 2
CHANGED 75 OHM (1071156) TO 50 OHM (1158860) CONNECTOR. PWN
B0 20083151 02/21/01 REH
REV ECO DATE APV

Signal Processing Backplane Lower
to CAM Controller

J106-1	LNA_MAC_S1
J106-2	LNA_MAC_S2
J106-3	LNA_MAC_S3
J106-4	LNA_MAC_S4
J106-5	
J106-6	DC_MAC_S1
J106-7	DC_MAC_S2
J106-8	DC_MAC_S3
J106-9	DC_MAC_S4
J106-10	DC_MAC_S5
J106-11	
J106-12	US_SW_MAC
J106-13	
J106-14	UC_MAC_S1
J106-15	UC_MAC_S2
J106-16	UC_MAC_S3
J106-17	UC_MAC_S4
J106-18	UC_MAC_S5
J106-19	
J106-20	V1
J106-21	V2
J106-22	V3
J106-23	V4
J106-24	DS_SW_MAC
J106-25	
J106-26	PA_MAC_S1
J106-27	
J106-28	PA_MAC_S2
J106-29	
J106-30	PA_MAC_S3
J106-31	
J106-32	PA_MAC_S4
J106-33	
J106-34	PA_MAC_S5

APV	DATE	ECO	REV

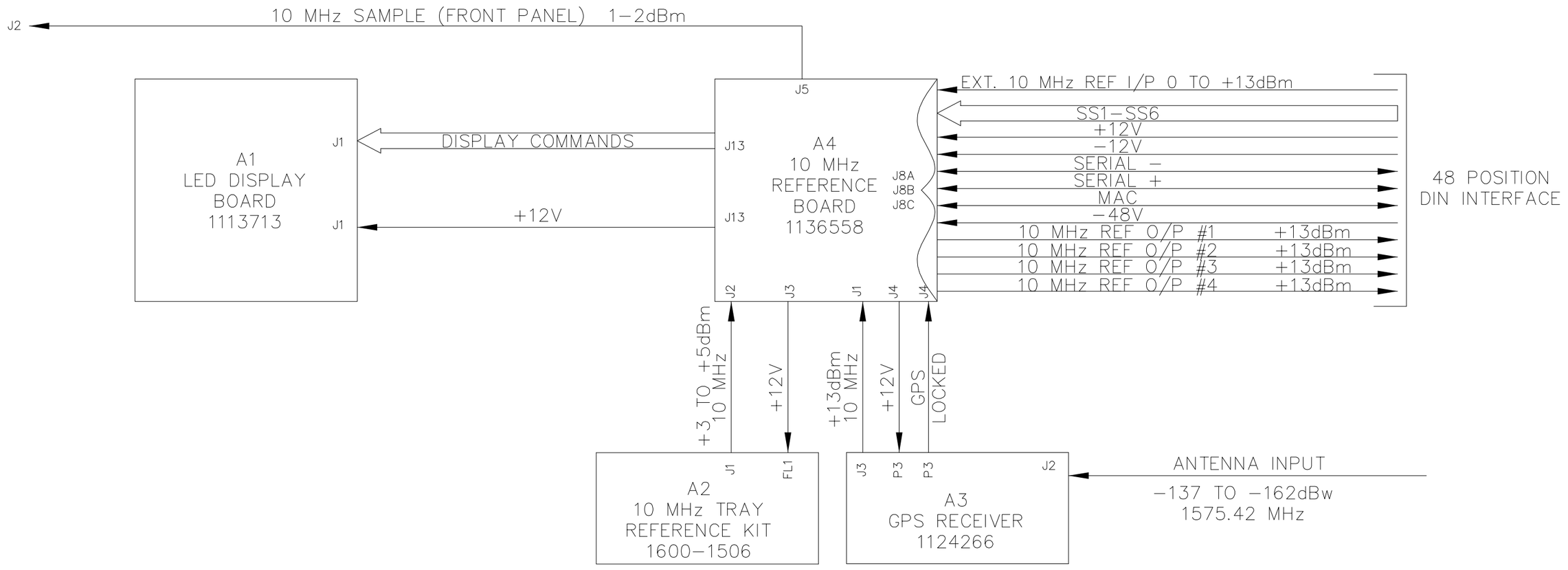
ADC Telecommunications

MATERIAL

FINISH

TITLE SCHEMATIC
BTS, RF, LOWER BACKPLANE

DWN	PWN	01/24/01	DWG. NO.		REV	
CHK	REH	01/31/01	1149606		B0	
REL	REH	01/31/01	D	SCALE - - -	SHEET	2 OF 2



ADC Telecommunications

REV	ECO	DATE	APV

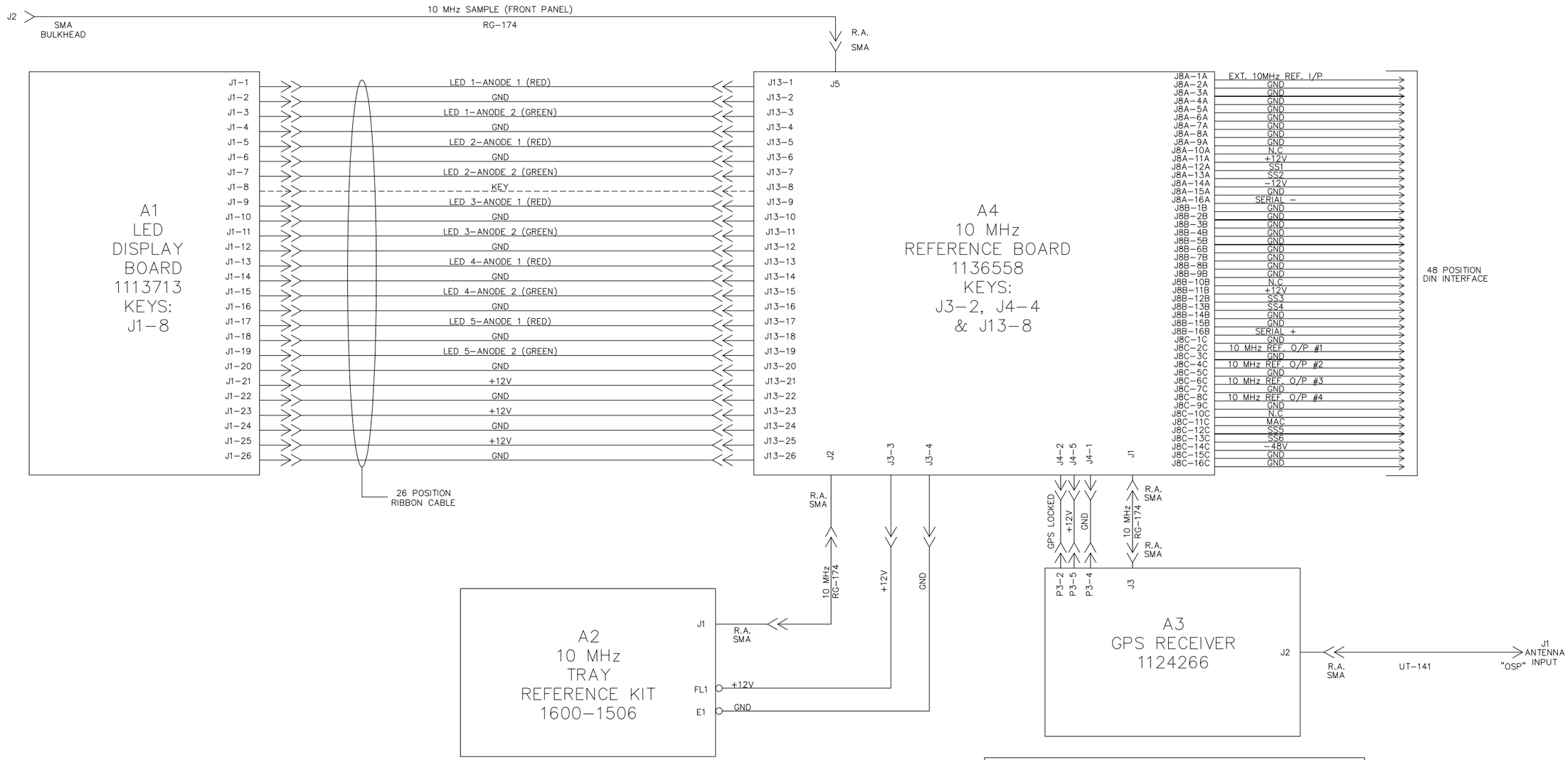
MATERIAL
– – – – –

FINISH
– – – – –

TITLE
B/D, 10MHz
FREQUENCY REFERENCE
ASSEMBLY

			DWG. NO.	REV
DWN	DRC	9/12/00	1129658	A0
CHK	DEZ	12/5/00		
REL	DEZ	12/5/00	B SCALE – – –	SHEET 1 OF 1

12/20/00 09:30:50 AM, c o o l d



NOTE : ALL WIRE IS 22 AWG UNLESS NOTED OTHERWISE

ADC Telecommunications

REV	ECO	DATE	APV

THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION.

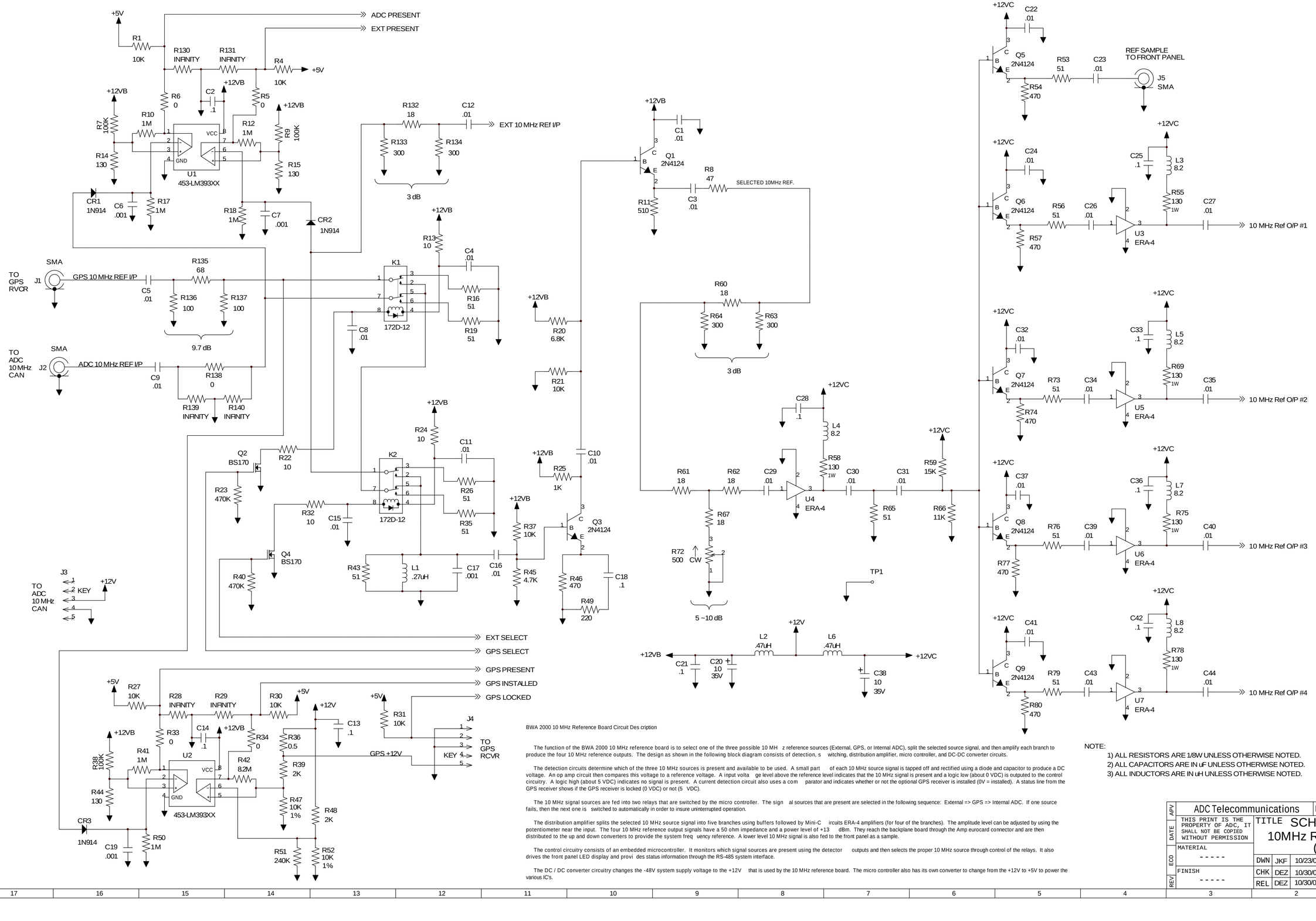
MATERIAL ——————

FINISH ——————

TITLE I/C, 10 MHz FREQ. REFERENCE ASSEMBLY

			DWG. NO.	REV
DWN	DRC	9/12/00	1129669	A0
CHK	DEZ	12/5/00		
REL	DEZ	12/5/00	B SCALE ———	SHEET 1 OF 1

12/19/00 04:06:24 PM. c o o l d



BWA 2000 10 MHz Reference Board Circuit Des cription

The function of the BWA 2000 10 MHz reference board is to select one of the three possible 10 MH z reference sources (External, GPS, or Internal ADC), split the selected source signal, and then amplify each branch to produce the four 10 MHz reference outputs. The design as shown in the following block diagram consists of detection, s witching, distribution amplifier, micro controller, and DC-DC converter circuits.

The detection circuits determine which of the three 10 MHz sources is present and available to be used. A small part of each 10 MHz source signal is tapped off and rectified using a diode and capacitor to produce a DC voltage. An op amp circuit then compares this voltage to a reference voltage. A input volta ge level above the reference level indicates that the 10 MHz signal is present and a logic low (about 0 VDC) is outputed to the control circuitry. A logic high (about 5 VDC) indicates no signal is present. A current detection circuit also uses a com parator and indicates whether or not the optional GPS receiver is installed (0V = installed). A status line from the GPS receiver shows if the GPS receiver is locked (0 VDC) or not (5 VDC).

The 10 MHz signal sources are fed into two relays that are switched by the micro controller. The sign al sources that are present are selected in the following sequence: External => GPS => Internal ADC. If one source fails, then the next one is switched to automatically in order to insure uninterrupted operation.

The distribution amplifier splits the selected 10 MHz source signal into five branches using buffers followed by Mini-C ircuits ERA-4 amplifiers (for four of the branches). The amplitude level can be adjusted by using the potentiometer near the input. The four 10 MHz reference output signals have a 50 ohm impedance and a power level of +13 dBm. They reach the backplane board through the Amp eurocard connector and are then distributed to the up and down converters to provide the system freq uency reference. A lower level 10 MHz signal is also fed to the front panel as a sample.

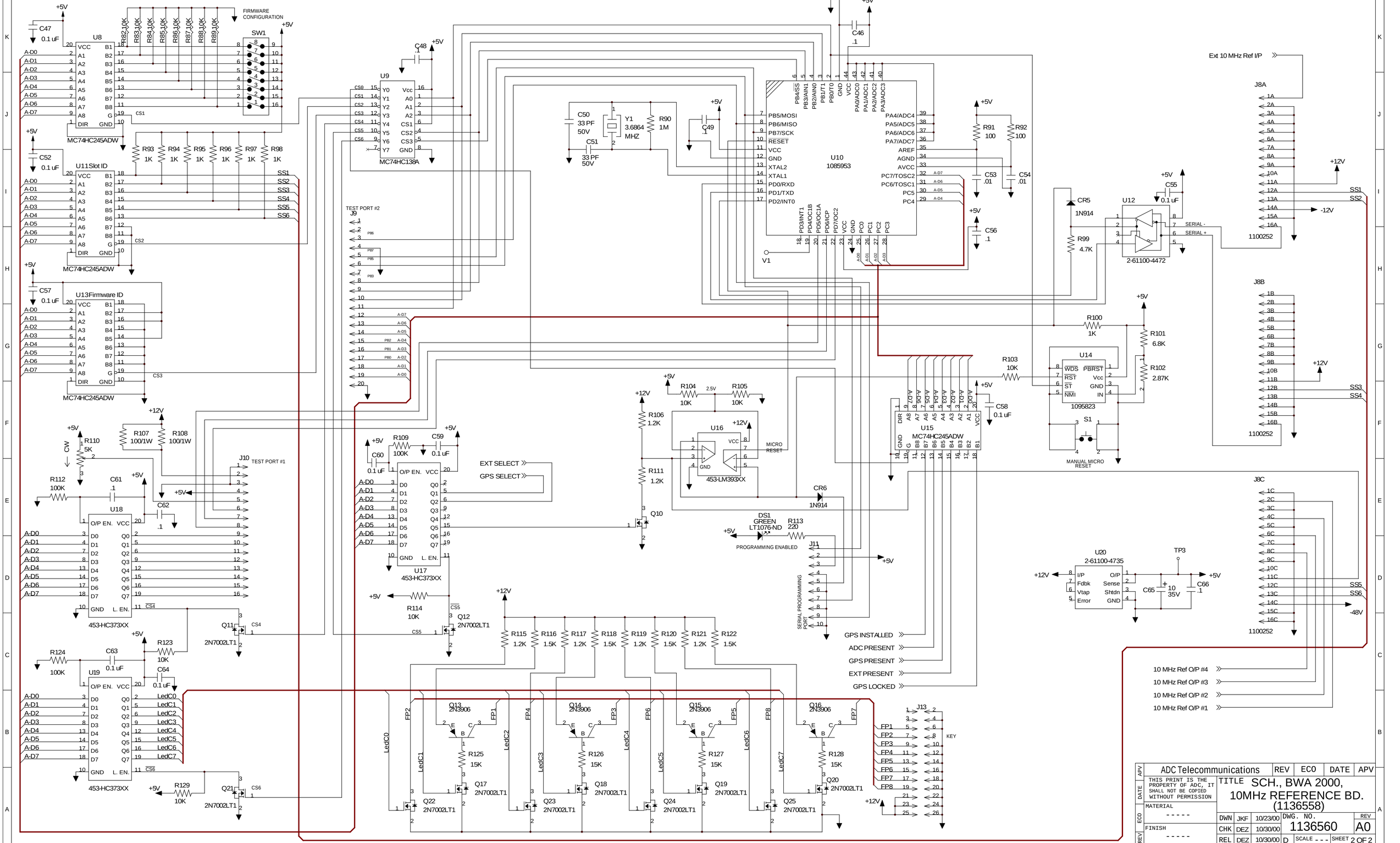
The control circuitry consists of an embedded microcontroller. It monitors which signal sources are present using the detector outputs and then selects the proper 10 MHz source through control of the relays. It also drives the front panel LED display and provi des status information through the RS-485 system interface.

The DC / DC converter circuitry changes the -48V system supply voltage to the +12V that is used by the 10 MHz reference board. The micro controller also has its own converter to change from the +12V to +5V to power the various IC's.

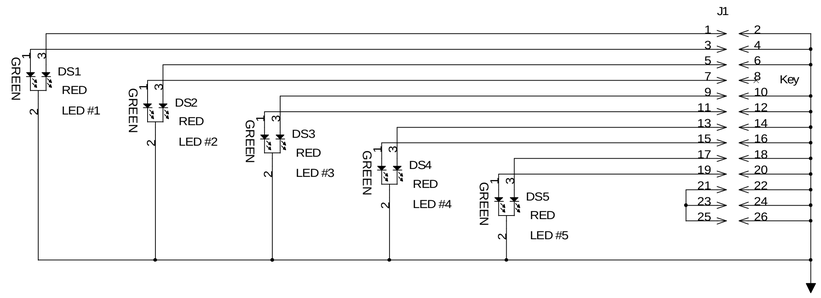
NOTE:

1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.

APV	ADC Telecommunications	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE	SCH., BWA 2000, 10MHz REFERENCE BD. (1136558)		
ECO	MATERIAL -----	DWN	JKF	10/23/00	DWG. NO. 1136560 REV A0
REV	FINISH -----	CHK	DEZ	10/30/00	
		REL	DEZ	10/30/00	D SCALE --- SHEET 1 OF 2



APV	ADC Telecommunications	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE	SCH., BWA 2000, 10MHz REFERENCE BD. (1136558)		
ECO	MATERIAL -----	DWN	JKF	10/23/00	DWG. NO. 1136560 REV A0
REV	FINISH -----	CHK	DEZ	10/30/00	
		REL	DEZ	10/30/00	D SCALE --- SHEET 2 OF 2



APV	**ADC Telecommunications**	REV	ECO	DATE	APV	
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE	SCH., BWA 2000 FRONT PANEL BD. {1113713}			
ECO	MATERIAL -----	DWN	PWN	6/9/00	DWG. NO. 1113710	REV A0
REV	FINISH -----	CHK	REH	6/9/00		
		REL	REH	6/9/00	D	SCALE - - - SHEET 1 OF 1

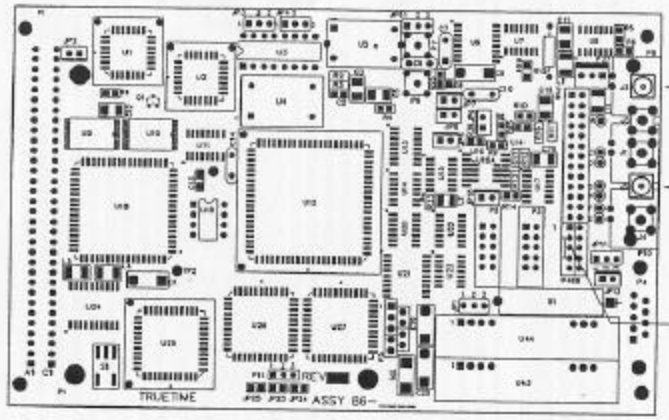
TrueTime

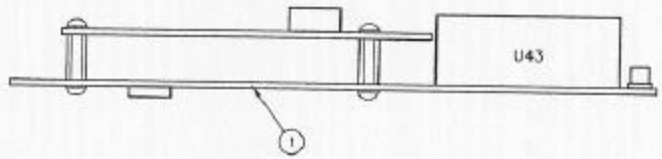
Model 87-664

GPS-XL Time and Frequency Module

TrueTime, Inc. Santa Rosa, CA USA
Phone 707-528-1230 Fax 707-527-6640
www.truetime.com Email truetime@truetime.com

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED





DETAIL-A
SEE TABLE 2
FOR PIN ASSIGNMENT

TABLE 2

PIN	DESCRIPTION
1	ALARM (OPEN COLLECTOR)
2	NC
3	GND
4	GND
5	+12V (9-18VDC)

MATING CONNECTOR:
MOLEX P/N 22-01-3057

CONTRACT NO.	

APPROVALS	DATE
DRAWN BY RNR	07/00
CHECKED BY	
APPROVED BY DRR	7/00

NEXT ASSY

TrueTime
"Where Customer Satisfaction is our Highest Priority"
2835 Duke Ct. Santa Rosa, CA 95407

ASSEMBLY, GPS-XL 12VDC/10MHz (SMA)

SIZE	CODE IDENT NO.	DRAWING NO.	REV
B		87-664	A

SCALE NONE SHEET 1 OF 2

FILENAME: \87\87-664
DATE: 07-19-00

1-31 PHYSICAL SPECIFICATIONS

1-32 The GPS-XL is a board level product with the following physical specifications:

GPS-XL Module Size:	3.94 in. x 6.30 in. x .91 in. (10 cm. x 16 cm. x 2.31 cm.)
Antenna Size:	2.625 in. dia. x 1.5 in. (6.67 cm. dia x 3.81 cm.)
Antenna/DownConverter Size: (Optional)	2.625 in. dia. x 8.6 in. (6.67 cm. dia. x 21.84 cm.)

Note: Antenna and Antenna/DownConverter Units are mounted on a 12 in. long PVC nipple with 3/4" Male Pipe Thread (MPT) on both ends. The above specified overall lengths of the Antenna and Antenna/DownConverter Units are therefore increased by approximately 11.25 in. when the mounting nipple is included.

GPS-XL Module Weight:	.4 lb max. (.186 Kg)
Antenna Weight: (Including mtg. nipple)	0.70 lb (.318 Kg)
Antenna/DownConverter Weight: (Including mtg. nipple) (Optional)	2.35 lb (1.067 Kg)
Antenna Cable, RG-59:	Standard length = 50 ft. 1.2 lb (.545 Kg)
Antenna/DownConverter Cable, RG-58: (Optional)	Standard length = 200 ft. 5.4 lb (2.452 Kg)

1-33 ENVIRONMENTAL SPECIFICATIONS

1-34 The environmental specifications are:

Operating Temperature:	
Antenna or Antenna/DownConverter:	-40° to +70° C (-40° to +158° F)
GPS-XL Module:	0° to +60° C (+32° to +140° F)
Storage Temperature:	
Antenna or Antenna/DownConverter:	-55° to +85° C (-67° to +185° F)
GPS-XL Module:	-40° to +85° C (-40° to +185° F)
Humidity:	
Antenna or Antenna/DownConverter:	100%, condensing
GPS-XL Module:	95%, non-condensing

1-35 POWER INPUT SPECIFICATIONS

SUPPLY OPTION	VOLTAGE	RIPPLE+NOISE	POWER
Standard Antenna:			
12 VDC & 5 VDC (STANDARD)	+/- 5%	<75 mV, 100 KHz BW	1.00 W @ 12V 3.75 W @ 5V
12 VDC (OPTION)	+/- 5%	<75 mV, 100 KHz BW	6.00 W
12 VDC (Batt.) (OPTION)	8-16.5 VDC	<1 V, 100 KHz BW	6.25 W
24 VDC (Batt.) (OPTION)	16-32 VDC	<1 V, 100 KHz BW	6.25 W
Antenna/DownConverter Option:			
12 VDC & 5 VDC (STANDARD)	+/- 5%	<75 mV, 100 KHz BW	3.00 W @ 12V 3.75 W @ 5V
12 VDC (OPTION)	+/- 5%	<75 mV, 100 KHz BW	8.00 W
12 VDC (Batt.) (OPTION)	8-16.5 VDC	<1 V, 100 KHz BW	8.75 W
24 VDC (Batt.) (OPTION)	16-32 VDC	<1 V, 100 KHz BW	8.75 W

1-36 BATTERY SPECIFICATIONS

The battery provides standby power to the GPS-XL memory.

Battery type: Lithium, 3.5 Volt

Battery life: 15000 hours standby, shelf life 10 years

1-37 TIMING/FREQUENCY PERFORMANCE SPECIFICATIONS

1-38 All performance specifications are valid when the antenna's geodetic position is known within 10 m in WGS-84 and four or more satellites are being tracked under the current conditions of Selective Availability (SA) as experienced at product release in March of 1994. In addition, in order to achieve the stated stability specifications, **the GPS-XL must be mounted in an enclosure which will eliminate exposure of the internal oscillator to rapid tempurature fluctuations due to air currents**. During periods without SA, timing performance is improved to the +/- 100 nS level.

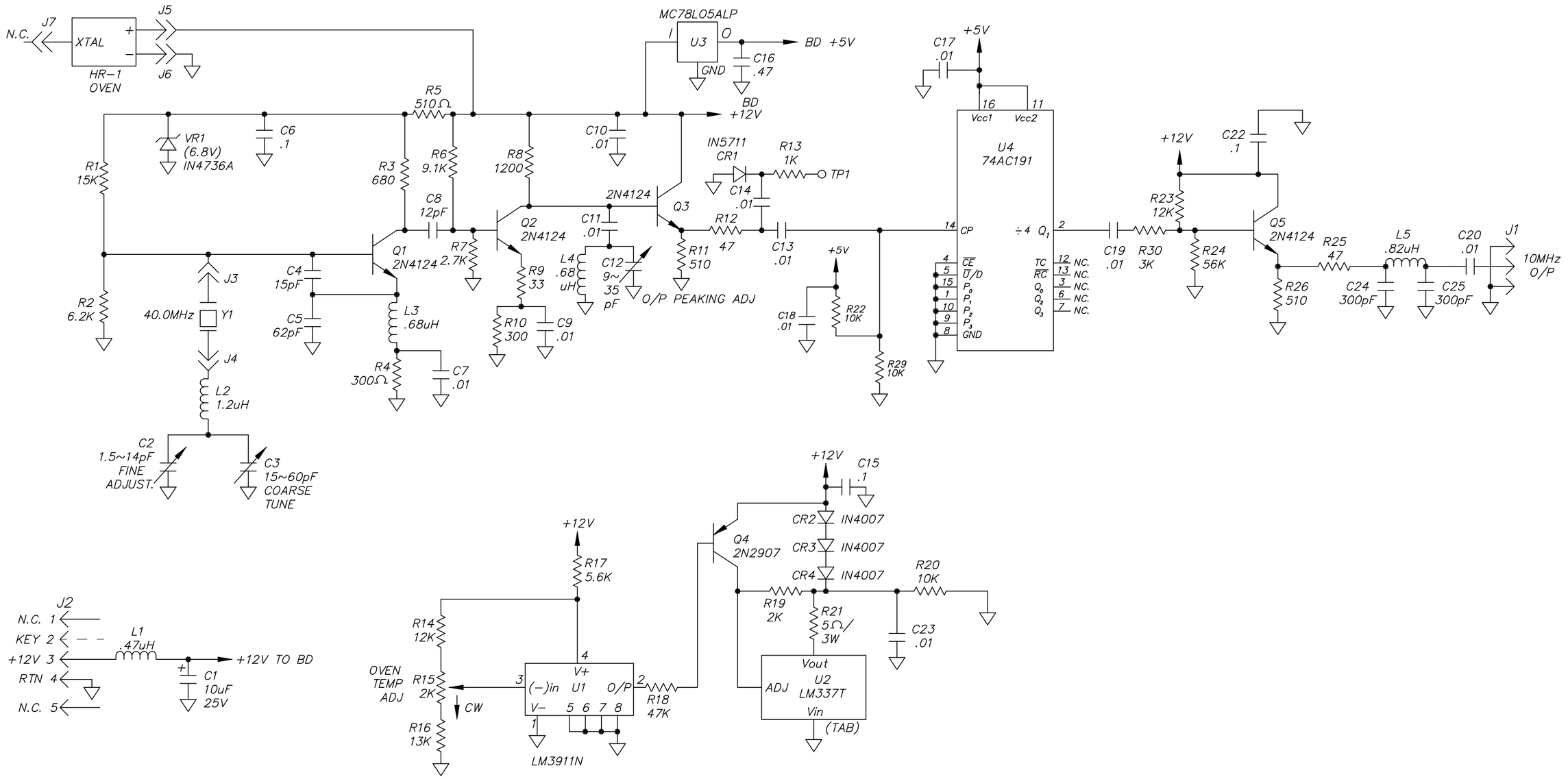
The GPS-XL core receiver specifications are:

Frequency:	1575.42 MHz (L1 signal).
Code:	Coarse Acquisition (C/A) code.
Tracking:	Up to six satellites.
Acquisition Time:	Less than 2 min if satellites visible, position correct within 100 km. Position errors greater than 100 km may require 15 min or longer, with satellites visible. See Section III.
Single Fix Position Accuracy:	Within 25 m (SEP) referred to WGS84 when sequentially tracking four (4) or more satellites with a PDOP $\leq$ 6. 100 meters (2 dRMS) if SA is enabled.
24 Hour Averaged Position Accuracy:	< 10 m.

The GPS-XL timing and frequency specifications are:

1PPS Output Accuracy:	GPS Time +/- 150 nS. UTC-USNO +/- 150 nS.
Frequency Output Accuracy:	$< 3 \times 10^{-12}$
Frequency/Timing Stability:	Allan Deviation, 1×10^{-9} @ 1 sec 3×10^{-10} @ 10 sec 3×10^{-10} @ 100 sec 3×10^{-12} @ 1 day
Oscillator Stability:	2×10^{-6}, over 0°C to 50°C when not tracking satellites.

IRIG B Amp. Mod. Output (STANDARD):
Accuracy: 10 uS to UTC



CHG'D PART # AT U4 FROM MC74AC190 TO 74AC191			JWG
2	8432	9/17/96	BKW
10MHZ AT J1 WAS 5MHZ.			SL
1	4401	9/28/95	JCM
REV	ECN	DATE	APV

ITS CORPORATION

MATERIAL ------

FINISH ------

TITLE SCHEMATIC- 10MHz REFERENCE GENERATOR BD. (1519-3126)

DWN	RT	5/17/95	DWG. NO. 1519-3126 REV 2
CHK	BKW	8/7/95	
REL	BKW	8/7/95	C SCALE --- SHEET 1 OF 1

J1A
913289
1A PA INTERLOCK
2A PA P.S. GOOD
3A PA P.S. ENABLE
4A PA OPER RQST
5A UNUSED #1
6A UNUSED #2
7A UNUSED #3
8A SPARE ANALOG #1
9A SYSTEM PS STAT 1
10A SYSTEM PS STAT 2
11A UC ALC SPARE
12A
13A FWD PWR METERING
14A
15A
16A
17A UC INTERLOCK
18A UC ALC VOLTAGE
19A UC MUTE CMD
20A UC MUTE INDICATOR
21A UC INPUT FAULT
22A UC REF FAULT
23A SPARE ANALOG OUT
24A LCD CTRL SELECT 2
25A LCD CTRL SELECT 5
26A
27A
28A
29A
30A
31A
32A UC PLL FAULT

J1B
913289
1B BPF INTERLOCK
2B SET BPF RELAY MAIN
3B BPF RELAY POSITION
4B SET BPF RELAY ABS
5B SLOT ID 3
6B CTRL INTERLOCK RTN
7B CTRL INTERLOCK
8B PS1 LOAD E
9B PS2 LOAD E
10B CTRL OPERATE IND
11B PS3 LOAD E
12B SPARE ANALOG IP #2
13B SPARE ANALOG INPUT 3
14B LCD CTRL SELECT 1
15B LCD CTRL SELECT 4
16B
17B SPARE OUT 1
18B SPARE OUT 2
19B RMT FWD PWR O/P
20B RMT REFL PWR O/P
21B SPARE OUT 3
22B SPARE OUT 4
23B ENABLE BACKUP CTRLR O/P
24B SPARE OUT 5
25B SPARE OUT 6
26B LCD BUFFER ENABLE
27B ABS BACKUP ENABLE
28B ENABLE BACKUP IP
29B -5V BIAS SENSE
30B PA OUTPUT STATUS
31B PA TEMP STATUS
32B REFL PWR METERING

J1C
913289
1C
2C LCD FAULT LED
3C
4C SPARE OUT 7
5C S5
6C S4
7C S3
8C S2
9C S1
10C
11C
12C CONTRAST
13C LCD RS
14C LCD R/W
15C LCD E
16C DB0
17C DB1
18C DB2
19C DB3
20C DB4
21C DB5
22C DB6
23C DB7
24C
25C
26C SERIAL +
27C
28C SERIAL -
29C DISABLE BACKUP CTRLR
30C LCD CTRL SELECT 3
31C SLOT ID 1
32C SLOT ID 2

J3

TEST INTERFACE

SW1

SW2
WT15L2SV-1QE

U3 MC74HC245ADW
U6 MC74HC245ADW
U7 MC74HC245ADW
U9 MC74HC245ADW
U12 MC74HC245ADW
U18 MC74HC245ADW

U10 MC7805CT

U13
OPTO ISOLATOR

U14
2-61100-4472

U17
MC68HC705B16CFN

U25
1095823

Y1
3.6864
MHZ

DS1
5300H5
Default

Q18
BS170

Q20
BS170

Q1
BS170

Q2
BS170

U1 U2 U8 U11 SN74H377DW

U4A U4B U4C U4D
MC74HC00ADR2

U5A U5D U5E U5F
MC74HC04N

U15A U15B
MC74HC138A

U16 U19
MC74HC138A

DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
R/W
/DS
/CS9
/CS4
/CS2
/CS3
/CS1
/CS0
/CS7
/CS8
/CS6
/CS5

DISABLE BACKUP CTRLR
BPF RELAY POSITION
LCD CTRL SELECT 1
LCD CTRL SELECT 2
LCD CTRL SELECT 3
LCD CTRL SELECT 4
LCD CTRL SELECT 5

SLOT ID 1
SLOT ID 2
SLOT ID 3
PS1 LOAD E
PS2 LOAD E
PS3 LOAD E

S1
S2
S3
S4
S5

PA INTERLOCK
PA TEMP STATUS
-5V POWER IND
PA OPER RQST
SYSTEM PS STAT 1
SYSTEM PS STAT 2
PA P.S. GOOD

UC INTERLOCK
UC MUTE INDICATOR
UC INPUT FAULT
UC REF FAULT
ABS BACKUP ENABLE
ENABLE BACKUP IP
UC PLL FAULT
BPF INTERLOCK

UNUSED #1
UNUSED #2
UNUSED #3
UC MUTE CMD
PA P.S. ENABLE
-5V POWER IND

O/P AMP STATUSBUF
PA OUTPUT STATUS
SERIAL -
SERIAL +
Q17toQ20
AN[0..7]
D[0..7]
A[0..5]
PLMB
LCD R/W
LCD RS
/CS[0..9]

REMOVED DO NOT INSTALL SYMBOLS ON SPECIFIED PARTS. PWN

C0	20085157	03/19/01	REH

ADD PARTS: Q20, CHANGE C19, C21, Y1, AND R67 TO SMT PARTS. CHANGE U14 PART NUMBER. ADD U25 (1095823), R139 (6.8K), AND R140 (2.87K). DELETE R73 AND C22. FIX LINES 7 AND 8 ON U14. PWN

B0	20079417	01/15/01	REH

NOTES: INDICATES COMPONENT IS NOT USED.

ADC Telecommunications

REV	ECO	DATE	APV

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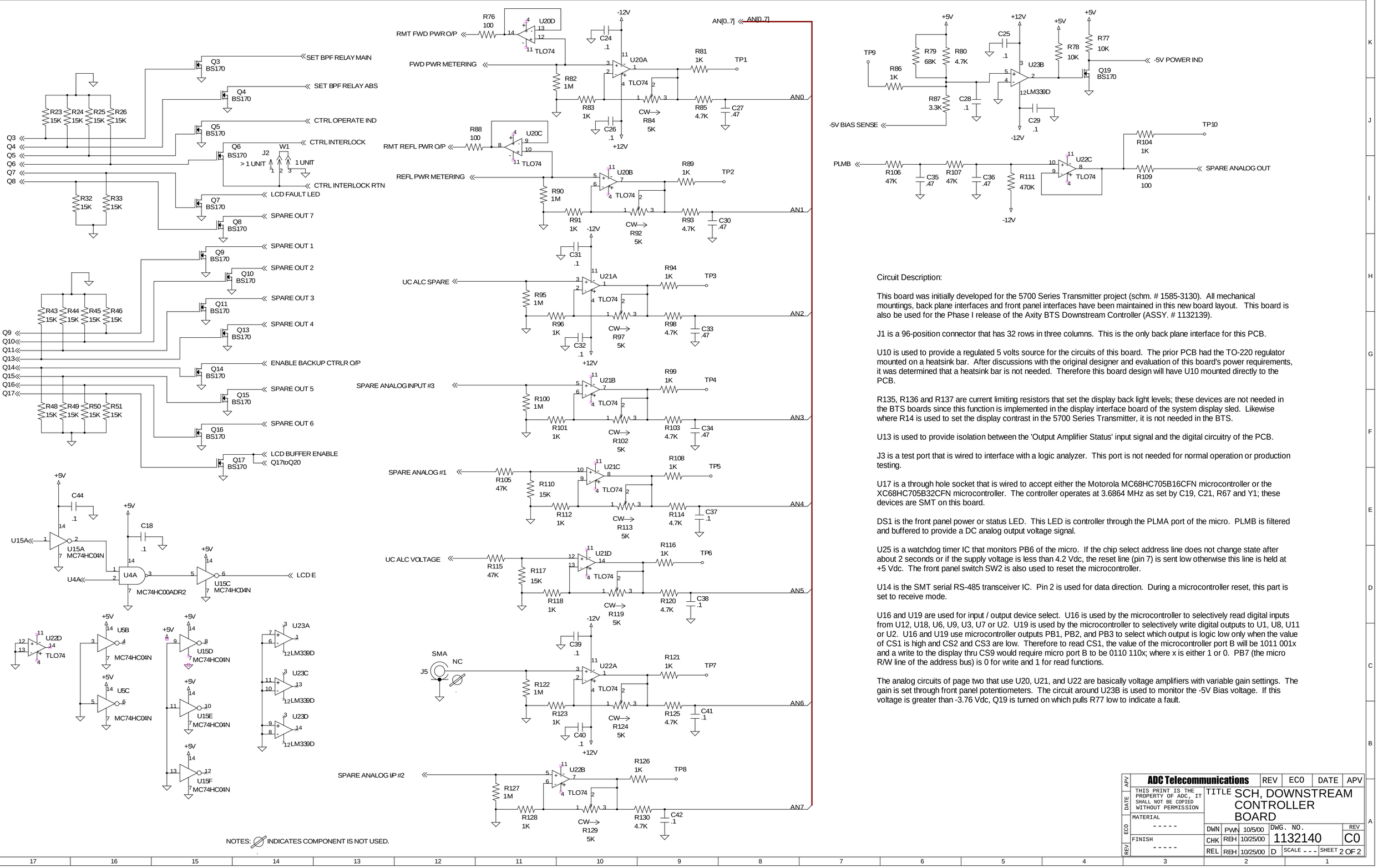
MATERIAL -----

FINISH -----

TITLE SCH, DOWNSTREAM CONTROLLER BOARD

DWN	PWN	10/5/00	DWG. NO. 1132140 REV C0
CHK	REH	10/25/00	
REL	REH	10/25/00	D SCALE --- SHEET 1 OF 2



Circuit Description:

This board was initially developed for the 5700 Series Transmitter project (schm. # 1585-3130). All mechanical mountings, back plane interfaces and front panel interfaces have been maintained in this new board layout. This board is also be used for the Phase I release of the Axity BTS Downstream Controller (ASSY. # 1132139).

J1 is a 96-position connector that has 32 rows in three columns. This is the only back plane interface for this PCB.

U10 is used to provide a regulated 5 volts source for the circuits of this board. The prior PCB had the TO-220 regulator mounted on a heatsink bar. After discussions with the original designer and evaluation of this board's power requirements, it was determined that a heatsink bar is not needed. Therefore this board design will have U10 mounted directly to the PCB.

R135, R136 and R137 are current limiting resistors that set the display back light levels; these devices are not needed in the BTS boards since this function is implemented in the display interface board of the system display sled. Likewise where R14 is used to set the display contrast in the 5700 Series Transmitter, it is not needed in the BTS.

U13 is used to provide isolation between the 'Output Amplifier Status' input signal and the digital circuitry of the PCB.

J3 is a test port that is wired to interface with a logic analyzer. This port is not needed for normal operation or production testing.

U17 is a through hole socket that is wired to accept either the Motorola MC68HC705B16CFN microcontroller or the XC68HC705B32CFN microcontroller. The controller operates at 3.6864 MHz as set by C19, C21, R67 and Y1; these devices are SMT on this board.

DS1 is the front panel power or status LED. This LED is controller through the PLMA port of the micro. PLMB is filtered and buffered to provide a DC analog output voltage signal.

U25 is a watchdog timer IC that monitors PB6 of the micro. If the chip select address line does not change state after about 2 seconds or if the supply voltage is less than 4.2 Vdc, the reset line (pin 7) is sent low otherwise this line is held at +5 Vdc. The front panel switch SW2 is also used to reset the microcontroller.

U14 is the SMT serial RS-485 transceiver IC. Pin 2 is used for data direction. During a microcontroller reset, this part is set to receive mode.

U16 and U19 are used for input / output device select. U16 is used by the microcontroller to selectively read digital inputs from U12, U18, U6, U9, U3, U7 or U2. U19 is used by the microcontroller to selectively write digital outputs to U1, U8, U11 or U2. U16 and U19 use microcontroller outputs PB1, PB2, and PB3 to select which output is logic low only when the value of CS1 is high and CS2 and CS3 are low. Therefore to read CS1, the value of the microcontroller port B will be 1011 001x and a write to the display thru CS9 would require micro port B to be 0110 110x; where x is either 1 or 0. PB7 (the micro R/W line of the address bus) is 0 for write and 1 for read functions.

The analog circuits of page two that use U20, U21, and U22 are basically voltage amplifiers with variable gain settings. The gain is set through front panel potentiometers. The circuit around U23B is used to monitor the -5V Bias voltage. If this voltage is greater than -3.76 Vdc, Q19 is turned on which pulls R77 low to indicate a fault.

APV	ADC Telecommunications	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE	SCH, DOWNSTREAM CONTROLLER BOARD		
ECO	MATERIAL -----	DWN	PWN 10/5/00	DWG. NO. 1132140	REV C0
REV	FINISH -----	CHK	REH 10/25/00		
		REL	REH 10/25/00	D SCALE ---	SHEET 2 OF 2

J1A
913289
1A UNUSED IN 1
2A UNUSED IN 2
3A UNUSED OUT 1
4A UNUSED IN 3
5A UNUSED OUT 2
6A UNUSED OUT 3
7A UNUSED OUT 4
8A ≪ SPARE ANALOG IN 1
9A SYSTEM PS STATUS1
10A SYSTEM PS STATUS2
11A ≪ SPARE ANALOG IN 2
12A
13A ≪ SPARE ANALOG IN 3
14A
15A
16A
17A LNA INTERLOCK S1
18A ≪ SPARE ANALOG IN 4
19A DC DISABLE S5
20A LNA INTERLOCK S2
21A LNA INTERLOCK S3
22A LNA INTERLOCK S4
23A ≪ SPARE ANALOG OUT 1
24A DC INTERLOCK S4
25A DS SW INTERLOCK
26A
27A
28A
29A
30A
31A
32A PS 2 LOAD ENABLE

J1B
913289
1B PS 3 LOAD ENABLE
2B ≪ ABS BACKUP ENABLE S1
3B DC INTERLOCK S2
4B ≪ ABS BACKUP ENABLE S2
5B CTRL INTERLOCK S3
6B ≪ ABS INTERLOCK RTN
7B ≪ ABS INTERLOCK
8B CTRL INTERLOCK S4
9B CTRL INTERLOCK S5
10B ≪ ABS BACKUP ENABLE S3
11B CTRL OPERATE INDICATOR S5
12B ≪ SPARE ANALOG IN 5
13B ≪ SPARE ANALOG IN 6
14B DC INTERLOCK S3
15B TX SW INTERLOCK
16B
17B ≪ DC DISABLE S1
18B ≪ DC DISABLE S2
19B ≪ RMT ANALOGO/P 1
20B ≪ RMT ANALOGO/P 2
21B ≪ DC DISABLE S3
22B ≪ DC DISABLE S4
23B ≪ DS SWITCH POS 1
24B ≪ DS SWITCH POS 2
25B ≪ US SWITCH POS 1
26B ≪ US SWITCH POS 2
27B US SWITCH INTERLOCK
28B PS1 LOAD ENABLE
29B ≪ SPARE ANALOG IN 7
30B UNUSED IN 4
31B UNUSED IN 5
32B ≪ SPARE ANALOG IN 8

J1C
913289
1C
2C ≪ ABS BACKUP ENABLE S4
3C
4C ≪ DISABLE BACKUP
5C S5 (NOT USED)
6C S4 (NOT USED)
7C S3 (NOT USED)
8C S2 (NOT USED)
9C S1 (NOT USED)
10C
11C
12C CONTRAST (NOT USED)
13C LCD RS (NOT USED)
14C LCD R/W (NOT USED)
15C ≪ LCD E (NOT USED)
16C DB0 (NOT USED)
17C DB1 (NOT USED)
18C DB2 (NOT USED)
19C DB3 (NOT USED)
20C DB4 (NOT USED)
21C DB5 (NOT USED)
22C DB6 (NOT USED)
23C DB7 (NOT USED)
24C
25C
26C SERIAL +
27C
28C SERIAL -
29C DC INTERLOCK S1
30C DC INTERLOCK S5
31C CTRL INTERLOCK S1
32C CTRL INTERLOCK S2

J3
1 /DS
2 R/W
3 A5
4 A4
5 A3
6 A2
7 A1
8 A0
9 D7
10 D6
11 D5
12 D4
13 D3
14 D2
15 D1
16 D0
TEST INTERFACE

R1 220
R2 220
R4 10K
R5 10K
R6 10K
R7 10K
R8 10K
R9 10K
R10 10K
R11 10K
R12 10K
R14 5K
R19 10K
R20 10K
R21 10K
R22 10K
R28 10K
R29 10K
R30 10K
R31 10K
R34 10K
R35 10K
R36 10K
R37 10K
R40 10K
R41 10K
R42 10K
R52 10K
R53 10K
R54 10K
R55 10K
R56 10K
R58 10K
R59 10K
R60 10K
R61 10K
R62 10K
R63 10K
R64 10K
R65 10K
R66 10K
R68 10K
R69 10K
R70 10K
R71 10K
R72 10K
R74 10K
R75 220
R131 10K
R132 10K
R133 10K
R134 10K
R135 100/1W
R136 100/1W
R137 100/1W
R138 10K
R139 6.8K
R140 2.87K
R57 220
R27 10K
R3 15K
R13 15K

C1 .1
C2 .1
C3 .1
C4 47 20V
C5 .1
C6 .1
C7 .1
C8 .1
C9 .1
C10 47 20V
C11 47 20V
C12 47 20V
C13 .1
C14 .1
C15 .1
C16 .47
C17 .1
C19 33 PF 50V
C20 .1
C21 33 PF 50V
C23 .01
C43 .1

SW1
Y1 3.6864 MHZ
SW2 WT15L2SV-1QE
DS1 5300H5 Default
Q18 BS170
Q1 BS170
Q2 BS170
Q20 BS170
Q17toQ20
J6
J7
J8
OPTO ISOLATOR

U1 SN74H377DW
U2 MC74HC245ADW
U3 MC74HC245ADW
U4A MC74HC00ADR2
U4B MC74HC00ADR2
U4C MC74HC00ADR2
U5A MC74HC04N
U5B MC74HC04N
U5D MC74HC04N
U5E MC74HC04N
U5F MC74HC04N
U6 MC74HC245ADW
U7 MC74HC245ADW
U8 SN74H377DW
U9 MC74HC245ADW
U10 MC7805CT
U11 SN74H377DW
U12 MC74HC245ADW
U13
U14 2-61100-4472
U15A
U16 MC74HC138A
U17 MC68HC705B16CFN
U18 MC74HC245ADW
U19 MC74HC138A
U25 1095823

DB0 (NOT USED)
DB1 (NOT USED)
DB2 (NOT USED)
DB3 (NOT USED)
DB4 (NOT USED)
DB5 (NOT USED)
DB6 (NOT USED)
DB7 (NOT USED)
R/W
/CS9
S1 (NOT USED)
S2 (NOT USED)
S3 (NOT USED)
S4 (NOT USED)
S5 (NOT USED)
/CS2
DC INTERLOCK S1
DC INTERLOCK S2
DC INTERLOCK S3
DC INTERLOCK S4
DC INTERLOCK S5
TX SW INTERLOCK
DS SW INTERLOCK
/CS5
CTRL INTERLOCK S1
CTRL INTERLOCK S2
CTRL INTERLOCK S3
CTRL INTERLOCK S4
CTRL INTERLOCK S5
CTRL OPERATE INDICATOR S5
/CS3
UNUSED IN 4
UNUSED IN 1
UNUSED IN 5
-5V POWER IND
UNUSED IN 3
SYSTEM PS STATUS1
SYSTEM PS STATUS2
UNUSED IN 2
/CS0
LNA INTERLOCK S1
LNA INTERLOCK S2
LNA INTERLOCK S3
LNA INTERLOCK S4
US SWITCH INTERLOCK
PS 1 LOAD ENABLE
PS 2 LOAD ENABLE
PS 3 LOAD ENABLE
/CS1
AN[0..7]
AN7
AN6
AN5
AN4
AN3
AN2
AN1
AN0
SERIAL -
SERIAL +
A[0..5]
D[0..7]
/CS[0..9]
/CS4
/CS6
/CS7
/CS8
UNUSED OUT 2
UNUSED OUT 3
UNUSED OUT 4
DC DISABLE S5
UNUSED OUT 1
LCD R/W (NOT USED)
LCD RS (NOT USED)
PLMB
U15A

REMOVED DO NOT INSTALL SYMBOLS ON SPECIFIED PARTS. PWN

C0	20085157	03/19/01	REH
ADD PARTS: Q20, CHANGE C19, C21, Y1, AND R67 TO SMT PARTS. CHANGE U14 PART NUMBER. ADD U25 (1095823), R139 (6.8K), AND R140 (2.87K). DELETE R73 AND C22. FIX LINES 7 AND 8 ON U14. PWN			
B0	20079417	01/15/01	REH

ADC Telecommunications

REV	EC0	DATE	APV

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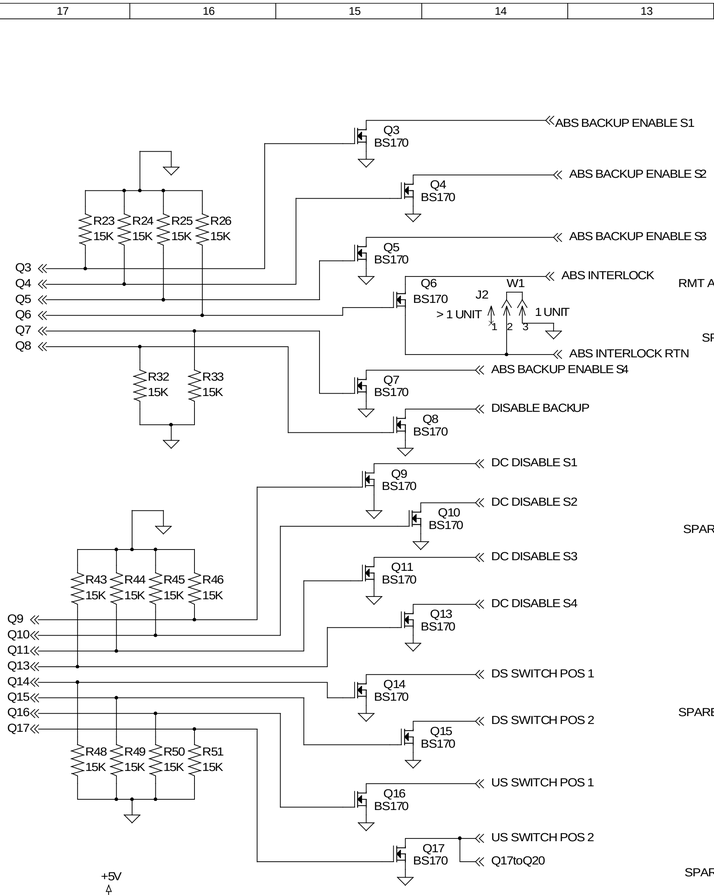
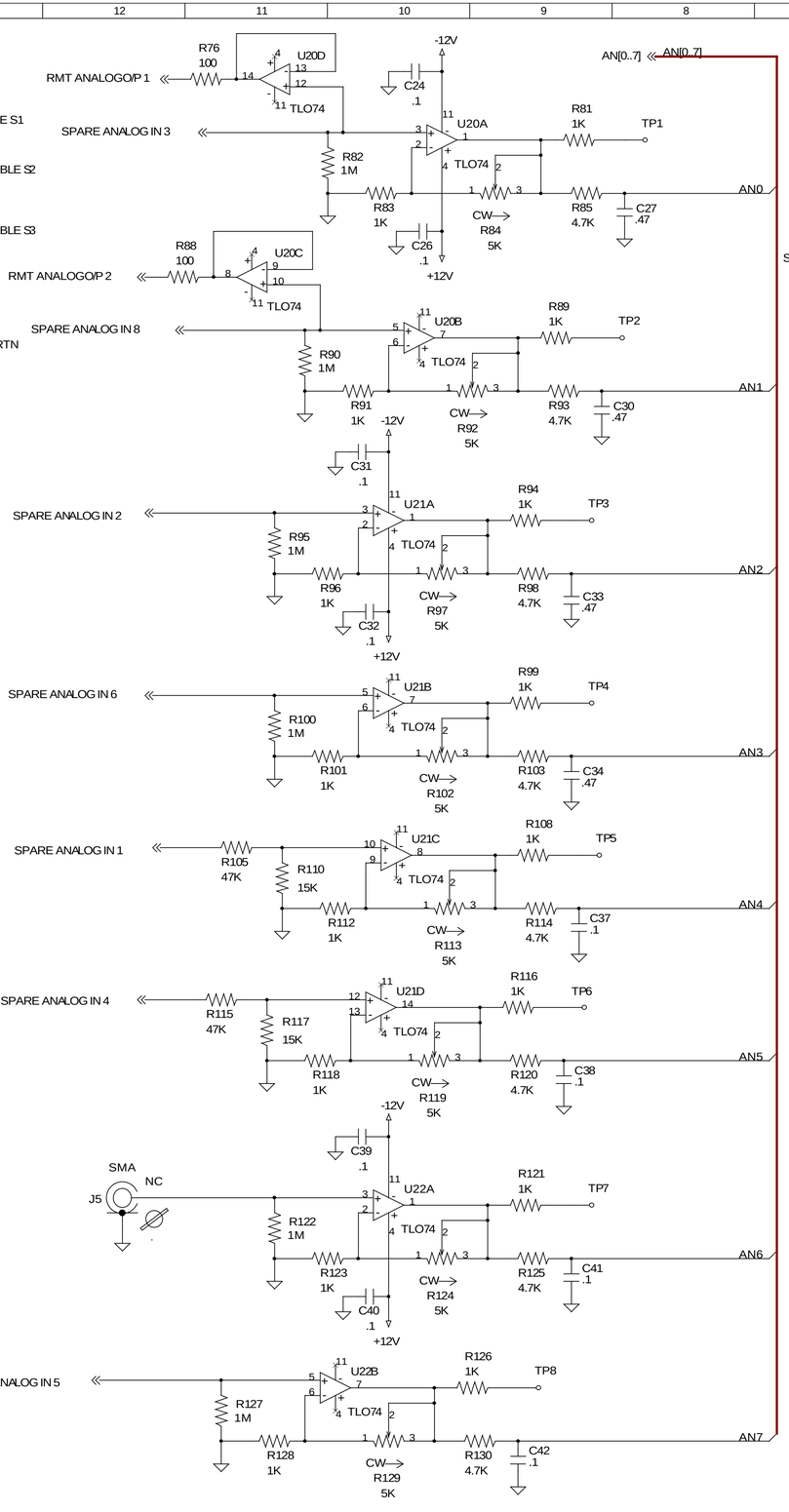
MATERIAL ------

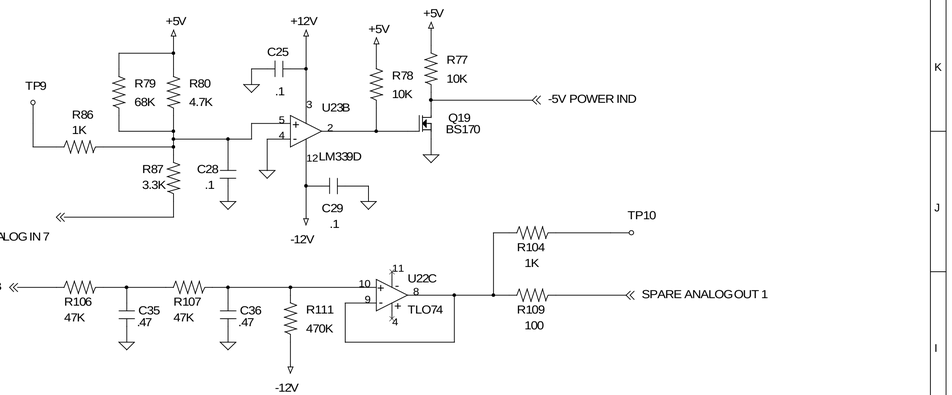
FINISH ------

TITLE SCH, ABS CONTROLLER BOARD

DWN	PWN	9/26/00	DWG. NO.		REV
CHK	REH	10/10/00	1132142		C0
REL	REH	10/10/00	D	SCALE ---	SHEET 1 OF 2







Circuit Description:

This board was initially developed for the 5700 Series Transmitter project (schm. # 1585-3130). All mechanical mountings, back plane interfaces and front panel interfaces have been maintained in this new board layout. This board is also be used for the Phase I release of the Axity BTS and ABS Sleds (ASSY. # 1132141).

J1 is a 96-position connector that has 32 rows in three columns. This is the only back plane interface for this PCB.

U10 is used to provide a regulated 5 volts source for the circuits of this board. The prior PCB had the TO-220 regulator mounted on a heatsink bar. After discussions with the original designer and evaluation of this board's power requirements, it was determined that a heatsink bar is not needed. Therefore this board design will have U10 mounted directly to the PCB.

R135, R136 and R137 are current limiting resistors that set the display back light levels; these devices are not needed in the BTS boards since this function is implemented in the display interface board of the system display sled. Likewise where R14 is used to set the display contrast in the 5700 Series Transmitter, it is not needed in the BTS.

U13 is used to provide isolation between the 'Output Amplifier Status' input signal and the digital circuitry of the PCB.

J3 is a test port that is wired to interface with a logic analyzer. This port is not needed for normal operation or production testing.

U17 is a through hole socket that is wired to accept either the Motorola MC68HC705B16CFN microcontroller or the XC68HC705B32CFN microcontroller. The controller operates at 3.6864 MHz as set by C19, C21, R67 and Y1; these devices are SMT on this board.

DS1 is the front panel power or status LED. This LED is controller through the PLMA port of the micro. PLMB is filtered and buffered to provide a DC analog output voltage signal.

U25 is a watchdog timer IC that monitors PB6 of the micro. If the chip select address line does not change state after about 2 seconds or if the supply voltage is less than 4.2 Vdc, the reset line (pin 7) is sent low otherwise this line is held at +5 Vdc. The front panel switch SW2 is also used to reset the microcontroller.

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The analog circuits of page two that use U20, U21, and U22 are basically voltage amplifiers with variable gain settings. The gain is set through front panel potentiometers. The circuit around U23B is used to monitor the -5V Bias voltage. If this voltage is greater than -3.76 Vdc, Q19 is turned on which pulls R77 low to indicate a fault.

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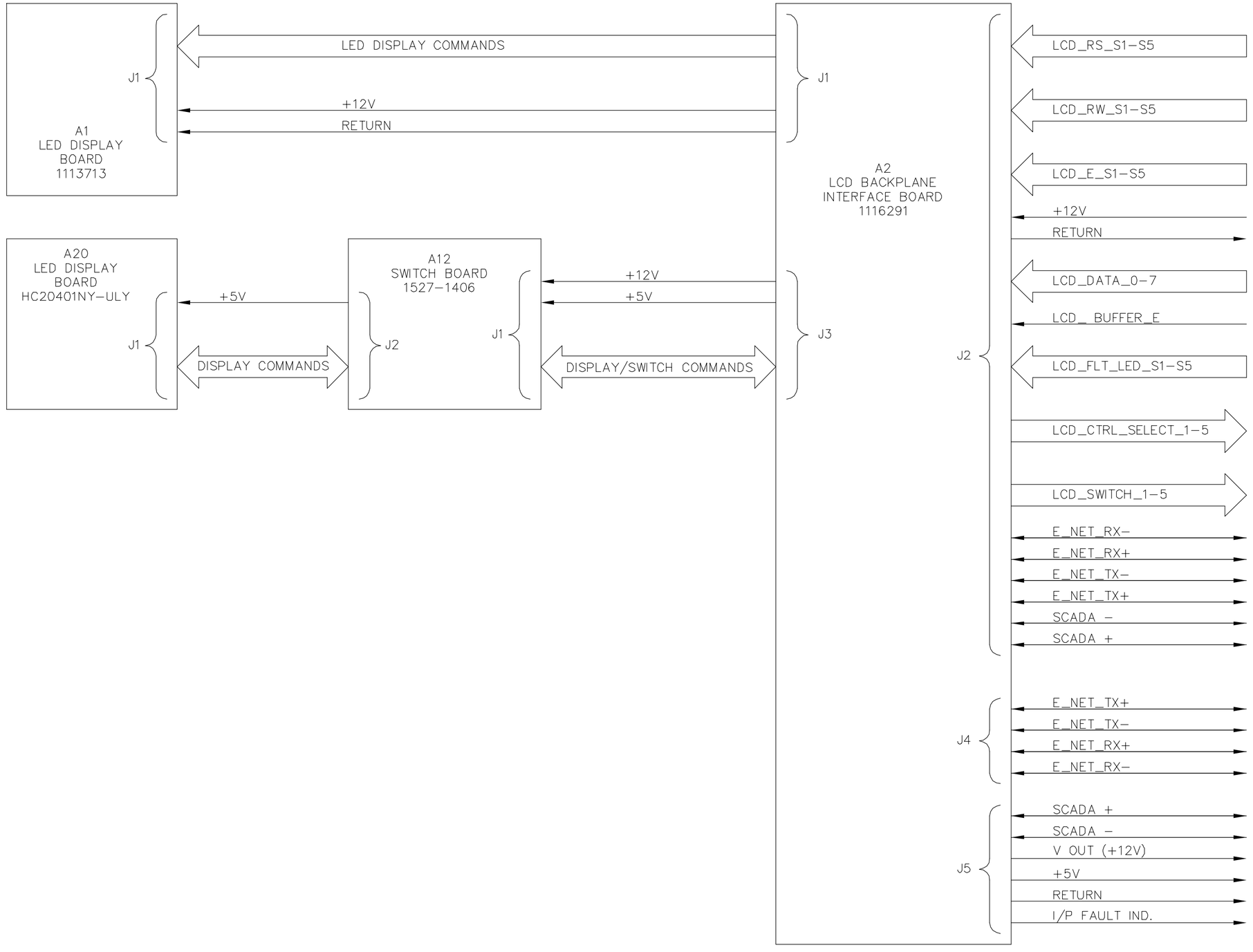
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE	SCH, ABS CONTROLLER BOARD		
ECO	MATERIAL -----	DWN	PWN 9/26/00	DWG. NO.	REV
REV	FINISH -----	CHK	REH 10/10/00	1132142	C0
		REL	REH 10/10/00	D SCALE ---	SHEET 2 OF 2



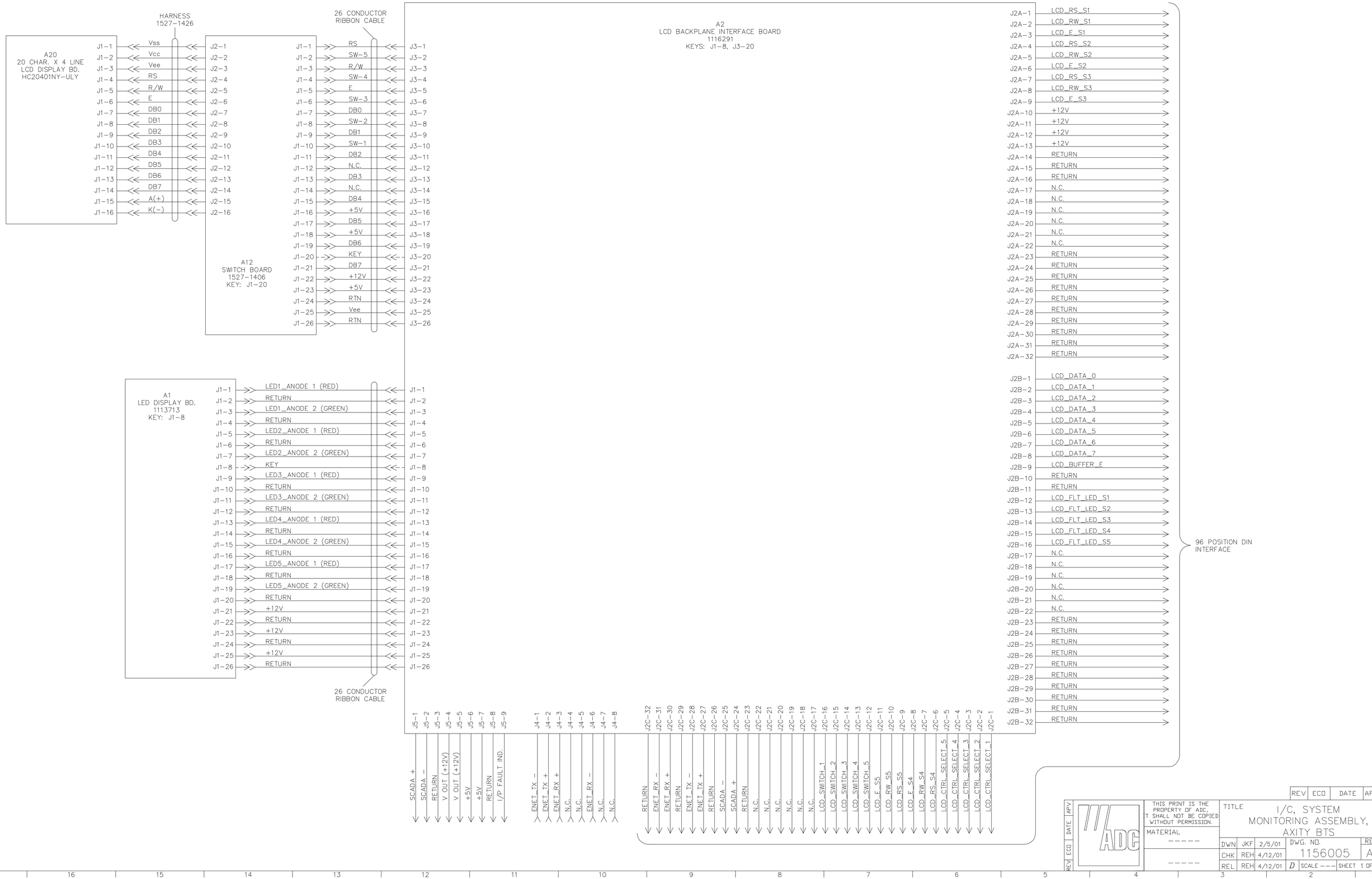
REV	ECO	DATE	APV

MATERIAL

FINISH

TITLE: B/D, SYSTEM MONITORING ASSY, AXITY BTS

			DWG. NO.	REV
DWN	JKF	2/7/01	1156006	A0
CHK	REH	4/12/01		
REL	REH	4/12/01	C SCALE ---	SHEET 1 OF 1

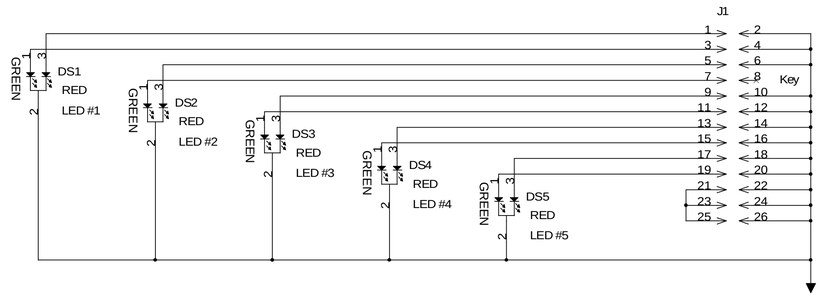


REV	ECO	DATE	APV

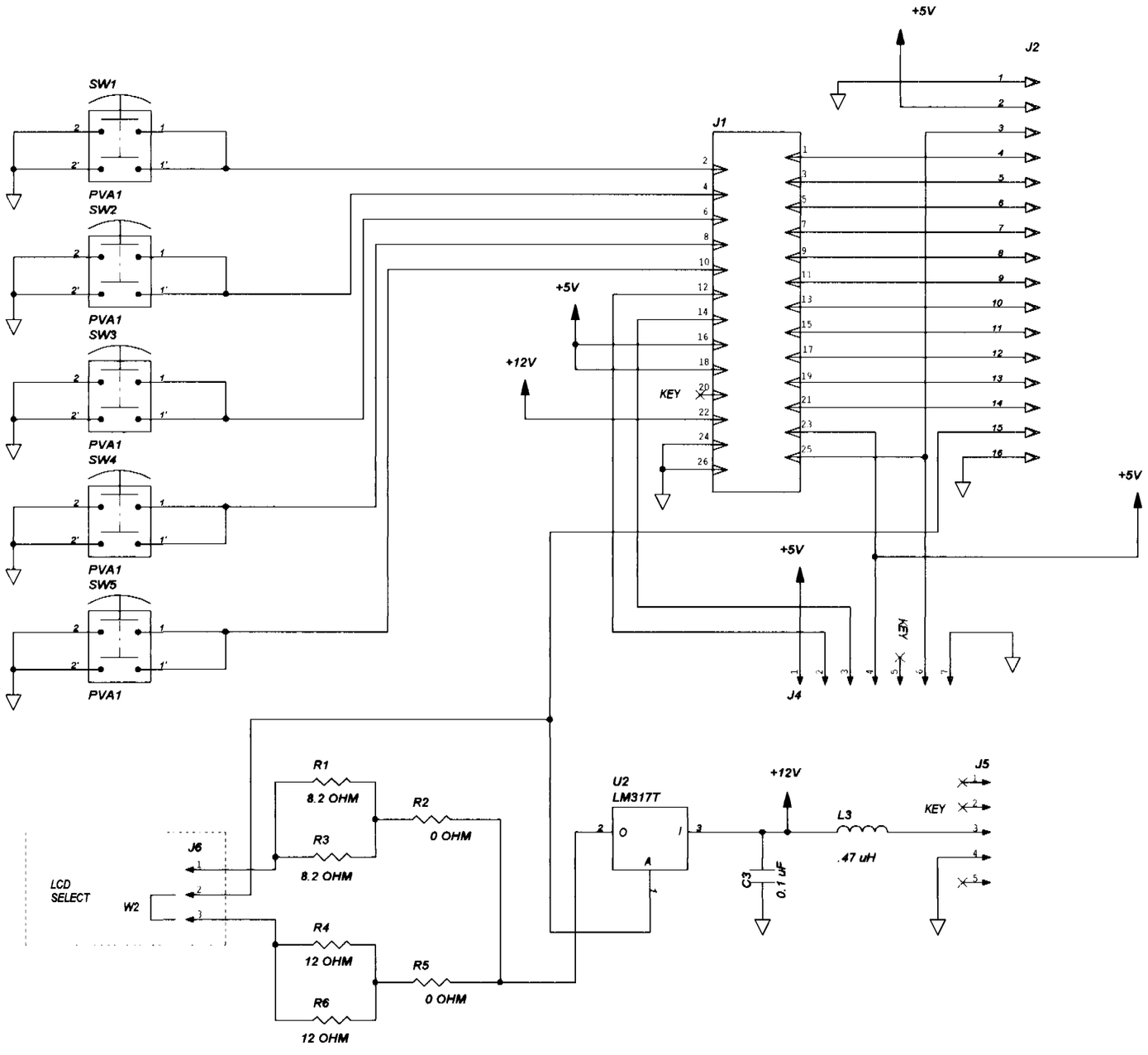
MATERIAL

TITLE: I/C, SYSTEM MONITORING ASSEMBLY, AXITY BTS

DWN	JKF	2/5/01	DWG. NO. 1156005 REV A0
CHK	REH	4/12/01	
REL	REH	4/12/01	D SCALE --- SHEET 1 OF 1



APV	**ADC Telecommunications**	REV	ECO	DATE	APV	
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE	SCH., BWA 2000 FRONT PANEL BD. {1113713}			
ECO	MATERIAL -----	DWN	PWN	6/9/00	DWG. NO. 1113710	REV A0
REV	FINISH -----	CHK	REH	6/9/00		
		REL	REH	6/9/00	D	SCALE - - - SHEET 1 OF 1



DELETED C1, C2, L1, L2, U1, J3, & W1. MOVED W2 FROM J6-1,-2 TO J6 -2,-3. JKF

REV	ECN	DATE	APV
3	8603	11/7/96	RAS
AT J2 W2 WAS W1. (TMY)			
2	8424	9/29/96	JCM
SWITCHED PINS 1 & 2 OF U2. (TMY)			
1	8368	8/27/96	RAS

ITS CORPORATION

MATERIAL ---

FINISH ---

TITLE SCHEMATIC SWITCH BOARD (1527-1406)

DWN	DLM	6/3/96	
CHK	RAS	6/14/96	
REL	RAS	6/14/96	

DWG. NO. 1527-3406 REV 3

B SCALE --- SHEET 1 OF 1

J1A — Sector 1 Control Card F1

PA_Interlock_S1	1A	
PA_PS_Good_S1	2A	
PA_PS_Enable_S1	3A	
PA_Oper_Rqst_S1	4A	
	5A	
	6A	
	7A	
	8A	
System_PS_Stat_1	9A	
System_PS_Stat_2	10A	
UC_ALC_S1	11A	
	12A	
PA_Frw_Pwr_S1	13A	
System_+12Vdc	14A	
	15A	
System_-12Vdc	16A	
UC_Interlock_S1	17A	
UC_ALC_S1	18A	
UC_Mute_Cmd_S1	19A	
UC_Mute_Ind_S1	20A	
UC_Input_Flt_S1	21A	
UC_Ref_Flt_S1	22A	
	23A	
LCD_Ctrl_Select_2	24A	
LCD_Ctrl_Select_5	25A	
	26A	
	27A	
	28A	
	29A	
	30A	
	31A	
UC_PLL_Flt_S1	32A	913642
BPF_Interlock_S1	1B	J1B
BPF_Rly_Main_S1	2B	
BPF_Rly_Pos_S1	3B	
BPF_Rly_ABS_S1	4B	
	5B	
	6B	
Ctrl_Interlock_S1	7B	
PS1_LoadE	8B	
PS2_LoadE	9B	
Ctrl_Oper_Ind_S1	10B	
PS3_LoadE	11B	
	12B	
	13B	
LCD_Ctrl_Select_1	14B	
LCD_Ctrl_Select_4	15B	
	16B	
	17B	
	18B	
	19B	
	20B	
	21B	
	22B	
En_Bkup_Ctrlr	23B	
	24B	
	25B	
LCD_Buffer_E	26B	
ABS_Bkup_E_S1	27B	
	28B	
PA_BiasVdc_S1	29B	
PA_Output_Stat_S1	30B	
PA_Temp_Stat_S1	31B	
PA_Rfl_Pwr_S1	32B	913642
	1C	J1C
LCD_Flt_LED_S1	2C	
	3C	
	4C	
LCD_Switch_5	5C	
LCD_Switch_4	6C	
LCD_Switch_3	7C	
LCD_Switch_2	8C	
LCD_Switch_1	9C	
	10C	
	11C	
	12C	
LCD_RS_S1	13C	
LCD_RW_S1	14C	
LCD_E_S1	15C	
LCD_Data_0	16C	
LCD_Data_1	17C	
LCD_Data_2	18C	
LCD_Data_3	19C	
LCD_Data_4	20C	
LCD_Data_5	21C	
LCD_Data_6	22C	
LCD_Data_7	23C	
	24C	
	25C	
SCADA_S+	26C	
	27C	
SCADA_S-	28C	
	29C	
LCD_Ctrl_Select_3	30C	
Slot ID 001	31C	
	32C	913642

J2A — Sector 2 Control Card F2

PA_Interlock_S2	1A	
PA_PS_Good_S2	2A	
PA_PS_Enable_S2	3A	
PA_Oper_Rqst_S2	4A	
	5A	
	6A	
	7A	
	8A	
System_PS_Stat_1	9A	
System_PS_Stat_2	10A	
UC_ALC_S2	11A	
	12A	
PA_Frw_Pwr_S2	13A	
System_+12Vdc	14A	
	15A	
System_-12Vdc	16A	
UC_Interlock_S2	17A	
UC_ALC_S2	18A	
UC_Mute_Cmd_S2	19A	
UC_Mute_Ind_S2	20A	
UC_Input_Flt_S2	21A	
UC_Ref_Flt_S2	22A	
	23A	
LCD_Ctrl_Select_2	24A	
LCD_Ctrl_Select_5	25A	
	26A	
	27A	
	28A	
	29A	
	30A	
	31A	
UC_PLL_Flt_S2	32A	913642
BPF_Interlock_S2	1B	J2B
BPF_Rly_Main_S2	2B	
BPF_Rly_Pos_S2	3B	
BPF_Rly_ABS_S2	4B	
	5B	
	6B	
Ctrl_Interlock_S2	7B	
PS1_LoadE	8B	
PS2_LoadE	9B	
Ctrl_Oper_Ind_S2	10B	
PS3_LoadE	11B	
	12B	
	13B	
LCD_Ctrl_Select_1	14B	
LCD_Ctrl_Select_4	15B	
	16B	
	17B	
	18B	
	19B	
	20B	
	21B	
	22B	
En_Bkup_Ctrlr	23B	
	24B	
	25B	
LCD_Buffer_E	26B	
ABS_Bkup_E_S2	27B	
	28B	
PA_BiasVdc_S2	29B	
PA_Output_Stat_S2	30B	
PA_Temp_Stat_S2	31B	
PA_Rfl_Pwr_S2	32B	913642
	1C	J2C
LCD_Flt_LED_S2	2C	
	3C	
	4C	
LCD_Switch_5	5C	
LCD_Switch_4	6C	
LCD_Switch_3	7C	
LCD_Switch_2	8C	
LCD_Switch_1	9C	
	10C	
	11C	
	12C	
LCD_RS_S2	13C	
LCD_RW_S2	14C	
LCD_E_S2	15C	
LCD_Data_0	16C	
LCD_Data_1	17C	
LCD_Data_2	18C	
LCD_Data_3	19C	
LCD_Data_4	20C	
LCD_Data_5	21C	
LCD_Data_6	22C	
LCD_Data_7	23C	
	24C	
	25C	
SCADA_S+	26C	
	27C	
SCADA_S-	28C	
	29C	
LCD_Ctrl_Select_3	30C	
Slot ID 010	31C	
	32C	913642

J3A — Sector 3 Control Card F3

PA_Interlock_S3	1A	
PA_PS_Good_S3	2A	
PA_PS_Enable_S3	3A	
PA_Oper_Rqst_S3	4A	
	5A	
	6A	
	7A	
	8A	
System_PS_Stat_1	9A	
System_PS_Stat_2	10A	
UC_ALC_S3	11A	
	12A	
PA_Frw_Pwr_S3	13A	
System_+12Vdc	14A	
	15A	
System_-12Vdc	16A	
UC_Interlock_S3	17A	
UC_ALC_S3	18A	
UC_Mute_Cmd_S3	19A	
UC_Mute_Ind_S3	20A	
UC_Input_Flt_S3	21A	
UC_Ref_Flt_S3	22A	
	23A	
LCD_Ctrl_Select_2	24A	
LCD_Ctrl_Select_5	25A	
	26A	
	27A	
	28A	
	29A	
	30A	
	31A	
UC_PLL_Flt_S3	32A	913642
BPF_Interlock_S3	1B	J3B
BPF_Rly_Main_S3	2B	
BPF_Rly_Pos_S3	3B	
BPF_Rly_ABS_S3	4B	
	5B	
	6B	
Ctrl_Interlock_S3	7B	
PS1_LoadE	8B	
PS2_LoadE	9B	
Ctrl_Oper_Ind_S3	10B	
PS3_LoadE	11B	
	12B	
	13B	
LCD_Ctrl_Select_1	14B	
LCD_Ctrl_Select_4	15B	
	16B	
	17B	
	18B	
	19B	
	20B	
	21B	
	22B	
En_Bkup_Ctrlr	23B	
	24B	
	25B	
LCD_Buffer_E	26B	
ABS_Bkup_E_S3	27B	
	28B	
PA_BiasVdc_S3	29B	
PA_Output_Stat_S3	30B	
PA_Temp_Stat_S3	31B	
PA_Rfl_Pwr_S3	32B	913642
	1C	J3C
LCD_Flt_LED_S3	2C	
	3C	
	4C	
LCD_Switch_5	5C	
LCD_Switch_4	6C	
LCD_Switch_3	7C	
LCD_Switch_2	8C	
LCD_Switch_1	9C	
	10C	
	11C	
	12C	
LCD_RS_S3	13C	
LCD_RW_S3	14C	
LCD_E_S3	15C	
LCD_Data_0	16C	
LCD_Data_1	17C	
LCD_Data_2	18C	
LCD_Data_3	19C	
LCD_Data_4	20C	
LCD_Data_5	21C	
LCD_Data_6	22C	
LCD_Data_7	23C	
	24C	
	25C	
SCADA_S+	26C	
	27C	
SCADA_S-	28C	
	29C	
LCD_Ctrl_Select_3	30C	
Slot ID 011	31C	
	32C	913642

J4A — Sector 4 Control Card F4

PA_Interlock_S4	1A	
PA_PS_Good_S4	2A	
PA_PS_Enable_S4	3A	
PA_Oper_Rqst_S4	4A	
	5A	
	6A	
	7A	
	8A	
System_PS_Stat_1	9A	
System_PS_Stat_2	10A	
UC_ALC_S4	11A	
	12A	
PA_Frw_Pwr_S4	13A	
System_+12Vdc	14A	
	15A	
System_-12Vdc	16A	
UC_Interlock_S4	17A	
UC_ALC_S4	18A	
UC_Mute_Cmd_S4	19A	
UC_Mute_Ind_S4	20A	
UC_Input_Flt_S4	21A	
UC_Ref_Flt_S4	22A	
	23A	
LCD_Ctrl_Select_2	24A	
LCD_Ctrl_Select_5	25A	
	26A	
	27A	
	28A	
	29A	
	30A	
	31A	
UC_PLL_Flt_S4	32A	913642
BPF_Interlock_S4	1B	J4B
BPF_Rly_Main_S4	2B	
BPF_Rly_Pos_S4	3B	
BPF_Rly_ABS_S4	4B	
	5B	
	6B	
Ctrl_Interlock_S4	7B	
PS1_LoadE	8B	
PS2_LoadE	9B	
Ctrl_Oper_Ind_S4	10B	
PS3_LoadE	11B	
	12B	
	13B	
LCD_Ctrl_Select_1	14B	
LCD_Ctrl_Select_4	15B	
	16B	
	17B	
	18B	
	19B	
	20B	
	21B	
	22B	
En_Bkup_Ctrlr	23B	
	24B	
	25B	
LCD_Buffer_E	26B	
ABS_Bkup_E_S4	27B	
	28B	
PA_BiasVdc_S4	29B	
PA_Output_Stat_S4	30B	
PA_Temp_Stat_S4	31B	
PA_Rfl_Pwr_S4	32B	913642
	1C	J4C
LCD_Flt_LED_S4	2C	
	3C	
	4C	
LCD_Switch_5	5C	
LCD_Switch_4	6C	
LCD_Switch_3	7C	
LCD_Switch_2	8C	
LCD_Switch_1	9C	
	10C	
	11C	
	12C	
LCD_RS_S4	13C	
LCD_RW_S4	14C	
LCD_E_S4	15C	
LCD_Data_0	16C	
LCD_Data_1	17C	
LCD_Data_2	18C	
LCD_Data_3	19C	
LCD_Data_4	20C	
LCD_Data_5	21C	
LCD_Data_6	22C	
LCD_Data_7	23C	
	24C	
	25C	
SCADA_S+	26C	
	27C	
SCADA_S-	28C	
	29C	
LCD_Ctrl_Select_3	30C	
Slot ID 100	31C	
	32C	913642

J5A — Back-Up Control Card F5

PA_Interlock_S5	1A	
PA_PS_Good_S5	2A	
PA_PS_Enable_S5	3A	
PA_Oper_Rqst_S5	4A	
	5A	
	6A	
	7A	
	8A	
System_PS_Stat_1	9A	
System_PS_Stat_2	10A	
UC_ALC_S5	11A	
	12A	
PA_Frw_Pwr_S5	13A	
System_+12Vdc	14A	
	15A	
System_-12Vdc	16A	
UC_Interlock_S5	17A	
UC_ALC_S5	18A	
UC_Mute_Cmd_S5	19A	
UC_Mute_Ind_S5	20A	
UC_Input_Flt_S5	21A	
UC_Ref_Flt_S5	22A	
	23A	
LCD_Ctrl_Select_2	24A	
LCD_Ctrl_Select_5	25A	
	26A	
	27A	
	28A	
	29A	
	30A	
	31A	
UC_PLL_Flt_S5	32A	913642
	1B	J5B
	2B	
	3B	
	4B	
	5B	
	6B	
Ctrl_Interlock_S5	7B	
PS1_LoadE	8B	
PS2_LoadE	9B	
Ctrl_Oper_Ind_S5	10B	
PS3_LoadE	11B	
	12B	
	13B	
LCD_Ctrl_Select_1	14B	
LCD_Ctrl_Select_4	15B	
	16B	
	17B	
	18B	
	19B	
	20B	
	21B	
	22B	
None:One controller enables back-up	23B	
	24B	
	25B	
LCD_Buffer_E	26B	
	27B	
En_Bkup_Ctrl	28B	
PA_BiasVdc_S5	29B	
PA_Output_Stat_S5	30B	
PA_Temp_Stat_S5	31B	
PA_Rfl_Pwr_S5	32B	913642
	1C	J5C
LCD_Flt_LED_S5	2C	
	3C	
	4C	
LCD_Switch_5	5C	
LCD_Switch_4	6C	
LCD_Switch_3	7C	
LCD_Switch_2	8C	
LCD_Switch_1	9C	
	10C	
	11C	
	12C	
LCD_RS_S5	13C	
LCD_RW_S5	14C	
LCD_E_S5	15C	
LCD_Data_0	16C	
LCD_Data_1	17C	
LCD_Data_2	18C	
LCD_Data_3	19C	
LCD_Data_4	20C	
LCD_Data_5	21C	
LCD_Data_6	22C	
LCD_Data_7	23C	
	24C	
	25C	
SCADA_S+	26C	
	27C	
SCADA_S-	28C	
Disable_Bkup_Ctrl	29C	
LCD_Ctrl_Select_3	30C	
Slot ID 101	31C	
	32C	913642

J6A — ABS Control Card F6 Slot ID 110

Slot ID #1	1A	
	2A	
	3A	
Slot ID #3	4A	
	5A	
	6A	
	7A	
	8A	
System_PS_Stat_1	9A	
System_PS_Stat_2	10A	
	11A	
	12A	
System_+12Vdc	13A	
	14A	
System_-12Vdc	15A	
LNA_Interlock_S1	16A	
	17A	
DC_Disable_S5	18A	
LNA_Interlock_S2	19A	
LNA_Interlock_S3	20A	
LNA_Interlock_S4	21A	
	22A	
DC_Interlock_S4	23A	
DS_SW_Interlock	24A	
	25A	
	26A	
	27A	
	28A	
	29A	
	30A	
	31A	
PS2_LoadE	32A	913642
PS3_LoadE	1B	J6B
ABS_Bkup_E_S1	2B	
DC_Interlock_S2	3B	
ABS_Bkup_E_S2	4B	
Ctrl_Interlock_S3	5B	
	6B	
	7B	
Ctrl_Interlock_S4	8B	
Ctrl_Interlock_S5	9B	
ABS_Bkup_E_S3	10B	
Ctrl_Oper_Ind_S5	11B	
	12B	
DC_Interlock_S3	13B	
TX_SW_Interlock	14B	
	15B	
DC_Disable_S1	16B	
DC_Disable_S2	17B	
	18B	
	19B	
	20B	
DC_Disable_S3	21B	
DC_Disable_S4	22B	
DS_Switch_Pos_S1	23B	
DS_Switch_Pos_S2	24B	
US_Switch_Pos_S1	25B	
US_Switch_Pos_S2	26B	
US_SW_Interlock	27B	
PS1_LoadE	28B	
	29B	
	30B	
Slot ID #2	31B	
	32B	913642
	1C	J6C
ABS_Bkup_E_S4	2C	
	3C	
Disable_Bkup_Ctrl	4C	
	5C	
	6C	
	7C	
	8C	
	9C	
	10C	
	11C	
	12C	
	13C	
	14C	
	15C	
	16C	
	17C	
	18C	
	19C	
	20C	
	21C	
	22C	
	23C	
	24C	
	25C	
SCADA_S+	26C	
	27C	
SCADA_S-	28C	
DC_Interlock_S1	29C	
DC_Interlock_S5	30C	
Ctrl_Interlock_S1	31C	
Ctrl_Interlock_S2	32C	913642

J7A — 10 MHz Reference F7

Ext_Ref_I/P	1A	
	2A	
	3A	
	4A	
	5A	
	6A	
	7A	
	8A	
	9A	
System_+12Vdc	10A	
Slot ID 111	11A	
	12A	
System_-12Vdc	13A	
	14A	
SCADA_S-	15A	
	16A	
	1B	J7B
	2B	
	3B	
	4B	
	5B	
	6B	
	7B	
	8B	
	9B	
	10B	
System_+12Vdc	11B	
	12B	
	13B	
	14B	
	15B	
SCADA_S+	16B	
	1C	J7C
	2C	
10MHz_Ref_O/P_1	3C	
	4C	
10MHz_Ref_O/P_2	5C	
	6C	
10MHz_Ref_O/P_3	7C	
	8C	
10MHz_Ref_O/P_4	9C	
	10C	
	11C	
	12C	
	13C	
	14C	
	15C	
	16C	

Ext_Ref_I/P — J9 BNC

10MHz_Ref_O/P_1 — J10 BNC

10MHz_Ref_O/P_2 — J11 BNC

10MHz_Ref_O/P_3 — J12 BNC

10MHz_Ref_O/P_4 — J13 BNC

J8A — LCD Board F8

LCD_RS_S1	1A	
LCD_RW_S1	2A	
LCD_E_S1	3A	
LCD_RS_S2	4A	
LCD_RW_S2	5A	
LCD_E_S2	6A	
LCD_RS_S3	7A	
LCD_RW_S3	8A	
LCD_E_S3	9A	
System_+12Vdc	10A	
	11A	
	12A	
	13A	
	14A	
	15A	
	16A	
	17A	
	18A	
	19A	
	20A	
	21A	
	22A	
	23A	
	24A	
	25A	
	26A	
	27A	
	28A	
	29A	
	30A	
	31A	
	32A	913642
LCD_Data_0	1B	J8B
LCD_Data_1	2B	
LCD_Data_2	3B	
LCD_Data_3	4B	
LCD_Data_4	5B	
LCD_Data_5	6B	
LCD_Data_6	7B	
LCD_Data_7	8B	
LCD_Buffer_E	9B	
	10B	
	11B	
LCD_Flt_LED_S1	12B	
LCD_Flt_LED_S2	13B	
LCD_Flt_LED_S3	14B	
LCD_Flt_LED_S4	15B	
LCD_Flt_LED_S5	16B	
	17B	
	18B	
	19B	
	20B	
	21B	
	22B	
	23B	
	24B	
	25B	
	26B	
	27B	
	28B	
	29B	
	30B	
	31B	
	32B	913642
LCD_Ctrl_Select_1	1C	J8C
LCD_Ctrl_Select_2	2C	
LCD_Ctrl_Select_3	3C	
LCD_Ctrl_Select_4	4C	
LCD_Ctrl_Select_5	5C	
LCD_RS_S4	6C	
LCD_RW_S4	7C	
LCD_E_S4	8C	
LCD_RS_S5	9C	
LCD_RW_S5	10C	
LCD_E_S5	11C	
LCD_Switch_5	12C	
LCD_Switch_4	13C	
LCD_Switch_3	14C	
LCD_Switch_2	15C	
LCD_Switch_1	16C	
	17C	
	18C	
	19C	
	20C	
	21C	
	22C	
	23C	
SCADA_S+	24C	
SCADA_S-	25C	
	26C	
Enet_TX+	27C	
Enet_TX-	28C	
	29C	
Enet_RX+	30C	
Enet_RX-	31C	
	32C	913642

J14-1 — Control Backplane to Bandpass Filter Backplane

BPF_Interlock_S1	1A	J14-1
BPF_Rly_Main_S1	2A	J14-2
BPF_Rly_Pos_S1	3A	J14-3
BPF_Rly_ABS_S1	4A	J14-4
BPF_MAC_S1	5A	J14-5
	6A	J14-6
BPF_Interlock_S2	7A	J14-7
BPF_Rly_Main_S2	8A	J14-8
BPF_Rly_Pos_S2	9A	J14-9
BPF_Rly_ABS_S2	10A	J14-10
BPF_MAC_S2	11A	J14-11
	12A	J14-12
BPF_Interlock_S3	13A	J14-13
BPF_Rly_Main_S3	14A	J14-14
BPF_Rly_Pos_S3	15A	J14-15
BPF_Rly_ABS_S3	16A	J14-16
BPF_MAC_S3	17A	J14-17
	18A	J14-18
BPF_Interlock_S4	19A	J14-19
BPF_Rly_Main_S4	20A	J14-20
BPF_Rly_Pos_S4	21A	J14-21
BPF_Rly_ABS_S4	22A	J14-22
BPF_MAC_S4	23A	J14-23
	24A	J14-24
TX_SW_Interlock	25A	J14-25
DS_Switch_Pos_S1	26A	J14-26
DS_Switch_Pos_S2	27A	J14-27
Ctrl_Oper_Ind_S5	28A	J14-28
TX_SW_MAC	29A	J14-29
System_PS_Stat_1	30A	J14-30
System_PS_Stat_2	31A	J14-31
PS1_LoadE	32A	J14-32
PS2_LoadE	1B	J14-33
PS3_LoadE	2B	J14-34

J15 — 95123-2881 Ethernet Input

Enet_TX+	1	
Enet_TX-	2	
Enet_RX+	3	
	4	
	5	
Enet_RX-	6	
	7	
	8	
GND	9	
GND	10	

J16-1 — Control Backplane to Power Amp / P.S. Backplane

PA_Interlock_S1	1A	J16-1
PA_PS_Good_S1	2A	J16-2
PA_PS_Enable_S1	3A	J16-3
PA_Oper_Rqst_S1	4A	J16-4
PA_Output_Stat_S1	5A	J16-5
PA_Temp_Stat_S1	6A	J16-6
	7A	J16-7
PA_Interlock_S2	8A	J16-8
PA_PS_Good_S2	9A	J16-9
PA_PS_Enable_S2	10A	J16-10
PA_Oper_Rqst_S2	11A	J16-11
PA_Output_Stat_S2	12A	J16-12
PA_Temp_Stat_S2	13A	J16-13
	14A	J16-14
PA_Interlock_S3	15A	J16-15
PA_PS_Good_S3	16A	J16-16
PA_PS_Enable_S3	17A	J16-17
PA_Oper_Rqst_S3	18A	J16-18
PA_Output_Stat_S3	19A	J16-19
PA_Temp_Stat_S3	20A	J16-20
	21A	J16-21
PA_Interlock_S4	22A	J16-22
PA_PS_Good_S4	23A	J16-23
PA_PS_Enable_S4	24A	J16-24
PA_Oper_Rqst_S4	25A	J16-25
PA_Output_Stat_S4	26A	J16-26
PA_Temp_Stat_S4	27A	J16-27
	28A	J16-28
PA_Interlock_S5	29A	J16-29
PA_PS_Good_S5	30A	J16-30
PA_PS_Enable_S5	31A	J16-31
PA_Oper_Rqst_S5	32A	J16-32
PA_Output_Stat_S5	1B	J16-33
PA_Temp_Stat_S5	2B	J16-34
	3B	J16-35
PA_Frw_Pwr_S1	4B	J16-36
PA_Rfl_Pwr_S1	5B	J16-37
PA_BiasVdc_S1	6B	J16-38
PA_Frw_Pwr_S2	7B	J16-39
PA_Rfl_Pwr_S2	8B	J16-40
PA_BiasVdc_S2	9B	J16-41
PA_Frw_Pwr_S3	10B	J16-42
PA_Rfl_Pwr_S3	11B	J16-43
PA_BiasVdc_S3	12B	J16-44
PA_Frw_Pwr_S4	13B	J16-45
PA_Rfl_Pwr_S4	14B	J16-46
PA_BiasVdc_S4	15B	J16-47
PA_Frw_Pwr_S5	16B	J16-48
PA_Rfl_Pwr_S5	17B	J16-49
PA_BiasVdc_S5	18B	J16-50

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J22-1 — Control Backplane to Signal Processing Backplane

UC_Interlock_S1	1	J22-1
UC_ALC_S1	2	J22-2
UC_Mute_Cmd_S1	3	J22-3
UC_Mute_Ind_S1	4	J22-4
UC_Input_Flt_S1	5	J22-5
UC_Ref_Flt_S1	6	J22-6
UC_PLL_Flt_S1	7	J22-7
UC_Interlock_S2	8	J22-8
UC_ALC_S2	9	J22-9
UC_Mute_Cmd_S2	10	J22-10
UC_Mute_Ind_S2	11	J22-11
UC_Input_Flt_S2	12	J22-12
UC_Ref_Flt_S2	13	J22-13
UC_PLL_Flt_S2	14	J22-14
UC_Interlock_S3	15	J22-15
UC_ALC_S3	16	J22-16
UC_Mute_Cmd_S3	17	J22-17
UC_Mute_Ind_S3	18	J22-18
UC_Input_Flt_S3	19	J22-19
UC_Ref_Flt_S3	20	J22-20
UC_PLL_Flt_S3	21	J22-21
UC_Interlock_S4	22	J22-22
UC_ALC_S4	23	J22-23
UC_Mute_Cmd_S4	24	J22-24
UC_Mute_Ind_S4	25	J22-25
UC_Input_Flt_S4	26	J22-26
UC_Ref_Flt_S4	27	J22-27
UC_PLL_Flt_S4	28	J22-28
UC_Interlock_S5	29	J22-29
UC_ALC_S5	30	J22-30
UC_Mute_Cmd_S5	31	J22-31
UC_Mute_Ind_S5	32	J22-32
UC_Input_Flt_S5	33	J22-33
UC_Ref_Flt_S5	34	J22-34
UC_PLL_Flt_S5	35	J22-35
LNA_Interlock_S1	36	J22-36
LNA_Interlock_S2	37	J22-37
LNA_Interlock_S3	38	J22-38
LNA_Interlock_S4	39	J22-39
DC_Interlock_S1	40	J22-40
DC_Disable_S1	41	J22-41
DC_Interlock_S2	42	J22-42
DC_Disable_S2	43	J22-43
DC_Interlock_S3	44	J22-44
DC_Disable_S3	45	J22-45
DC_Interlock_S4	46	J22-46
DC_Disable_S4	47	J22-47
DC_Interlock_S5	48	J22-48
DC_Disable_S5	49	J22-49
	50	J22-50
DS_SW_Interlock	51	J22-51
DS_Switch_Pos_S1	52	J22-52
DS_Switch_Pos_S2	53	J22-53
Ctrl_Oper_Ind_S5	54	J22-54
	55	J22-55
US_SW_Interlock	56	J22-56
US_Switch_Pos_S1	57	J22-57
US_Switch_Pos_S2	58	J22-58
DC_Disable_S5	59	J22-59
Set US-DS_Dev Type	60	J22-60

J17 SCADA — 95123-2881

SCADA_S+	4
SCADA_S-	5
GND	9
GND	10

J18 SCADA — 95123-2881

SCADA_S+	4
SCADA_S-	5
GND	9
GND	10

J19 — 55556-4

System_+12Vdc	1

J20 — 55556-4

J21 — 55556-4

System_-12Vdc	1

APV	ADC Telecommunications	REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION	TITLE	SCH., BWA 2000, CNTRL MOD. BACKPLANE, PHASE 1 (1119948)		
ECO	MATERIAL -----	DWN	JKF	7/11/00	DWG. NO. 1119953 REV A0
REV	FINISH -----	CHK	REH	9/5/00	
		REL	REH	9/5/00	D SCALE --- SHEET 1 OF 1