EXHIBIT I

FCC TYPE ACCEPTANCE REPORT

ADC TELECOMMUNICATIONS

MODEL 5721

FCC ID-CJJ79XITS-7039

ITFS/MDS/MMDS TRANSMITTER

Date Filed _____

This application is filed in compliance with
Part 2, Part 21 and Part 74
of the FCC Rules and Regulations.

ADC Telecommunications
102 Rahway Road
McMurray, PA 15317

Rev. 1.0

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1.0 IDENTIFICATION OF APPLICANT AND EQUIPMENT

1.1 Applicant:

ADC Telecommunications
102 Rahway Road
McMurray, PA 15317-3345

The above name and address is printed on a label attached to the rear panel of the equipment.

1.2 Equipment and Model Number: 5721

This information is provided on the front panel of the equipment.

1.3 ADC Telecommunications shall manufacture this product in quantities necessary to satisfy market demand.

2.0 TECHNICAL DESCRIPTION - MODEL 5721

2.1 Introduction

The 5721 is a complete MDS/MMDS/ITFS transmitter capable of operating as television transmitter at a nominal power of 10 Watts peak sync and 316 mW average aural. The baseband video and audio signals are fed to the modulator which modulates the signals onto their respective carriers (45.75 MHz visual, 41.25 MHz aural). The visual and aural signals are internally diplexed and the combined IF output is routed to the upconverter module for IF signal processing and upconversion to the MDS/MMDS/ITFS frequency. The RF signal is then fed to an amplifier module for final amplification. The 5721 utilizes ALC circuitry for automatic level control of the output signal to maintain a constant power level. The 5721 transmitter is a 19-inch rack mount assembly and can be supplied with or without a cabinet. The unit is supplied complete with cables and cabinet slides.

Parameters and specifications for operation of this unit as an NTSC transmitter are provided on the following pages, and a complete circuit description and alignment procedure are also included in this report. Refer to the overall system block diagram and the particular referenced schematics in the attached circuit description section of this report.

2.0 TECHNICAL DESCRIPTION

2.2 Technical Specifications

Type of Emissions:
- Visual 5M75C3F
- Aural 250KF3E

Frequency Range ..... 2150 to 2162 and 2500 to 2686 MHz (any 6 MHz channel)
Output Power Rating: ..... 20 watts peak envelope
- Visual ..... 10 watts peak-of-sync
- Aural ..... -15 dB (relative to peak-of-sync)

DC voltage and total current of final amplifier stage ..... 10 volts DC at 6.86 amps
(Class A - Not RF power dependent)

2.3 Performance Specifications

Visual Performance

Operating Frequency Range ..... 2150 to 2162 and 2500 to 2686 MHz
RF output - Nominal:
- Power ..... 10 watts peak-of sync
- Impedance ..... 50 ohms
- Connector ..... Type N

Combined Input::
- Level ..... 0 dBm
- Impedance ..... 75/50 Ω

Visual Sideband Response:
(Referenced to 200 KHz)
- From -0.75 to 3.58 MHz ..... ±1 dB
- Below -1.25 MHz ..... -20 dB
- Above +4.75 MHz ..... -30 dB
- From 3.58 to 4.18 MHz ..... +0. -2 dB

Differential Phase ..... ±3°
Incidental Phase Modulation ..... ±3°
Differential Gain 0.5%
Low Frequency Linearity ..... 0.5 dB
Amplitude Variation Over One Field 2%
Regulation Of Output 4%
Envelope Delay vs. Frequency ..... Per FCC
2T Pulse 2%
12.5T pulse 4%
AM Noise ..... -55 dB
Harmonic and Spurious Emission ..... -60 dB
Carrier Frequency Stability ..... ±1000 Hz

Note: Visual sideband Response is Reversed for the MDS service

2.0 TECHNICAL DESCRIPTION

2.3 Performance Specifications

Aural Performance

Output Power	(relative to visual power) -15 dB (adjustable in the Modulator)
Amplitude vs. Frequency Response	±0.5 dB
Audio Harmonic Distortion	0.5%
FM Noise	-55 dB
Aural to Visual Carrier Separation	4.5 MHz ±100 Hz
Modulation capability	±75 KHz

Electrical Requirements

Power Line Voltage:	117 VAC ±10%, 60 Hz or 220 VAC ±10%, 50 Hz
Power Consumption:	250 watts

Environmental

Maximum Altitude:	12,000 feet (3,660m)
Ambient Temperature	0° to 50°C

Mechanical

Dimensions: (WxDxH):	19" x 21" x 8.75" (48.3cm x 53.3cm x 22.24cm)

Weight: 45 lbs. (22.0 kgs)

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description

The 5721 ITFS/MDS/MMDS Transmitter can be subdivided further as follows:

- Modulator Module
- IF Processing Module
- Power Amplifier Module
- Power Supply Module
- Control Monitoring Module
- L.O./Upconverter Module
- Backplane Board
- Front Panel LCD Display/Keypad Entry

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description

Analog Modulator Module

The visual and aural input signals to the 5721 transmitter are fed to the Analog Modulator Board (1585-3305). The Analog Modulator Board has separate video and audio input connectors and a combined IF output connector. The baseband video signal enters at J1 and is applied to a diode surge protection circuit then buffered to several sections of group delay circuitry which compensates for any signal delay that may occur during chanel combining. Video gain adjustment is provided by potentiometer R61. The video signal is then fed to a balanced modulator where it is modulated onto a 45.75 MHz oven controled VCXO carrier. The output of the modulator is double sideband AM. An LCR network around the modulator provides a degree of incidental phase correction. The double-sideband AM signal is buffered and sent to a loop through at J17 and J14, for IF encoding, then transformer coupled to a SAW filter. In the SAW filter path LRC (R216, R161, L15, C81 and R217, R162, L16, C82) networks are provided for frequency response adjustments. The output of the SAW Filter is amplified (U17) to copensate for any loss in the filter and combined with the aural signal using a lumped element Wilkinson combiner.

The modulator module accepts both balanced and composite audio signals. Provisions have also been made to allow 4.5 MHz IF input signals through the composite audio input line by moving on board jumpers (W1, W2, and W4). The balanced and composite audio signals are applied to diode surge protecters then buffered and applied to a common junction point before before being applied to an audio gain amplifier. The gain of the amplifier is set by adjusting R13. The signal is then modulated onto a 4.5 MHz VCO generated carrier utilizing a varactor diode controlled tank circuit. The signal is then fed to a balanced modulator where it is frequency modulated to an IF feequency of 41.25 MHz. The IF signal is then sent to a loop through at J21, for IF encoding , then applied to the Wilkinson combiner where it is combined with the visual signal. Visual and aural level adjustments are provided by R147 and R167 respectfully. These adjustments set the Visual/Aural carrier ratio (typically 10 to 15 dB). The combined IF from the Wilkinson combiner is applied to an LCR frequency response correction circuit then amplified before being fed to the combined output of the module (J1C-31) An IF O/P sample (J10) is provided by a transformer coupler.

The visual IF carrier is produced by a phase locked loop controlled VCXO with an output frequency of 45.75 MHz (NTSC). The PLL circuit takes a sample of the IF output frequency and using a dual modulas prescaler and a PLL IC (U15), compares it to a reference frequency generated from an external precise 10 MHz reference input. The difference between the phase of the reference frequency and the divided down oscillator output, causes the PLL IC to create an error voltage output (AFC), which is used to bias a voltage controlled variable capacitor in the VCXO. By continuously correcting the output frequency of the VCXO with this error voltage, the frequency stability of the VCXO can be increased to that of a precise reference frequency source.

The Modulator Module also provides for locking the frequency separation between the visual and aural IF carriers to a precise 5 5/9 KHz reference signal which is generated from the 10 MHz reference input. A sample of the 4.5 MHz frequency generated by the aural VCO, also known as the intercarrier is applied to a PLL IC (U14), which is programmed using DIP switches S3, S4, and S5 and S11. The PLL IC divides the reference and intercarrier signals to a common frequency and compares each signal to produce an error signal which in turn is applied to an active filter circuit. The active filter produces an AFC voltage which is directed to the aural VCO, establishing a PLL circuit. Any subsequent change in the visual to aural separation frequency will be corrected by the AFC.

2.4 Circuit Description - continued

Analog Modulator Module - continued

Because the PLL circuits require a reference signal for correct operation, a reference detector circuit is provided to sense the presense of the external 10 MHz source. If a reference is present, an automatic latching relay provides the reference signal to the reference divider IC (U10). If the detector circuit does not sense the presence of the external reference, the circuit automatically switches to an internal 10.00MHz crystal (U11).

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

IF Processing Module

The combined IF output signal from the modulator module is applied to the IF input jack (J14) on the rear of the tray. This IF input signal is then fed to the IF Processing Card (1585-3108).

The IF signal enters the card at J1 and is transformer coupled for impeadance matching of the IF signal (75Ω to 50Ω). The signal is then applied to an adjustable resistor pad network which allows for three IF input level ranges of 10 dB each. The signal is amplified and applied to a 6 dB transformer directional coupler which provides a sample to a peak detector in the ALC portion of the circuit. The main output of the coupler is fed to frequency response correction circuitry which consist of four adjustable notch filters. The frequency response correction circuit may be removed using on board jumpers. The output of the frequency response corrector is amplified and applied to a PIN diode attenuator. The ALC circuitry takes a peak detected sample of the IF signal and generates an ALC voltage which biases the PIN diode attenuator. The ALC circuit senses any change in the IF level and automatically adjust the loss through the PIN attenuator to compensate, thereby maintaining a constant IF output regardless of minor changes in the input signal. The ALC circuit uses a DC level generated externally to control the output power level. There are two possible bias voltage inputs. The first, Inner Loop, is generated form a peak detected sample of the output amplifier. The second, Outer Loop, is used only if an external final amplifier tray is connected to the system. If both Inner Loop and Outer Loop inputs are used, the signal that is the largest in level controls the ALC circuit.

The ALC circuit may be bypassed by placing switch SW2 in the manual position. When the ALC circuit is disabled, the loss through the PIN attenuator is adjusted by a manual gain potentiometer which then directly controls the output in a manual fashion.

The ALC circuit also contains a average detector which detects the average level of the IF signal. This average level is compared to the output of the peak detector and if the average level approaches the peak level, indicating a loss of modulation on the IF signal, a mute signal will be generated muting the IF. This prevents against overpower conditions in situations where the modulating signal is interrupted. The ALC circuit provides several front panel LED indicators including: Peak Vs. Average Fault, I/P Fault, Mute, and ALC Fault.

The output of the PIN diode attenuator is amplified an applied to three sections of group delay equalization which compensate for group delay created by external filters. Each section of group delay may be removed from the circuit using on board jumpers. For non-adjacent analog applications, Delay Equalizer 1 is removed from the circuit. For adjacent analog applications, all three sections are used. For adjacent and non-adjacent digital applications, Delay Equalizer 3 is removed from the circuit. The output of the delay equalizer circuit is fed to a 6 MHz lumped element bandpass filter. The bandpass filter may be removed from the circuit using on board jumpers. The bandpass filter may also be bypassed through a SAW filter when tight filtering of the IF is required.

The output of the bandpass filter is applied to a linearity correction circuit which compensates for compression in later stages of the system. The output of the linearity correction circuit is fed to a 6 dB transformer directional coupler which provides a front panel sample of the IF signal. The main output of the coupler is connected to the output of the IF Processing Card (J1B).

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Frequency Generator/Upconversion/PLL Module

The Frequency Generator/Upconversion/PLL Module consist of a L.O./Upconverter Board (1585-3117), Interdigital Filter (2140-1006), and a Single stage Amplifier Board (1585-3101).

The L.O./Upconverter Board generates a UHF L.O. frequency using a voltage controlled oscillator (VCO) IC (V804ME01). The VCO is locked to an external precise 10 MHz reference using a frequency synthesizer PLL IC (LMX2325TM) in a phase lock loop configuration. The LMX2325TM is a high performance frequency synthesizer with integrated prescalers and uses a proprietary digital phase lock loop technique to produce a very stable low noise signal that is used to control the VCO frequency. The desired L.O. frequency is selected using the front panel LCD display/keypad. The Control Monitoring Assembly detects the keyboard input and routs the serial data to the serrial data input of the PLL IC.

Under normal operating conditions, the external 10 MHz precise reference input will be routed to the oscillator input of the PLL IC through a magnetic latching relay (K1). IF the external precise reference is removed the relay will open and an internal 10 MHz reference oscillator IC will be routed to the oscillator input of the PLL IC.

The L.O. signal from the VCO is buffered to an internal microstrip coupler which provides an L.O. sample that is routed to a rear panel jack. The L.O. signal is then amplified by an IC amplifier (U8) to a sufficient level to drive the L.O. input of an IC mixer(U10). An IF input to the mixer is provided via the IF Processing Assembly. The output of the mixer is amplified by an IC amplifier (U12) and fed to the RF output jack of the board (J8).

The RF signal is then fed to a 6 MHz bandpass interdigital filter (2140-1006) which selects the desired conversion frequency (L.O. - IF) and attenuates any undesired signals generated during the mixing process.

The RF output of the filter is then fed to the Single Stage Amplifier Board (1585-3101) which consist of a single IC amplifier (VNA-25) with a gain of 14 dB. An RF sample is obtained using a microstrip coupler (J2). The main RF output is connected to the output jack of the module (J8).

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Power Amplifier Module

The Power Amplifier Module consist of an 40W PEP Amplifier Module (1585-3196), 5 Section Bias Board (1585-3109), and Dual Power Detector Board (1585-3125).

The 80W pep Amplifier provides both amplification and Feed Forward distortion cancellation. This module is subdivided into 5 functional sections: preamplifier section, power amplifier section, feed forward cancellation section, correction signal amplifier section, and RF output section.

The RF input signal from the Frequency Generator/Upconversion/PLL Module enters the module at J1 and is fed to the preamplifier section. The preamplifier consist of three cascaded GaAs FET amplifiers (FLL 101ME driving a FLL 351ME driving a FLL 200IB-3) with an overall gain of approximately 24 dB. The output of the final FET is applied to a 3.0 dB microstrip hybrid coupler which splits the signal providing an output sample at J2. This sample is used in the feed forward distortion cancellation section of the module which the correction signal that will be amplified and coupled with the RF output signal to cancel the distortion created in the power amplifier. The main output of the coupler is fed to the power amplifier section of the module.

The power amplifier consist of three GaAS FET amplifiers (FLL 200IB-3 driving two parallel S45V2527-51's) with an overall gain of approximately 21 dB. A 20 dB microstrip coupler provides an uncorrected (distorted) sample of the RF signal at J4. This uncorrected sample is fed to the correction signal input (J10) of the feed forward distortion cancellation section of the module.

The preamplifier (undistorted) sample is phase shifted 180° through a delay line and fed to the feed forward distortion cancellation section where it is coupled with the uncorrected signal from the output amplifier. Combining these two signals(the phase shifted (180°) input signal, and the distorted RF output signal) cancels the information carrying component of the signal, leaving only the distortion of the output amplifier.

This correction signal is fed to the correction signal amplifier section of the module where it is amplified to a sufficient level to cancel the distortion created by the output amplifier. The correction signal amplifier consist of three cascaded GaAs FET amplifiers (FLL101ME driving a FLL351ME driving a S45V2527-51) with an overall gain of approximately 36 dB.

The amplified correction signal and the phase shifted (180°) output of the power amplifier are applied to a hybrid microstrip coupler in the RF output section of the module where the signals are coupled together, effectively canceling the distortion in the output signal. The main output of the module (J8) is connected to the RF output jack (J8) on the rear of the tray. A 20 dB forward power sample is obtained using an internal microstrip coupler. A reflected power sample is provided by a circulator.

The DC biasing of the FET amplifiers in each section of the module is controlled and filtered by corresponding daughter boards (daughter boards D6 and D7 for the preamplifier, daughter boards D1, D2, and D3 for the power amplifier, and daughter boards D4 and D5 for the correction signal amplifier). which are soldered directly to the main board. The DC bias drain to source currents are set by adjusting the negative gate to source voltages which are adjusted by potentiometers on the daughter boards.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

The 5 Section Bias Protection Board distributes the -5V bias voltages and +10V drain voltages to the Amplifier Module as well as providing protection from an over current condition with board mounted fuses.

The -5V bias voltage is generated on board using a voltage regulator (LM377T). This bias voltage is also used as an interlock which is fed to the Transmitter Control and Monitoring Module. IF the bias voltage is lost, the control circuitry will immediately shut down the switching supply, thereby removing the drain voltages from the amplifier modules and protecting the GaAS FET devices.

Differential amplifier OP Amp circuits are used to monitor the drain currents of the FET devices. The OP Amp outputs drive LED indicators as well as an opto-isolated O/P amplifier status line.

The Dual Power Detector Board inputs forward and reflective power signals from the Amplifier Module and detects the levels using peak detector circuits. These circuits provide voltage levels proportional to the power level of the sampled signal which are used for metering and ALC purposes. Metering adjustment is provided with on board potentiometers.

The Dual Power Detector Board also contains a gating pulse timing circuit that serves to maintain the proper power level when sync suppression scrambling systems are used.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Transmitter Control Monitoring and Module

The Transmitter Control and Monitoring Module (1585-1129) consist of an 8-bit microcontroller (MC68HC705B`6) and associated control circuitry and provides the capability to control and monitor the operating status o the transmitter. The interconnection between the Transmitter Control and Monitoring Module, IF Processing Module, and Local Oscillator/Upconverter Module is accomplished through the Backplane Board. The interconnection between the Transmitter Control and Monitoring Module, Power Supply Module, and Power Amplifier Module is accomplished through interconnect cables. A detailed listing of all the interfaces between the Transmitter Control and Monitoring Module and the various modules which make up the ITS-5724 transmitter is given below.

Power Amplifier Module

Signal Name	Signal Type/Description
Amplifier Interlock	Discrete contact closure input - indicates Power Amplifier Module is installed.
Reflective Pwr Metering	Analog input (0 - 1.25V) - indicates reflective power from Power Amplifier Module.
Overtemp Fault	Discrete contact closure input - indicates overtemp condition exist in Power Amplifier Module.
O/P Amplifier Status	Discrete open collector input - indicates operating status of output amplifier.
-5V Bias Sense	Analog input (0 - 6V) - indicates the voltage level of the - 5V bias supply.

Local Oscillator/Upconverter Module

Signal Name	Signal Type/Description
External Reference Indicator	Discrete open collector input - indicates the presence of external 10 MHz reference.
Logic Enable	Discrete CMOS output - provides a load enable signal the the frequency synthesizer chip.
Data	Discrete CMOS output - provides serial data to the frequency synthesizer chip.
Clock	Discrete CMOS output - provides the serial clock the frequency synthesizer chip.
AFC	Analog input (1 - 10V) - indicates the level of the AFC voltage.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Transmitter Control Monitoring and Module - continued

Signal Name	Signal Type/Description
L.O./Upconverter Interlock	Discrete contact closure input - indicates L.O./Upconverter Module is installed.
Unlock Indicator	Discrete open collector input - indicates the L.O./Upconverter Module is locked to the external or internal 10 MHz reference.

IF Processing Module

Signal Name	Signal Type/Description
Open Loop Monitor	Analog input (1 - 1.25V) - indicates output power of an external amplifier.
Forward Power Metering	Analog input (0 - 1.25 V) - indicates output power tray's power amplifier.
IF Processor Interlock	Discrete Contact Closure Input - indicates that IF Processing module is installed.
ALC Voltage	Analog input (0 - 10V) - indicates voltage applied to pin attenuator in ALC circuit.
Mute to IF Processor	Discrete open collector output - controls mute feature in the IF processor.
Mute from IF Processor	Discrete open collector input - indicates IF processor is in mute.
Input Fault	Discrete open collector input - indicates that IF is not present.
ALC Conditioning	Analog Input (-1 - +1V) - Provides adjustment voltage to the ALC circuitry to correct for frequency dependence of peak detector.

Power Supply Module

Signal Name	Signal Type/Description
P.S Good	Discrete open collector input - indicates switching power supply is operating properly.
P.S Enable	Discrete open collector output - enable signal to switching power supply.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Transmitter Control and Monitoring Module - continued

Front Panel Assembly

Signal Name	Signal Type/Description
Fault Anode	Fault LED drive voltage (+5V) - supply to anode of Fault LED.
Fault Cathode	Discrete open collector output - provides pull down to turn on Fault LED.
Operate Anode	Fault LED drive voltage (+5V) - supply to anode of Operate LED.
Operate Cathode	Discrete open collector output - provides pull down to turn on Operate LED.
S1-S5	Discrete contact closure inputs - input lines from front panel keyboard switches.
VSS (GND)	Ground - Provides return to front panel board.
VCC	+5VDC - provides +5V to front panel display logic.
VEE	Control voltage output (0 - 5V) - controls contrast of LCD display.
RS	Discrete TTL/HCMOS output - indicates to display whether instruction or data command is being sent.
E	Discrete TTL/HCMOS output - initiates the transfer of data to the display.
DB0-DB7	Discrete TTL/HCMOS bidirectional data lines - data lines which pass data between the display and transmitter control and monitoring module.
Anode Backlight	Control voltage output (3.8 - 4.6 V) - provides drive voltage to LCD backlight of display.
Cathode Backlight	Control voltage return - return for control voltage of LCD display.

SCADA Communications Interface

Signal Name	Signal Type/Description
+ Serial Line	+RS-485 communications line - provides the +differential line for the +bidirectional line of the bidirectional RS-485 communications..
- Serial Line	-RS-485 communications line - provides the -differential line for the +bidirectional line of the bidirectional RS-485 communications..

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Transmitter Control and Monitoring Module - continued

Control and Remote Interface

Signal Name	Signal Type/Description
Standby Command (FA)	Discrete open collector input - indicates frequency agile is requesting transmitter be placed into standby mode.
Operate Command (FA)	Discrete open collector input - indicates frequency agile is requesting transmitter be placed into operate mode.
Aural/Visual Mute (FA)	discrete open collector input - indicates that frequency agile is presently in aural/visual mute.
ABS Standby CMD	Discrete open collector input - indicates that Automatic Back-up System is requesting transmitter be placed into standby.
EXT Operate CMD	Discrete open collector output - enables external amplifier when transmitter enters operate mode.
XMTR Interlock Iso Return	Ground - configurable ground return which can be either jumpered directly to ground or be the “source” pin of an FET so that transmitter interlock can be daisy chained with other transmitters.
XMTR Interlock	Discrete open collector output - enables transmitter interlock or complete interlock daisy chain.
EXT O/P Amp Mod Status	Discrete open collector input - indicates external amplifier has a fault.
EXT P.S. Status (amp)	Discrete open collector input - indicates power supply in external amplifier is functional.
Operate Indication	Discrete open collector output - indicates transmitter is in operate mode.
EXT Overtemp (amp)	Discrete open collector input - indicates external amplifier has overtemp condition.
EXT Refl Pwr (amp)	Analog input (0 - 1.25V) - indicates reflected power of external amplifier.
Standby CMD (RCVR)	Discrete open collector input - indicates external receiver is requesting transmitter be placed into standby.
Operate Commend	Discrete open collector input - indicates external receiver is requesting transmitter be placed into operate.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Transmitter Control and Monitoring Module - continued

Control and Remote Interface

Signal Name	Signal Type/Description
RMT Operate Indicator	Discrete open collector output - indicates transmitter is in operate mode.
O/P Amp Module Status	Discrete open collector output - indicates no faults present in amplifier modules of transmitter.
RMT FWD Power O/P	Analog output (0 - 1.25V) - power amplifier module forward power loop through.
RMT REFL Power	Analog output (0 - 1.25V) - power amplifier module reflective power loop through.
RMT XMTR Fault Ind	Discrete open collector output - indicates fault exist in transmitter.
IF Present Status O/P	Discrete open collector output - indicates IF is not present.
RMT PLL Locked Ind	Discrete open collector output - indicates frequency generator/upconverter is unlocked.
RMT XMTR Overtemp Ind	Discrete open collector output - indicates transmitter amplifier module is in overtemp.
P.S. Fault Ind	Discrete open collector output - indicates that power supply of transmitter has failed.
EXT PLL Ref Present	Discrete open collector output - indicates external 10 MHz reference is not present.
RMT XMTR Stby Command	Discrete open collector input - indicates remote interface is requesting transmitter be placed in standby.
RMT XMTR Oper Command	Discrete open collector input - indicates remote interface is requesting transmitter be placed in operate.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description - continued

Power Supply Module

The transmitter may be powered by either a 115 VAC/60 Hz or 230 VAC/50 Hz source. The AC source enters the tray at jack J1and passes through the Power Entry Module. The Power Entry Module contains a switch, for selecting 115V or 230 V input, a line filter and fuse protection. The output of the Power Entry Module is distributed to a terminal block (TB1). Varistors VR1, VR2, VR3 and VR4 provide transient and over voltage protection to the transmitter. The rear panel circuit breaker applies AC voltage to the input of the 530 W Switching Power Supply (MP6-2K-4ll-00-415-CE) located on the Power Supply Module.

The Switching Supply provides three outputs. The first output is a +11 VDC/31A line used to power the GaAs FET amplifiers with power The remaining outputs are +12 VDC lines used to supply the modules within the transmitter. The +12 VDC line is also used to power the 12 VDC cooling fan via the Backplane Board.

2.0 TECHNICAL DESCRIPTION

2.5 Alignment Procedure

In the following procedure, the complete transmitter is adjusted for optimum performance, beginning with the modulator, followed by the upconverter/amplifier, starting at the baseband input and adjusting each circuit for its specified performance while observing the appropriate output parameters of the board or subassembly being adjusted.

Because of the broadband nature of most of the amplifier stages, this is a straightforward procedure, easily accomplished if baseband, IF, and RF test equipment is available. In this procedure, the input signals are first connected and each circuit is adjusted in sequence by connecting the test equipment to the specified point.

Equipment Needed

Backplane Test Fixture	
Spectrum Analyzer	10 MHz Reference Generator
Oscilloscope	Video Signal Generator
RF Power Meter	Voltmeter
30 dB Directional Coupler	50Ω Load
10 dB Directional Coupler	

Modulator Assembly

Follow the steps below to align the Analog Modulator Module.

1. Connect test jumpers from Visual IF O/P to Visual IF I/P, and from Aural IF I/P to Aural IF O/P on the Backplane Test Fixture.

2. Preset the following jumpers on the modulator board:

J4 pins 2 and 3	J2 to In
J6 pins 2 and 3	J5 pins 1 and 2
J9 pins 2 and 3	J11 pins 1 and 2

3. Connect external 10MHz source to the 10MHz I/P of the Backplane Test Fixture.

4. Connect the +12V source to the power supply harness on the Backplane Test Fixture.

5. Measure voltage at test point 1 (TP1). Verify that voltage is between 3 and 6 volts.

6. Adjust L1 for 4 volts at TP1.

2.0 TECHNICAL DESCRIPTION

2.5 Alignment Procedure - continued

7. Record voltage level at TP2.
8. Connect the video source to the Video I/P on the Backplane Test Fixture.
9. Connect the VM700 to the Visual O/P of the Backplane Test Fixture.
10. Set the video generator for a 5 step NTSC video signal.
11. Set the front panel Clamp switch to “on”, and set the proper depth of modulation using R61..
12. Set the front panel Clamp switch to “off”, and adjust Manual Bias potentiometer R83 for proper depth of modulation.
13. With a spectrum analyzer connected to the Visual O/P of the Backplane Test Fixture, adjust front panel Visual Level potentiometer (R14) for an output of –8 dBm.
14. Adjust L17, L18 and L19 for maximum aural peak.
15. Adjust R167 to verify that a 15Db A/V ratio can be obtained.
16. Connect the VM700 to the Combined O/P of rthe Backplane test Fixture.
17. Using C107 and R197 adjust for best ICPM. Verify ICPM is within specifications.
18. Readjust Video Gain for proper depth of modulation.
19. Set the video signal to Multiburst and verify that the Out of Band products are within specifications.
20. Reconnect the Combined O/P to the spectrum analyzer and sert video signal to Cable Sweep.
21. If necessary, adjust R161, R162, C81, and C82 to meet frequency response specifications.
22. Reconnect the VM700 to the Combined O/P of the Backplane Test Fixture and set the video input signal to SinX/X.
23. Adjust R69, R80, R79, R74, L2, L5, L4 and L3 for optimum Group Delay response.
24. Set the video source to FCC Composite, and measure the Differential Gain and Differential Phase. Verify measurements are within specs.
25. Measure Video Signal to Noise Ratio and verify measurement is within specs.
26. Adjust R98 Visual Overmodulation potentiometer just until DS7 LED illuminates, and verify no change in response.
27. Turn Visual Overmodulation potentiometer CCW just until DS7 LED extinguishes.
28. Verify that the external 10MHz LED lights with external 10MHz source connected to the board.

2.0 TECHNICAL DESCRIPTION

2.5 Alignment Procedure - continued

29. Disconnect the external 10MHz source, and verify that the external 10MHz LED extinguishes.

30. Connect an IF CW source (0dBm) to the IF CW jack of the Basckplane Test Fixture and verify that the CW LED lights.

31. Disconnect the video source from the bacdkplane and verify that the Video Loss LED lights.

32. Connect an external 4.5 MHz source from a signal generator at –10 dBm to the Composite Audio I/P. Reconnect the spectrum analyzer to the Combined IF O/P.

33. Set J4, J5 and J6 jumpers to pins 2 and 3.

34. Verify that a 15 dB A/V ratio can be set.

35. Return the J4, J5 and J6 jumpers to pins 1 and 2.

Control Monitoring Module (A4) 1585-1129

Set front panel configuration DIP switches as follows:

SW1	Open (no external amplifier)	SW5	Open (not used)
SW1	Open (external ITS-5010 modulator)	SW6	Open (not used)
SW3	Open (not used)	SW7	Open (not used)
SW4	Open (not used)	SW8	Open (English language LCD)

IF Processing Module (A3) 1585-1207

1. Select 75Ω input impeadance using jumpers J28 and J29.

2. Select Low Input Impeadance using jumpers J8, J9, J10 and J11.

3. Enable Peak Vs. Average detection by placing J30 into the In position.

4. Enable Frequency Response Correction by placing J2 and J3 into the In position.

2.0 TECHNICAL DESCRIPTION

2.5 Alignment Procedure - continued

5. Set Delay Equilizers and Attenuation Equilizers as follows:

Delay Equlizer1 (J35, J36)	Out
Attenuation Equlizer1 (J37, J38)	Out
Delay Equlizer2 (J43, J44)	Out
Delay Equlizer3 (J31, J32)	Out
Attenuation Equlizer3 (J33, J34)	Out

6. Set filter circuit to Band Pass Filter by placing jumpers J19, J20, J22 and J23 into the BPF position.

7. Select High Output Gain by placing jumpers J26 and J27 into the High position.

8. Remove linear equalization by placing front panel Linear Equalization toggle switch into the out position.

9. Select Manual Gain by placing Gain Selection toggle switch into the Manual position.

LO/Upconverter Module (A5) 1585-1143

1. Place Reference jumper J1 into the External position..

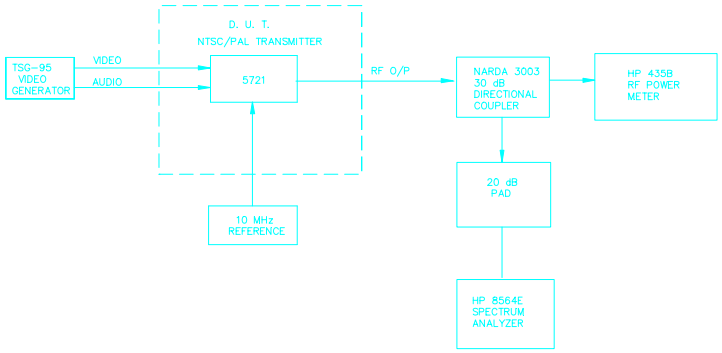
Power Amplifier Module (A6) 1585-1136

1. Select Peak Detection by placing J2 into the Peak position on the Dual Power Detector Module.

2.0 TECHNICAL DESCRIPTION

2.5 Alignment Procedure - continued

Connect the 5721 as shown below:



Power Setup/Meter Calibration

1. Apply power to the tray by placing the rear panel power switch (CB1) into the on position.
2. Measure voltage on Forward Detector Level test point on the Power Amplifier module front panel and adjust for 0 volts using the Forward Zero potentiometer.
3. Measure voltage on Reflective Detected Level test point on the Power Amplifier module front panel and adjust for 0 volts using the Reflected Zero potentiometer.
4. Verify that no faults are displayed on the LCD display on the front panel of the tray.
5. Place transmitter into operate by pressing the Operate button below the LCD display.
6. Set the video generator for a 0IRE no burst test signal and adjust Manual Gain potentiometer on front panel of IF Processing module for 50 watts peak-of-sync as observed on RF power meter.
7. Measure voltage on Forward Detected test point on front panel of Power Amplifier module and adjust for 1 volt using the Forward Level potentiometer.
8. Place transmitter into standby by pressing the Standby button below the font panel LCD display.
9. Remove cable connection from RF output jack (J8) of tray.
10. Place transmitter into operate mode by pressing the Operate button below the front panel LCD display.
11. Measure Reflective Detected Level test point and adjust for 1V using Reflected Level potentiometer.
12. Place transmitter into standby by pressing the Standby button below the front panel LCD display.

2.0 TECHNICAL DESCRIPTION

2.5 Alignment Procedure - continued

13. Reconnect cable to RF output jack (J8) of the tray.

14. Place transmitter into the operate mode by pressing the Operate button below the front panel LCD display.

15. Adjust ALC potentiometer on front panel of IF Processing module for 1 volt on the Forward Detected Level test point on power Amplifier Module.

RF Response

1. Adjust video generator for cable sweep input signal.

2. Adjdust Spectrum Analyzer for the following settings:

Span	10MHz
Resolution BW	100KHz
Video BW	100 KHz
Center Frequency	Channel Frequency

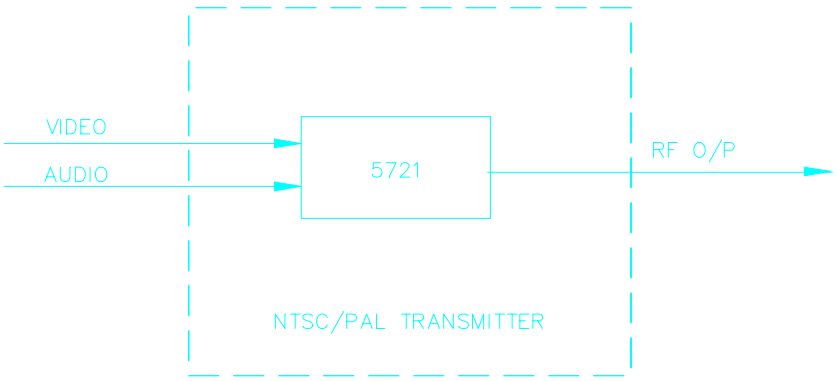
3. Adjust the four Frequency Response potentiometers on the front panel of the IF Processing module for flat response on spectrum analyzer.

2.0 TECHNICAL DESCRIPTION

2.6 Block Diagrams

System Block Diagram:

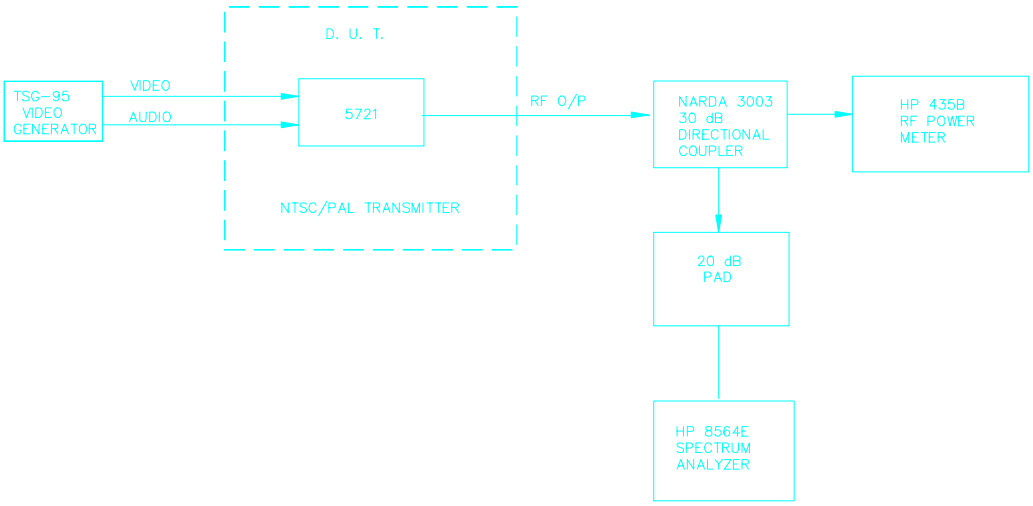
The following is a system block diagram for the 5721 NTSC/PAL transmitter. Detailed Block Diagrams and Schematics are included in Exhibit II.



3.0 ENGINEERING DATA

3.1 RF Power Measurements

The following block diagram describes the test equipment set-up for the following measurement:



With the video generator set for a 0 IRE no burst signal, the output power of the 5721 was adjusted to obtain 10 peak RF output as observed on the power meter.

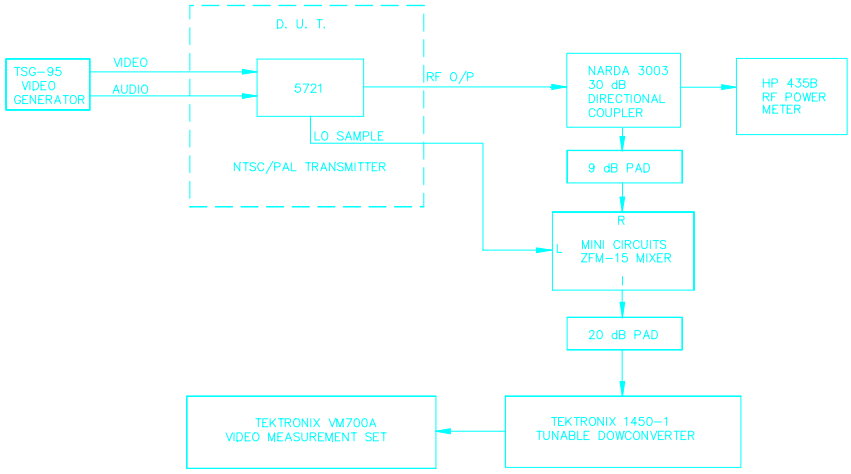
With the power level properly set to 10 watts (peak), all required test were performed and recorded in the following sections.

3.0 ENGINEERING DATA

3.2 Modulation Characteristics

3.2.1 Video Modulation

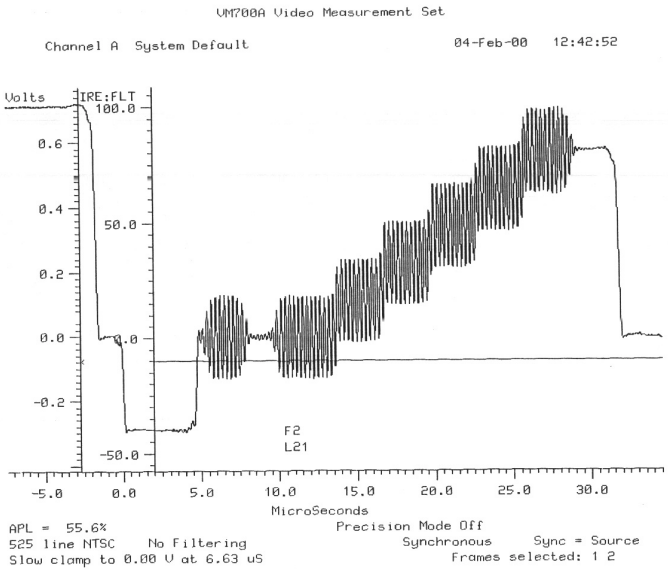
Using the test set-up shown below, The video was adjusted for a modulated staircase, and the differential phase and gain were recorded.



Differential Phase: 1.42°

Differential Gain : 0.85%

This plot of the demodulated stairstep video waveform illustrates the substantially linear transfer characteristic of the transmitter:



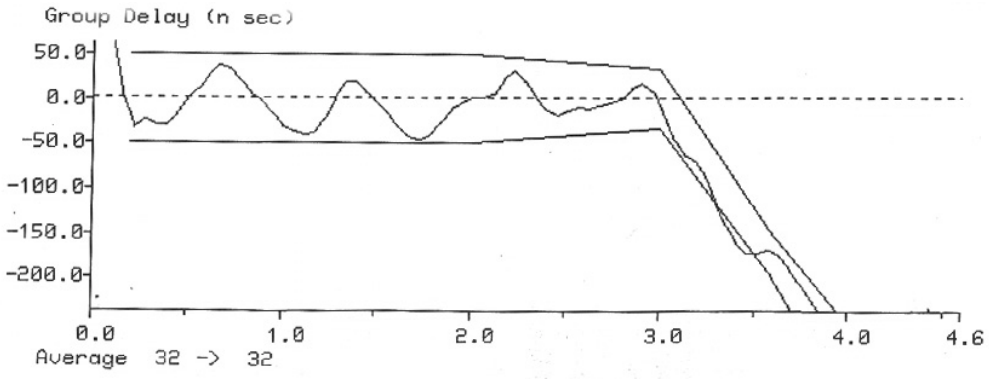
3.0 ENGINEERING DATA

3.2 Modulation Characteristics - continued

3.2.2 Video Envelope Delay

Using the test set-up in section 3.2.1, the envelope delay was measured and the data recorded:

Note: For this test, the video was adjusted to provide a SinX/X video waveform, and the measurement was made with the Tektronix VM700A Video Measurement Set.



Video Frequency	Delay (ns)
150.00 KHz	0 (Reference)
200.00 KHz	- 22
500.00 KHz	- 4
1.00 MHz	- 31
1.50 MHz	- 7
2.00 MHz	- 1
2.50 MHz	- 16
3.00 MHz	- 16
3.25 MHz	- 97
3.50 MHz	- 172
3.58 MHz	- 171
4.00 MHz	- 269
4.18 MHz	- 292

3.0 ENGINEERING DATA

3.2 Modulation Characteristics - continued

3.2.3 Video Noise

Using the test set-up in section 3.2.1, the video was observed on the waveform monitor. The video was set for 1 volt peak-to-peak and the noise was observed on one step of the 5-step staircase to be less than 6 mV peak-to-peak. This is a video peak to noise ratio of 1000/6 = 44.4 dB, or, using the standard conversion factor of peak to RMS noise of 14 dB, about 58.4 dB S:N rms.

Observing the video field rate on the waveform monitor, the low frequency noise (AC line related) was below the measurement threshold of -60 dB.

3.0 ENGINEERING DATA

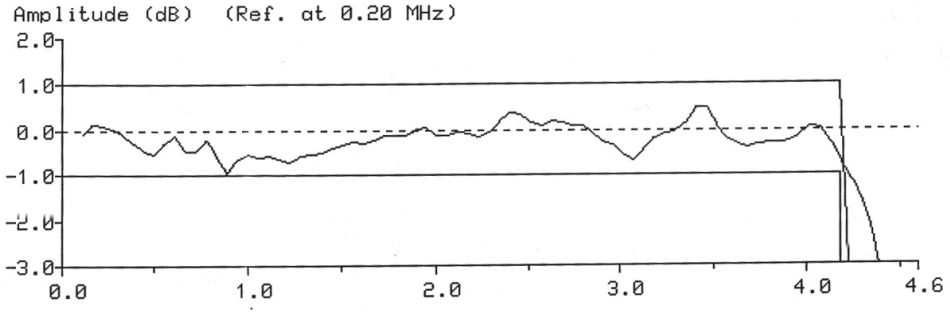
3.2 Modulation Characteristics - continued

3.2.4 Video Frequency Response

Using the test set-up in section 3.2.1, the frequency response was recorded:

Note: For this test, the video signal was adjusted to provide a SIN X/X video waveform, and the measurement was made with the Tektronix VM700A Video Measurement Set.

Video Frequency	Relative Response
200.00 KHz	0.0 dB
500.00 KHz	-0.6 dB
750.00 KHz	-0.4 dB
1.00 MHz	-0.6 dB
1.25 MHz	-0.7 dB
1.50 MHz	-0.4 dB
2.00 MHz	-0.1 dB
2.50 MHz	-0.2 dB
3.00 MHz	-0.5 dB
3.50 MHz	+0.2 dB
3.58 MHz	-0.3 dB
4.00 MHz	-0.1 dB
4.18 MHz	-0.7 dB
4.50 MHz	-6.4 dB



3.0 ENGINEERING DATA

3.2 Modulation Characteristics - continued

3.2.5 RF Sideband Response

Using the test set-up shown in section 3.1, the TSG-95 Video Generator was adjusted to provide a 0 IRE no burst output and the output power of the 5721 transmitter was set to 10 Watts peak, as observed on the power meter.

With the output power set to the proper level, the TSG-95 Video Generator was adjusted to provide a cable sweep test signal and the RF Sideband Response of the transmitter was recorded.

Output Frequency	Video Frequency	Response (dB)
2669.25 MHz	Carrier	-
2669.45 MHz	+200 KHz	0 (reference)
2669.05 MHz	-200 KHz	-3.7
2669.75 MHz	+500 KHz	-4.8
2668.75 MHz	-500 KHz	-4.5
2670.00 MHz	+750 KHz	-4.7
2668.50 MHz	-750 KHz	-4.8
2670.25 MHz	+ 1.0 MHz	-4.8
2668.25 MHz	-1.0 MHz	-12.0
2670.50 MHz	+1.25 MHz	-4.8
2668.00 MHz	-1.25 MHz	-30.3
2670.75 MHz	+1.5 MHz	-4.5
2667.75 MHz	-1.5 MHz	-48.3
2671.25 MHz	+2.0 MHz	-4.2
2667.25 MHz	-2.0 MHz	-47.5
2672.25 MHz	+3.0 MHz	-4.8
2666.25 MHz	-3.0 MHz	-47.8
2672.83 MHz	+3.58 MHz	-4.5
2665.67 MHz	-3.58 MHz	-50.0
2673.25 MHz	+4.0 MHz	-3.67
2665.25 MHz	-4.0 MHz	-48.5
2673.43 MHz	+4.18 MHz	-7.2
2665.07 MHz	-4.18 MHz	-51.3
2673.75 MHz	+4.5 MHz	-23.0
2664.75 MHz	-4.5 MHz	-54.7
2674.00 MHz	+4.75 MHz	-41.0
2664.50 MHz	-4.75 MHz	-51.8
2674.25 MHz	+5.0 MHz	-51.8
2664.25 MHz	-5.0 MHz	-54.2
2676.25 MHz	+7.0 MHz	-53.0

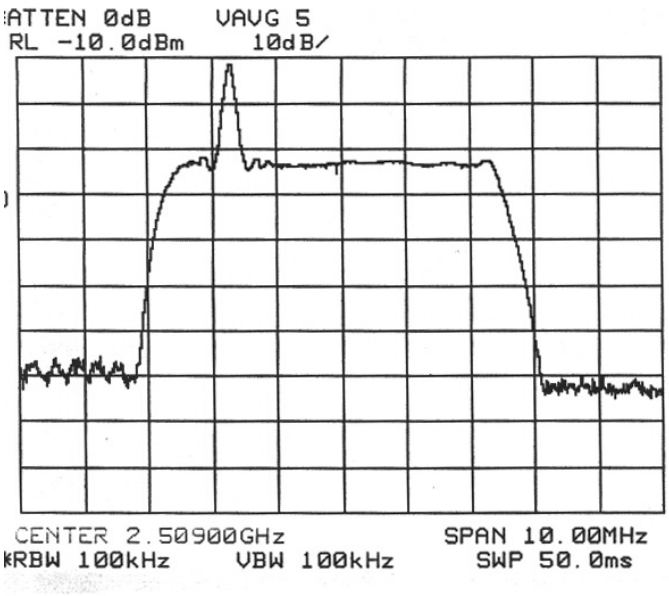
Spectrum analyzer plots are provided on the following page.

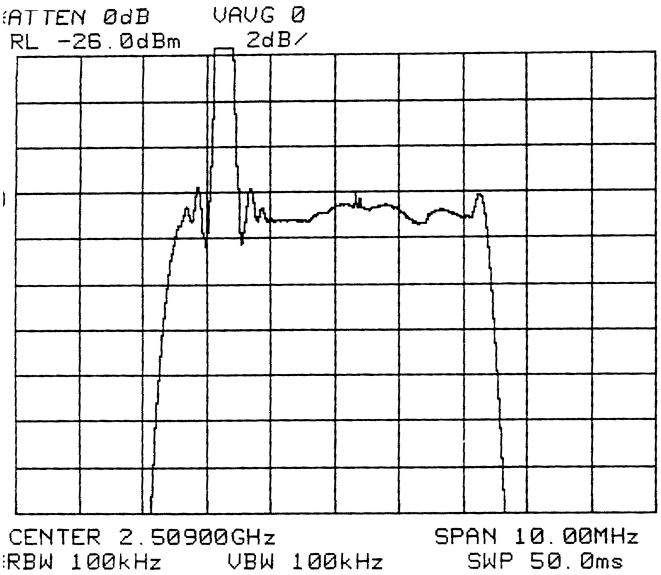
3.0 ENGINEERING DATA

3.2 Modulation Characteristics - continued

3.2.5 RF Sideband Response

Analyzer Plots (RF Sideband Response):



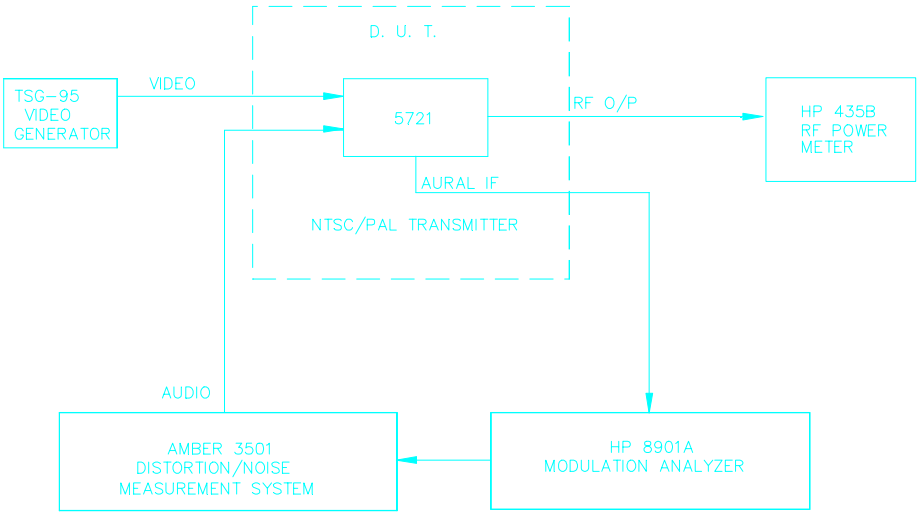


3.0 ENGINEERING DATA

3.2 Modulation Characteristics - continued

3.2.6 Audio Modulation

Using the test set-up below, the FM distortion was measured:



Distortion Measurements:

Audio Frequency	Deviation 6.25 KHz Distortion	Deviation 12.5 KHz Distortion	Deviation 25 KHz Distortion	Deviation 40 KHz Distortion
100 Hz	0.06%	0.04%	0.20%	0.03%
1000 Hz	0.06%	0.03%	0.18%	0.03%
5000 Hz	0.15%	0.07%	0.08%	0.04%
15000 Hz	0.40%	0.22%	0.12%	0.05%

3.0 ENGINEERING DATA

3.2 Modulation Characteristics - continued

3.2.6 Audio Modulation - continued

Using the same test set-up shown above, and maintaining ±25 KHz deviation, the audio input frequency and level were varied and the response was recorded:

Audio Frequency	Audio Level	Response
50 Hz	+10.2 dBm	-0.2 dB
100 Hz	+10.1 dBm	-0.1 dB
400 Hz	+10.0 dBm	0.0 dB
1000 Hz	+9.25 dBm	+0.75 dB
2000 Hz	+7.5 dBm	+2.5 dB
5000 Hz	+2.5 dBm	+7.5 dB
10000 Hz	-2.8 dBm	+12.8 dB
15000 Hz	-7.0 dBm	+17.0 dB

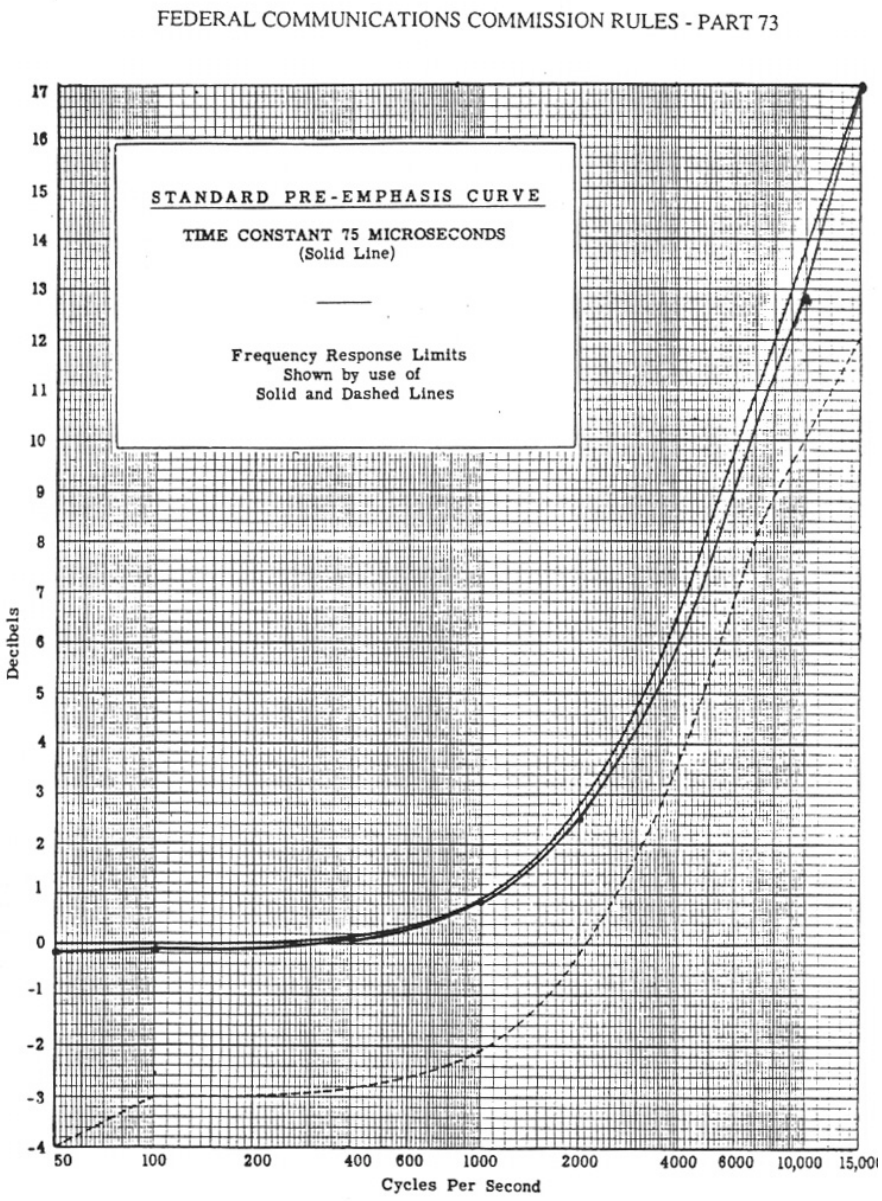
This data is plotted on the graph on the following page.

3.0 ENGINEERING DATA

3.2 Modulation Characteristics - continued

3.2.6 Audio Modulation - continued

Audio Frequency Response Plot:

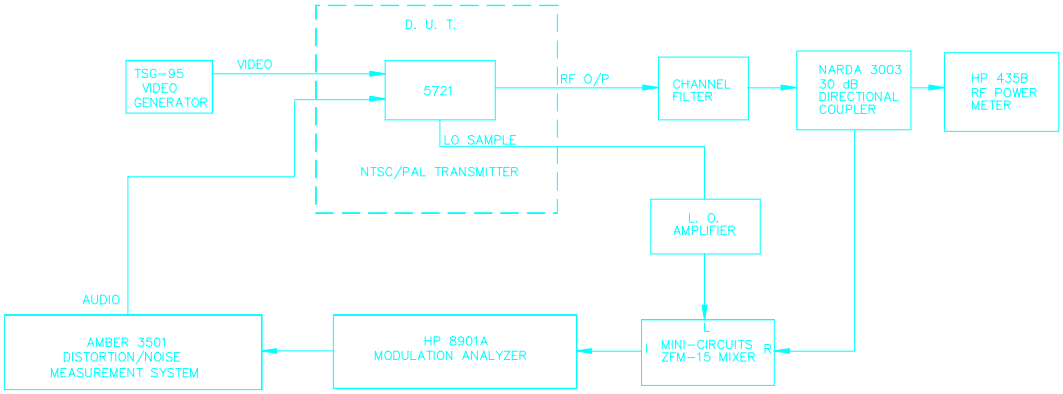


3.0 ENGINEERING DATA

3.2 Modulation Characteristics - continued

3.2.7 AM and FM Noise

Using the following test set-up, the AM and FM noise was recorded.



NOISE MEASUREMENTS

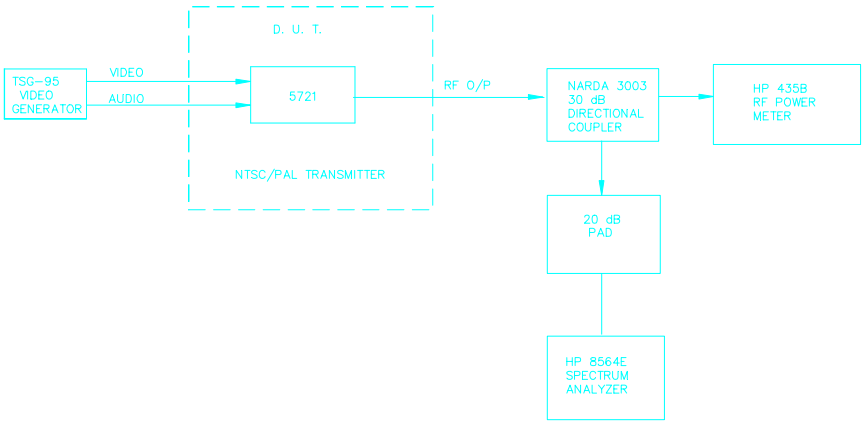
AM Noise 55 dB
FM Noise 60 dB

3.0 ENGINEERING DATA

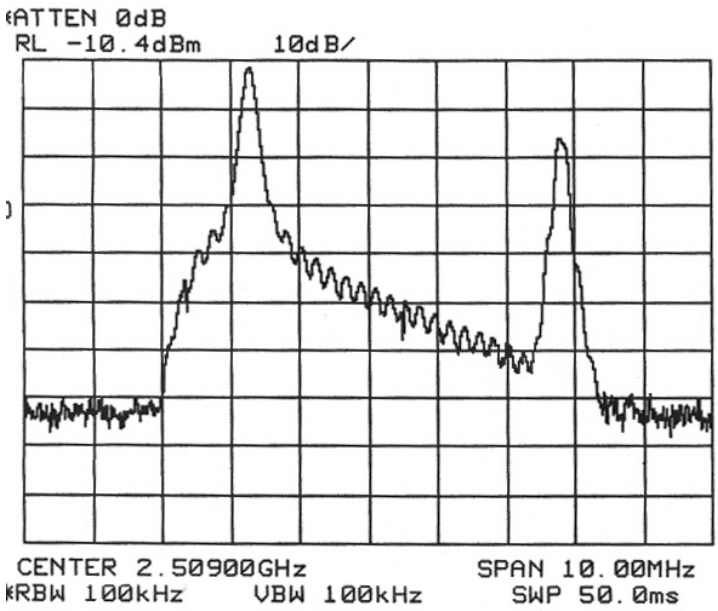
3.3 Occupied Bandwidth

Using the following test set-up, the transmitter was operated at maximum power and a plot of the transmitter occupied bandwidth spectrum was taken and is shown below.

For these measurements a 0 IRE black video input was applied and the aural deviation was adjusted to ±25 KHz. Plots of the visual and aural occupied bandwidth are shown below.



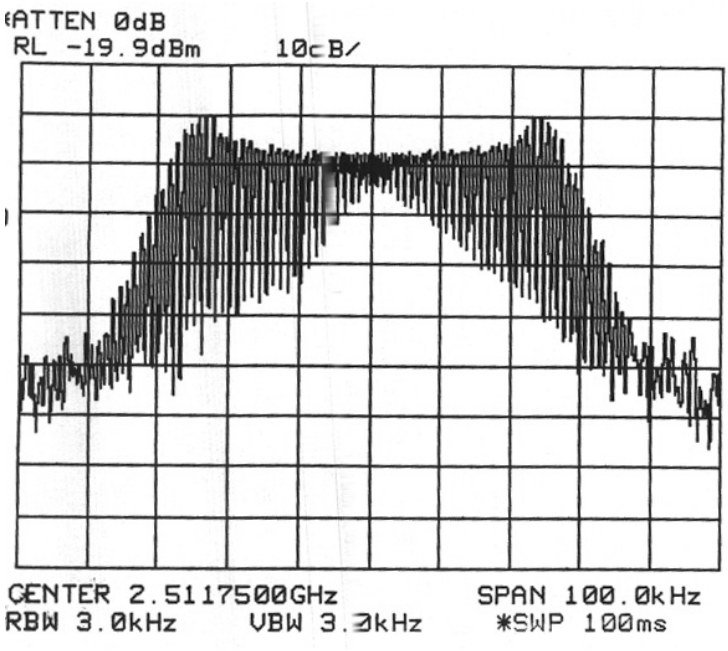
Spectrum Analyzer Plot (Occupied Bandwidth):



3.0 ENGINEERING DATA

3.3 Occupied Bandwidth - continued

Spectrum Analyzer Plot (Aural Carrier Occupied Bandwidth):

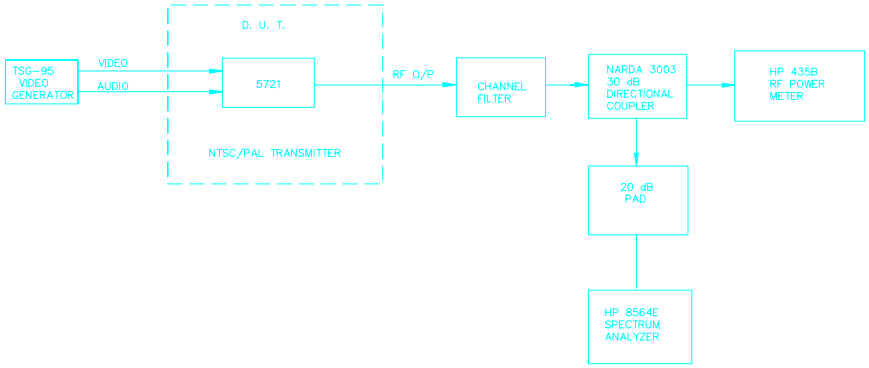


3.0 ENGINEERING DATA

3.4 Out-of-Band Power

Using the test set-up shown below, the spectrum outside of the specified channel was observed and the data was taken on all products above the -70 dB noise floor of the spectrum analyzer. The measured data is shown in the table on the following page for 20 watts peak output power.

Spurious Emissions were observed on the analyzer at both 20 MHz and 40 MHz span (see spectrum plots on the following page). With the peak visual carrier set as the reference, the spurious emissions were observed. The measured data is shown in the table below for 20 watts peak output power.

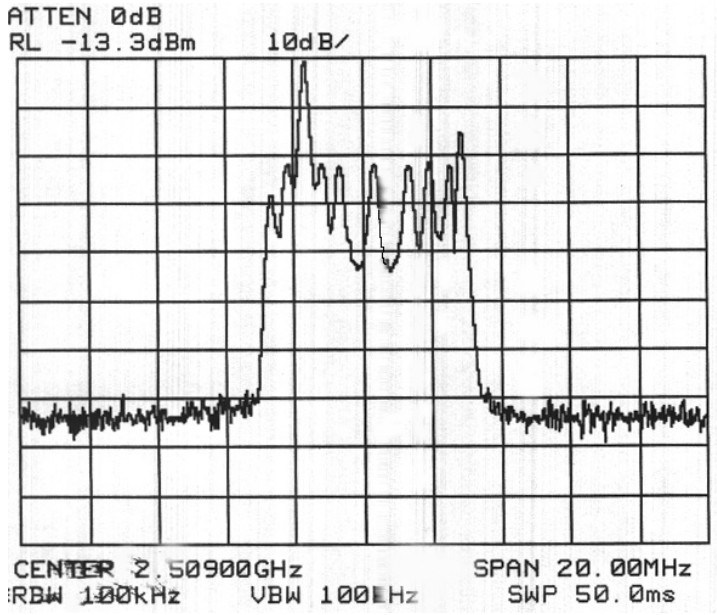


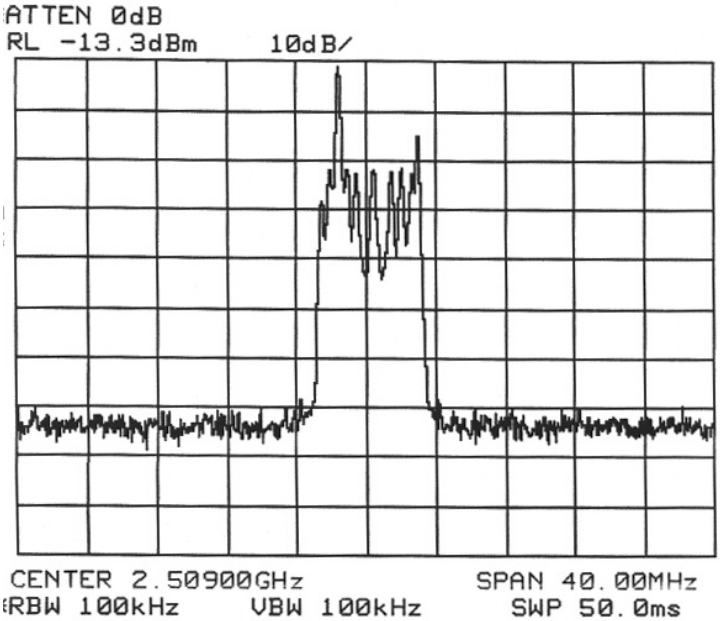
Frequency	Source	Level Observed
2760.75 MHz	Image Visual Carrier	None Observed
2756.25 MHz	Image Aural Carrier	None Observed
2715.00 MHz	Local Oscillator	None Observed
2660.25 MHz	-9 MHz Product	None Observed
2664.75 MHz	-4.5 MHz Product	-68.0 dB
2673.75 MHz	Aural Carrier	-15.0 dB
2669.25 MHz	Visual Carrier	0 dB (reference)
2678.25 MHz	+9 MHz Product	None Observed
2665.67 MHz	-3.58 MHz Product	None Observed
5338.50 MHz	2nd Harmonic-Visual. Carrier	None Observed
5347.50 MHz	2nd Harmonic-Aural Carrier	None Observed
8007.75 MHz	3rd Harmonic-Visual Carrier	None Observed
8021.25 MHz	3rd Harmonic-Aural Carrier	None Observed
10677.00 MHz	4th Harmonic-Visual Carrier	None Observed
10695.00 MHz	4th Harmonic-Aural Carrier	None Observed
13346.25 MHz	5th Harmonic-Visual Carrier	None Observed
13368.75 MHz	5th Harmonic-Aural Carrier	None Observed
16015.50 MHz	6th Harmonic-Visual Carrier	None Observed
16042.50 MHz	6th Harmonic-Aural Carrier	None Observed
18684.75 MHz	7th Harmonic-Visual Carrier	None Observed
18716.25 MHz	7th Harmonic-Aural Carrier	None Observed
21354.00 MHz	8th Harmonic-Visual Carrier	None Observed
21390.00 MHz	8th Harmonic-Aural Carrier	None Observed
24023.25 MHz	9th Harmonic-Visual Carrier	None Observed
24063.75 MHz	9th Harmonic-Aural Carrier	None Observed
26692.50 MHz	10th Harmonic-Visual Carrier	None Observed
26737.50 MHz	10th Harmonic-Aural Carrier	None Observed

3.0 ENGINEERING DATA

3.4 Out-of-Band Power - continued

Spectrum Analyzer Plots (Out-of-Band Power):





3.0 ENGINEERING DATA

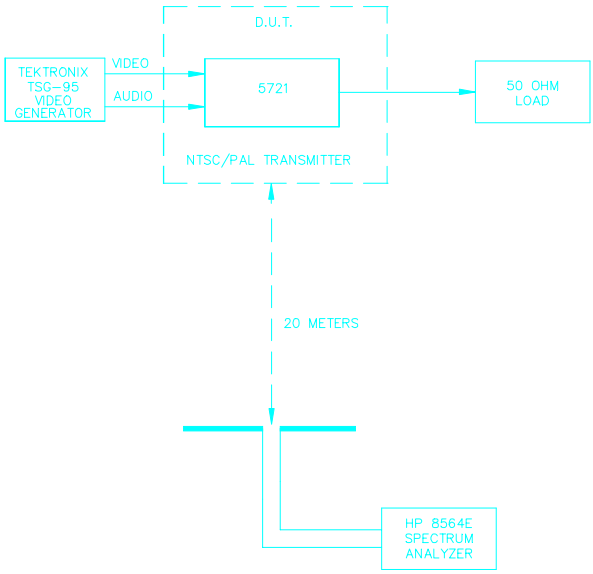
3.5 Radiated Emissions

Using the test set-up below, with the transmitter operating at 10 watts peak output power, the spectrum analyzer was moved 20 meters from the transmitter and connected to a dipole antenna cut to the carrier frequency (2507.25 MHz). This antenna was oriented to maximize the received level, and the data was recorded. The antenna was then cut to the Aural carrier frequency, IF frequency, local oscillator frequency, and the second through the tenth harmonic frequencies of the Visual and Aural carriers and all signals received were maximized by antenna orientation, and their absolute levels were recorded.

With these various antennas the data was taken and recorded in the table on the following page.

Note: The spectrum analyzer had a maximum sensitivity of -100 dBm during these test.

Test Set-up:



3.0 ENGINEERING DATA

3.5 Radiated Emissions - continued

MEASURED LEVELS

Frequency	Source	Level Observed
45.75 MHz	IF	None Observed
2553.00 MHz	Local Oscillator	None Observed
2511.75 MHz	Aural Carrier	-80 dBm
2507.25 MHz	Visual Carrier	-70.0 dBm
5014.50 MHz	2nd Harmonic-Visual. Carrier	None Observed
5023.50 MHz	2nd Harmonic-Aural Carrier	None Observed
7521.75 MHz	3rd Harmonic-Visual Carrier	None Observed
7535.25 MHz	3rd Harmonic-Aural Carrier	None Observed
10029.00 MHz	4th Harmonic-Visual Carrier	None Observed
10047.00 MHz	4th Harmonic-Aural Carrier	None Observed
12536.25 MHz	5th Harmonic-Visual Carrier	None Observed
12558.75 MHz	5th Harmonic-Aural Carrier	None Observed
15043.50 MHz	6th Harmonic-Visual Carrier	None Observed
15070.50 MHz	6th Harmonic-Aural Carrier	None Observed
17550.75 MHz	7th Harmonic-Visual Carrier	None Observed
17582.25 MHz	7th Harmonic-Aural Carrier	None Observed
20058.00 MHz	8th Harmonic-Visual Carrier	None Observed
20094.00 MHz	8th Harmonic-Aural Carrier	None Observed
22565.25 MHz	9th Harmonic-Visual Carrier	None Observed
22605.75 MHz	9th Harmonic-Aural Carrier	None Observed
25072.50 MHz	10th Harmonic-Visual Carrier	None Observed
25117.50 MHz	10th Harmonic-Aural Carrier	None Observed

3.0 ENGINEERING DATA

3.5 Radiated Emissions - continued

The measured levels were then compared to the following reference level:

If all of the transmitter's power (20 Watts) was radiated by an isotropic radiator, the power density at 20 meters would be:

$$Pd = Pt/4\pi R^2 = 10/4\pi (20)^2 \cong 1.989 \times 10^{-3} \text{ w/m}^2$$

Using a dipole transmitting antenna increases this by 1.64 to:

$$1.64 * 1.989 \times 10^{-3} = 3.263 \times 10^{-3} \text{ w/m}^2$$

If a dipole receive antenna of area $1.64 * \lambda^2/4\pi$ is used to receive the signal, the received level would be:

$$3.263 \times 10^{-3} * 1.64 * \lambda^2/4\pi = 5.96 \times 10^{-6} \text{w} = -52 \text{ dBw} = -22 \text{ dBm}$$

The receive levels were therefore at the following relative levels:

Frequency	Relative Measured Level (Ref = -22 dBm)
2511.75 MHz	**-58 dBc**
2507.25 MHz	**-48 dBc**

3.0 ENGINEERING DATA

3.6 Frequency Stability

The5721 is designed to operate using an external 10 MHz precise reference oscillator. The frequency stability of this external reference determines the frequency stability of the transmitter.

The frequency determining variables of the transmitter may be defined as follows:

F_{LO} = Desired local oscillator frequency
F_{IF} = Desired IF oscillator frequency
F_R = Desired external reference oscillator frequency
F_{RF} = Desired RF output frequency
E_{LO} = Local oscillator frequency offset error
E_{IF} = IF oscillator frequency offset error
E_R = External reference oscillator frequency offset error
E_{RF} = RF output frequency error

The PLL circuitry maintains a constant ratio between the external reference frequency and the output frequency of the oscillator. This ratio is defined below for both the LO and IF oscillators.

$G_{LO} = F_{LO}/F_R$
$G_{IF} = F_{IF}/F_R$

Any change in the external 10 MHz reference will effect a corresponding change in the output frequency such that the above ratios are maintained.

$$G_{LO} = (F_{LO} + E_{LO})/(F_R + E_R) = F_{LO}/F_R$$

$$G_{IF} = (F_{IF} + F_{IF})/(F_R + E_R) = F_{IF}/F_R$$

Solving for the change in output frequency yields:

$$E_{LO} = E_R * (F_{LO}/F_R) = E_R * G_{LO}$$

$$E_{IF} = E_R * (F_{IF}/F_R) = E_R * G_{IF}$$

The desired RF carrier frequency is equal to the LO frequency minus the IF frequency:

$$F_{RF} = F_{LO} - F_{IF}$$

The actual RF frequency, including any error introduced by the external reference, may be defined as follows:

$F_{RF} + E_{RF} = (F_{LO} + E_{LO}) - (F_{IF} + E_{IF})$
$F_{RF} + E_{RF} = (F_{LO} + F_{IF}) - (E_{LO} - E_{IF})$
$F_{RF} + E_{RF} = F_{RF} + (E_{LO} - E_{IF})$

3.0 ENGINEERING DATA

3.6 Frequency Stability - continued

Calculating for the error of the RF carrier yields:

$E_{RF} = (E_{LO} - E_{IF})$
$E_{RF} = E_R * G_{LO} - E_R * G_{IF}$
$E_{RF} = E_R (G_{LO} - G_{IF})$
$E_{RF} = E_R/F_R * (F_{LO} - F_{IF})$
$E_{RF} = E_R/F_R * F_{RF}$

Therefore, the error of the RF carrier is a function of the external 10 MHz reference error.

The maximum RF frequency error for this service is ±1.0 KHz. The highest channel frequency for this service (G4 = 2681.25 MHz) represents the worst case condition. With these values the maximum allowable reference error ($E_{R(max)}$) can be calculated.

$E_{R(max)} = 3.73$ Hz

The required reference oscillator stability may be calculated as follows:

Stability = $E_{R(max)}/F_R$
Stability = 3.73 Hz/10 x 10^6 Hz = 0.373 x 10^{-6}

Therefore, the RF frequency error of the ITS-5721 will not exceed ±1.0 KHz when operated with a precise reference oscillator with a stability equal to or better than 0.373 x 10^{-6}.

Commercially available GPS precise reference oscillators, such as the TRAK Systems 8821 which has a frequency stability of 1 x 10^{-11} over a temperature range of -10 to 50 °C, and a line voltage/frequency range from 85 to 265 VRMS/48 to 440 Hz (see TRAK Systems 8821 specifications on the following pages), insure a frequency stability within the tolerance specified in the Rules and Regulations for this service.

TRAK SYSTEMS DIVISION OF **TRAK MICROWAVE**

GPS Clock

Model 8821A (1-3/4") and B (3-1/2")

- **Accurate Time and Frequency with Just One Satellite**
- **Parallel Tracking of Six Satellites**
- **Oscillator Disciplined to GPS**
- **Choice of Oscillator Options**
- **5 MHz, 10 MHz, 1.544 MHz, or 2.048 MHz Outputs**
- **PC Software Disk for Setup and Output**
- **1 PPS Output Sync Within 1 Microsecond of GPS**
- **IRIG B Modulated and DC Output Options**
- **Form - C Relay and TTL Status Outputs**
- **Dual RS-232 Ports**
- **85 - 265 Vac or 100 - 370 Vdc Operation (24 or 48 Vdc Optional)**

The Model 8821 GPS Clock is a reduced-cost version of TRAK Systems' extremely successful Model 8812 and 8820 GPS Station Clocks. This versatile unit incorporates a six-channel parallel GPS receiver, a disciplined crystal oscillator, and a precise time and frequency generator in a single assembly. Phase offset of the 1 PPS output, referenced to UTC, is typically less than one microsecond when one or more satellites are being tracked.

The unit operates from 85 - 265 Vrms, 48-440 Hz or 100-370 Vdc, voltage ranging is automatic. No strapping or switchover is required. Optional power inputs include 24 Vdc and 48 Vdc.

The Model 8821 incorporates automatic oscillator calibration by GPS, automatic leap second correction and built-in calendar for automatic leap year updates. By using the remote setup feature, the operator may set up for automatic daylight savings time corrections. These features, a very high MTBF, and an RS-232 remote status monitoring feature virtually eliminate the need for site visits for setup, calibration, and maintenance.

The unit is supplied with a monitor and control application program for DOS-based computers. Program is normally supplied on a 3-½ inch floppy disk.

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MODEL 8821 SPECIFICATIONS

Internal Oscillator Options

E4A (Standard Model 8821A OCXO)

Accuracy while Tracking: (one-hour averaging)	<1 X 10^{-11}
Aging rate when coasting*:	<5 X 10^{-9}/day
1 PPS coasting drift*: (first 8 hours)	<6 µs/hour
Phase noise @ 10 Hz offset	<-100 dBc
Phase noise @ 100 Hz offset	<-130 dBc
Phase noise @ 1 KHz offset	<-135 dBc
Phase noise @ 10 KHz offset	<-140 dBc
Harmonic distortion	<-40 dBc
Non-Hormonic distortion	<-100 dBc

B7A (Standard Model 8821B OCXO)

Accuracy while Tracking: (one-hour averaging)	<1 X 10^{-11}
Aging rate when coasting*:	<5 X 10^{-10}/day
1 PPS coasting drift*: (first 8 hours)	<500 ns/hour
Phase noise @ 10 Hz offset	<-105 dBc
Phase noise @ 100 Hz offset	<-125 dBc
Phase noise @ 1 KHz offset	<-140 dBc
Phase noise @ 10 KHz offset	<-145 dBc
Harmonic distortion	<-30 dBc
Non-Hormonic distortion	<-100 dBc

Other Frequencies

Option B7 also available for output of 1.544 MHz, 2.048 MHz, or 5 MHz from the Model8821B.

Synchronization

The position of the antenna is determined by measuring the pseudo-range to four satellites and computing the position of these satellites using ephemeris data.

*Coasting factors apply only if there has been an antenna or receiver failure or if antenna is blocked from view of all satellites.

The receiver basic specifications are as follows:

Receiver Description:	L1 C/A code pseudo-ranging
Channels:	Six independent, continuous tracking channels
Frequency:	1575.42 MHz
Acquisition Time:	Typically less than two minutes

Navigation Outputs

Latitude, longitude, and height with a position accuracy of ± 30 meters, 2 drms (without SA) are available on the RS-232 ports.

Tracking Modes

In its default tracking mode, the Model 8821 automatically tracks one to six satellites, as available, on a stationary platform.

Two other modes, one for use on a moving platform and the other for use with an operator-entered fixed position, can be selected.

Timekeeping

The Model 8821 normally accumulates Universal Time (UTC). By command, this may be changed to local time. When local time is used, automatic daylight savings time adjustments are made at preprogrammed dates. Leap second and leap year adjustments are made automatically. Time is available on the RS-232 ports with a resolution of one millisecond.

Optional IRIG B Output**

Format:	Modulated IRIG B 122
Level:	3 Vpp nominal
Drive:	Will drive 50 ohms
Mod. Ratio:	Adjustable 2:1 to 6:1
Phase:	Modulated code on-time mark adjustable to within ± 10 microseconds of on-time reference.

** Rate and IRIG B outputs are a single option. Not available separately

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Optional Rate/DC Code Output**

Frequency:	One of the following may be selected: 1 PPH, 6 PPH, 12 PPH, 1 PPM, or 1 PPS - 1 MPPS in decade steps. IRIG B DC may be output in place of a selected rate.
Levels:	TTL
Drive:	50 ohms
Coherence:	Within one microsecond of UTC
Connector:	BNC

1 PPS Output

Levels:	TTL
Pulsewidth:	100 microseconds
Drive:	50 ohms
Coherence:	Within one microsecond of UTC
Connector:	BNC

High Rate Output (Sinewave)

Frequency:	Same as internal oscillator (10 MHz standard, others optional)
Level:	1 Vrms ± 10%
Drive:	50 ohms
Coherence:	Phase coherent to 1 PPS
Connector:	BNC

Optional Output Frequencies
Other available frequency outputs (Model 8821B only) include 5 MHz, 1.544 MHz, and 2.048 MHz.

Optional TTL Rate Output
TTL levels on High Rate Output in place of sinewave. Drive is 50 ohms.

Status Output
Three contacts of a Form-C relay provide tracking status output on a 9-pin connector. Contact rating is 1/2 amp. Also on this connector is status at TTL logic levels.

Remote Setup and Status
The following is a partial list of setup and status commands via the RS-232 Port.

Set/Request UTC/LOCAL
Set/Request local time offset
Set/Request daylight savings dates
Set/Request output rate
Set/Request local position
Set/Request minimum tracking elevation
Request time output
Request navigation data
Request tracking/locked status
Request time offset data
Request leap second status
Request satellites being tracked
Request firmware version

Time/Status Display (option)
The unit can be ordered with an LED display of time and status.

Power Supply
The unit operates on 85-265 Vrms, 48-440 Hz, or 100-370 Vdc. Power required is 25 watts nominal. Options available for 24 or 48 Vdc in place of ac.

Internal Battery
An internal lithium battery maintains GPS module stored data and coarse timekeeping during time that no external power is applied.

Physical
Model 8821A chassis is 19" wide X 1.72" high X 9" deep. Model 8821B chassis is 3.47 inches high. Weight is 9 pounds.

Antenna unit is 4.25 inches in diameter X 6.5 inches high. Weight is 7 ounces. It is connected to the main chassis via a coaxial cable. A 50 foot cable with TNC connectors is supplied. Optional lead-in systems with coaxial cables and in-line amplifiers are available to 2500 feet. Refer to application note AN-3A for complete details.

Temperature

Main unit:	-10 to + 50° C
Antenna:	-40 to + 70° C

See Page 2 for notes.

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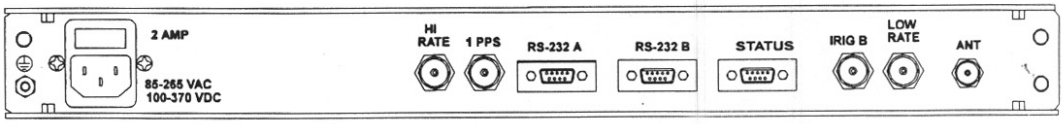
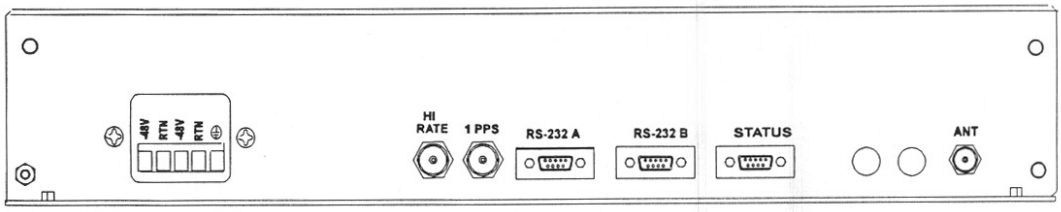
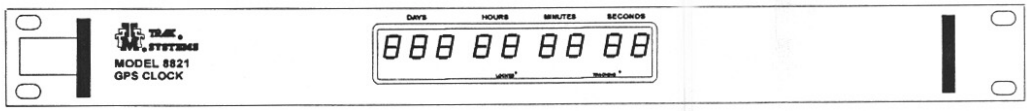
Typical Views



Model 8821A Rear Panel (with Code/Low Rate Option)



Model 8821B Rear Panel (with 48 Vdc Power Option)



Model 8821A with Display Option

Specification subject to change without notice.

Printed in U.S.A., January, 1996

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3.0 ENGINEERING DATA

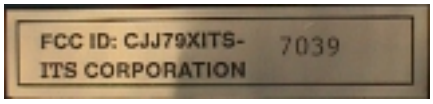
3.7 Test Equipment

MODEL	MANUFACTURER	DESCRIPTION		SERIAL #
8564E	Hewlett Packard	Spect. Analyzer 9 KHz-40 GHz		Rental
8595E	Hewlett Packard	Spect. Analyzer 9 kHz- 6.5GHz		3543A01613
3003-30	Narda	Directional Coupler	41991	
435B	Hewlett Packard	RF Power Meter	2732009080	
2349A	Hewlett Packard	30 Watt Power Head		3318A05525
2230	Tektronix	Oscilloscope		2230B025251
1992	Racal-Dana	Frequency Counter		950304
8135	Bird	50 Ohm Termination		8520
79	Fluke	Digital Multimeter		56660032
F-11-CHM-2-2	Thermotron	Temperature Test Chamber		5737
TEK-95	Tektronix	Video Generator		B0109999
VM700A	Tektronix	Video Measurement Set		B020724
1450-1	Tektronix	Television Demodulator		B020540
2022D	Marcone Instruments	Signal Generator	119168/061	
31732	California Amplifier	31 Channel Downconverter		6280121184

4.0 IDENTIFICATION LABELS/LABEL PLACEMENT AND PHOTOGRAPHS

4.1 Rear Panel FCC Identification Label:

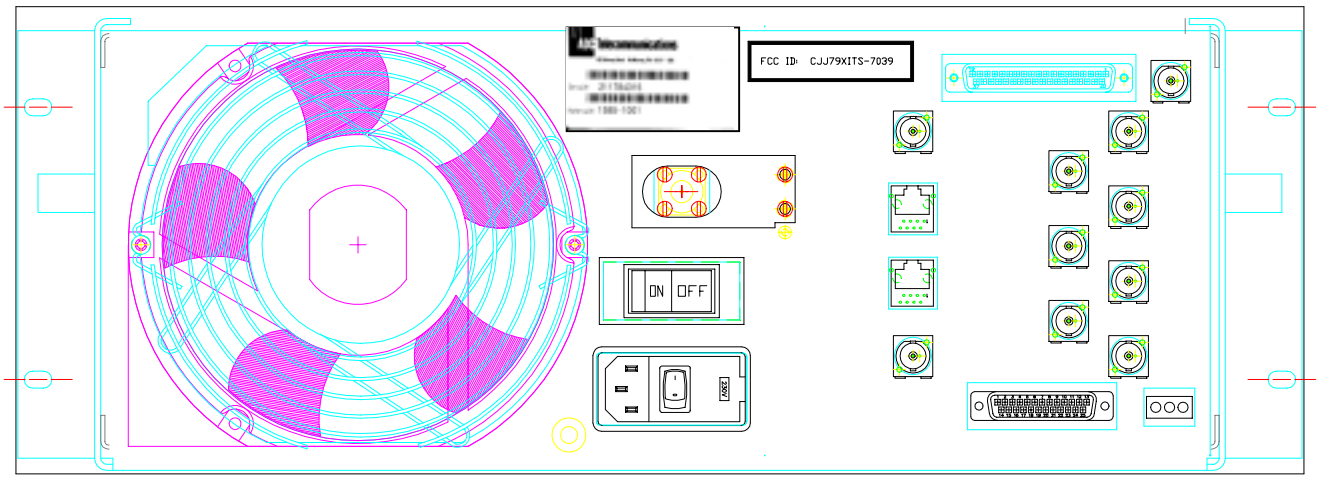
Note: The following Identification Labels and Label Placement Drawing can also be found in the Labels attachment.



4.2 Rear Panel ADC Telecommunications Manufacturer's Label:

4.0 IDENTIFICATION LABELS/LABEL PLACEMENT AND PHOTOGRAPHS

4.3 Rear Panel Drawing (Label Placement):



4.0 IDENTIFICATION LABELS/LABEL PLACEMENT AND PHOTOGRAPHS

4.4 Photograph List

Note: The following photos can also be found in the external photos attachment:

4.4.1 Front view, 5721 Transmitter (Closed Front Panel).

4.4.2 Front view, 5721 Transmitter (Open Front Panel).

4.4.3 Rear view, 5721 Transmitter.

Note: The following photos can also be found in the internal photos attachment:

4.4.4 Top view, IF Processing Module.

4.4.5 Top view, Local Oscillator/Upconverter Module.

4.4.6 Top view, Power Supply Module.

4.4.7 Top view, Transmitter Control and Monitoring Module.

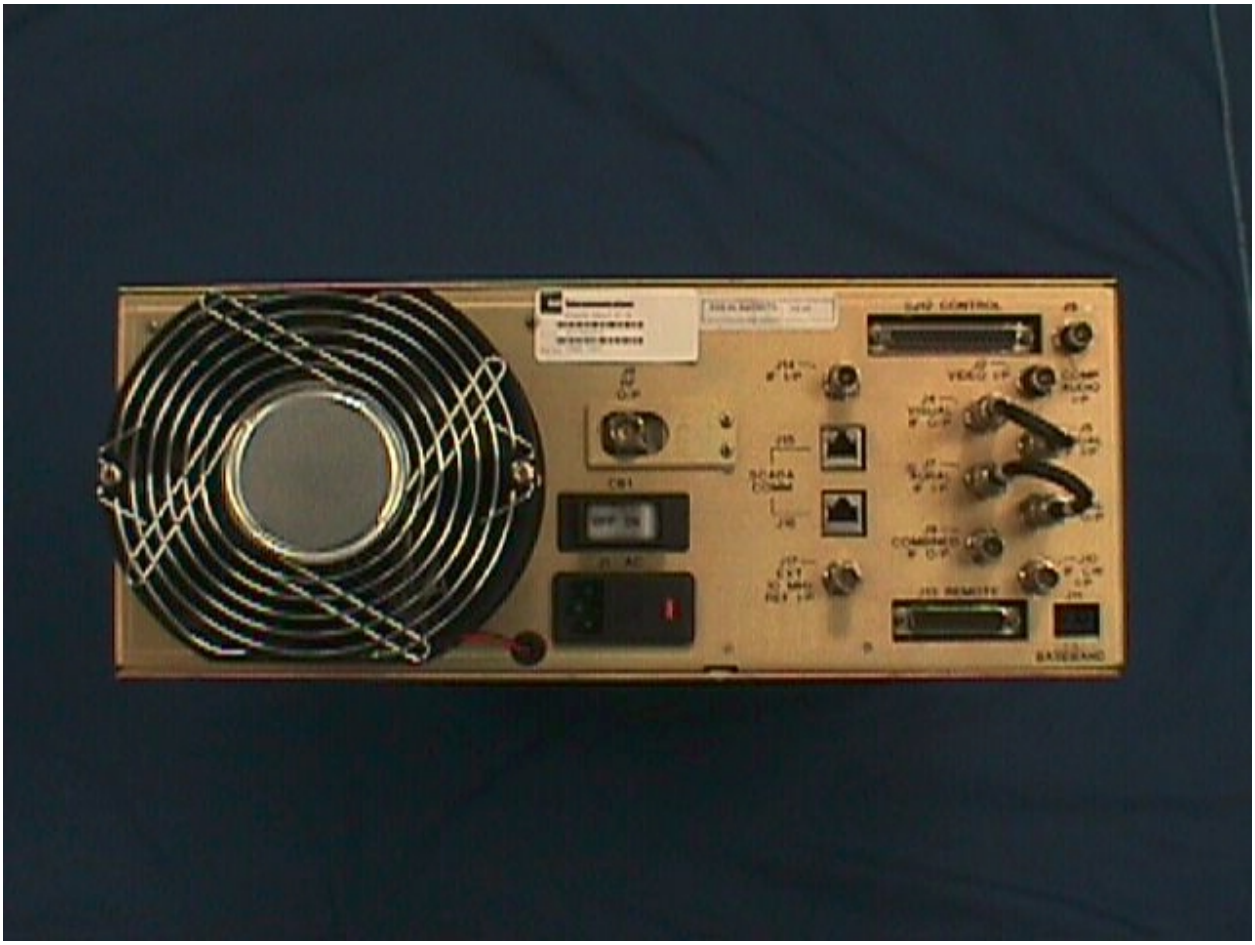
4.4.8 Top view, Power Amplifier Module.

.4.9 Top view, NTSC Modulator Module.

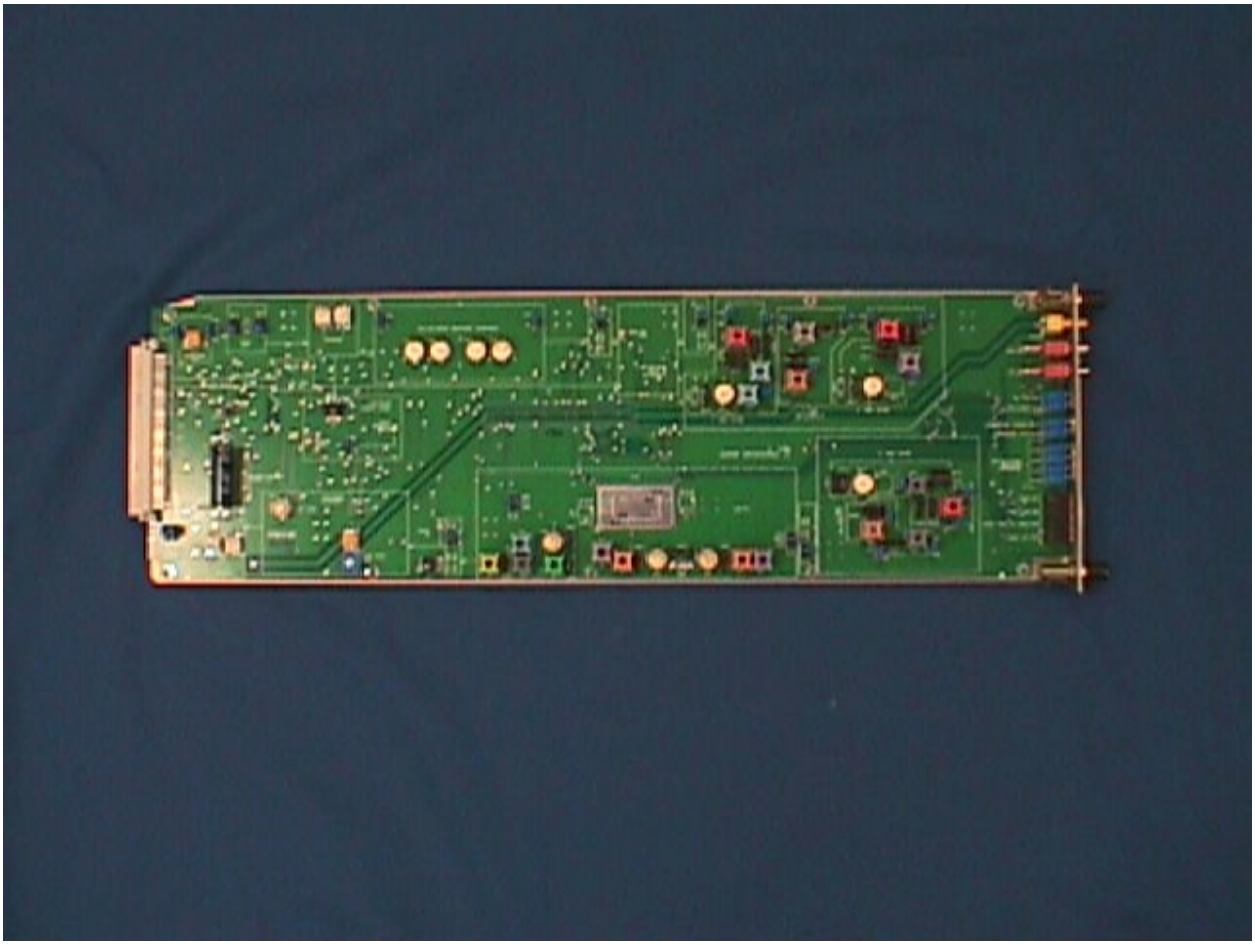
4.4.1 Front view, 5721 Transmitter (Closed Front Panel)

4.4.2 Front view, 5721 Transmitter (Open Front Panel)

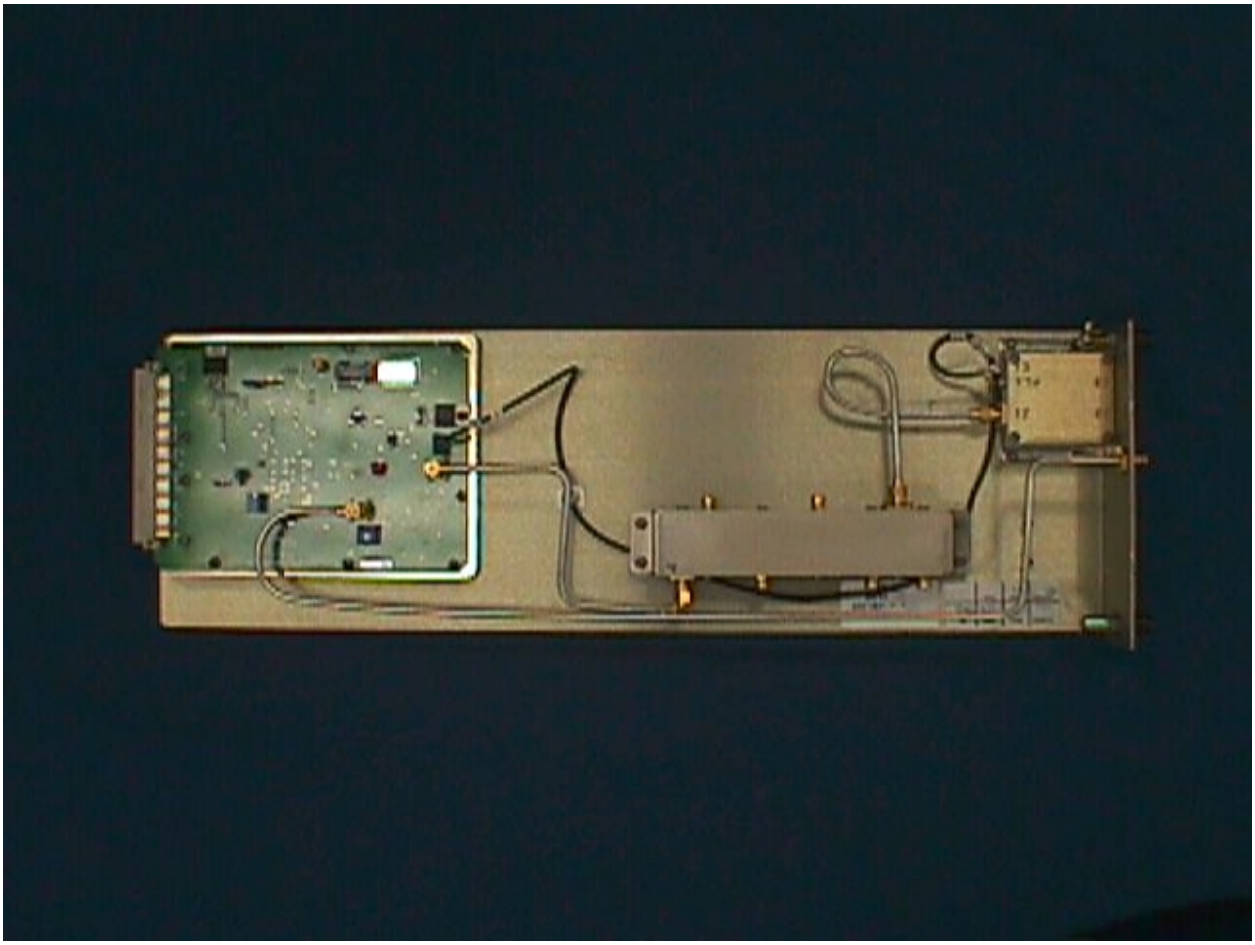
4.4.3 Rear view, 5721 Transmitter



4.4.4 Top view, 5721, IF Processing Module

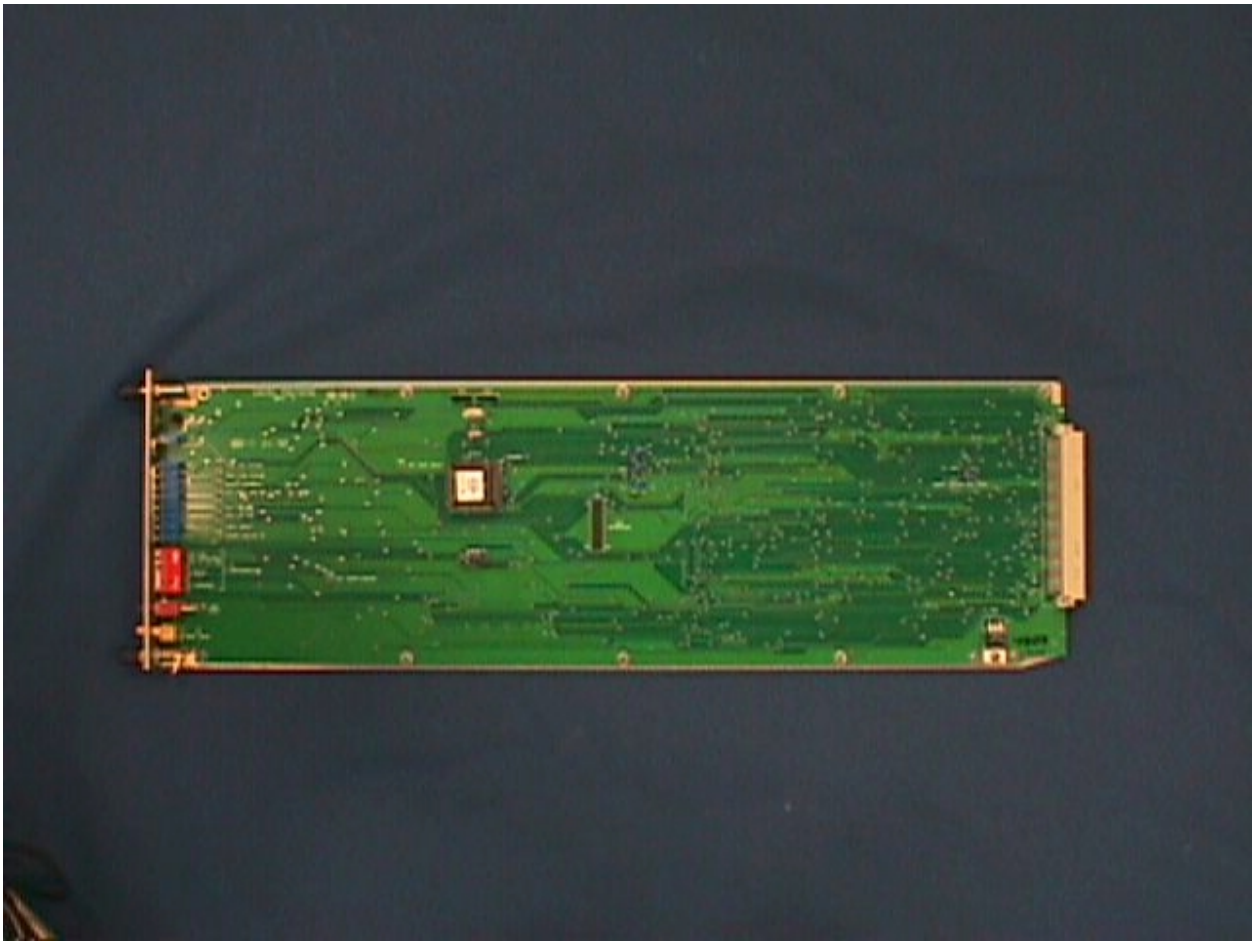


4.4.5 Top view, 5721, Local Oscillator/Upconverter Module

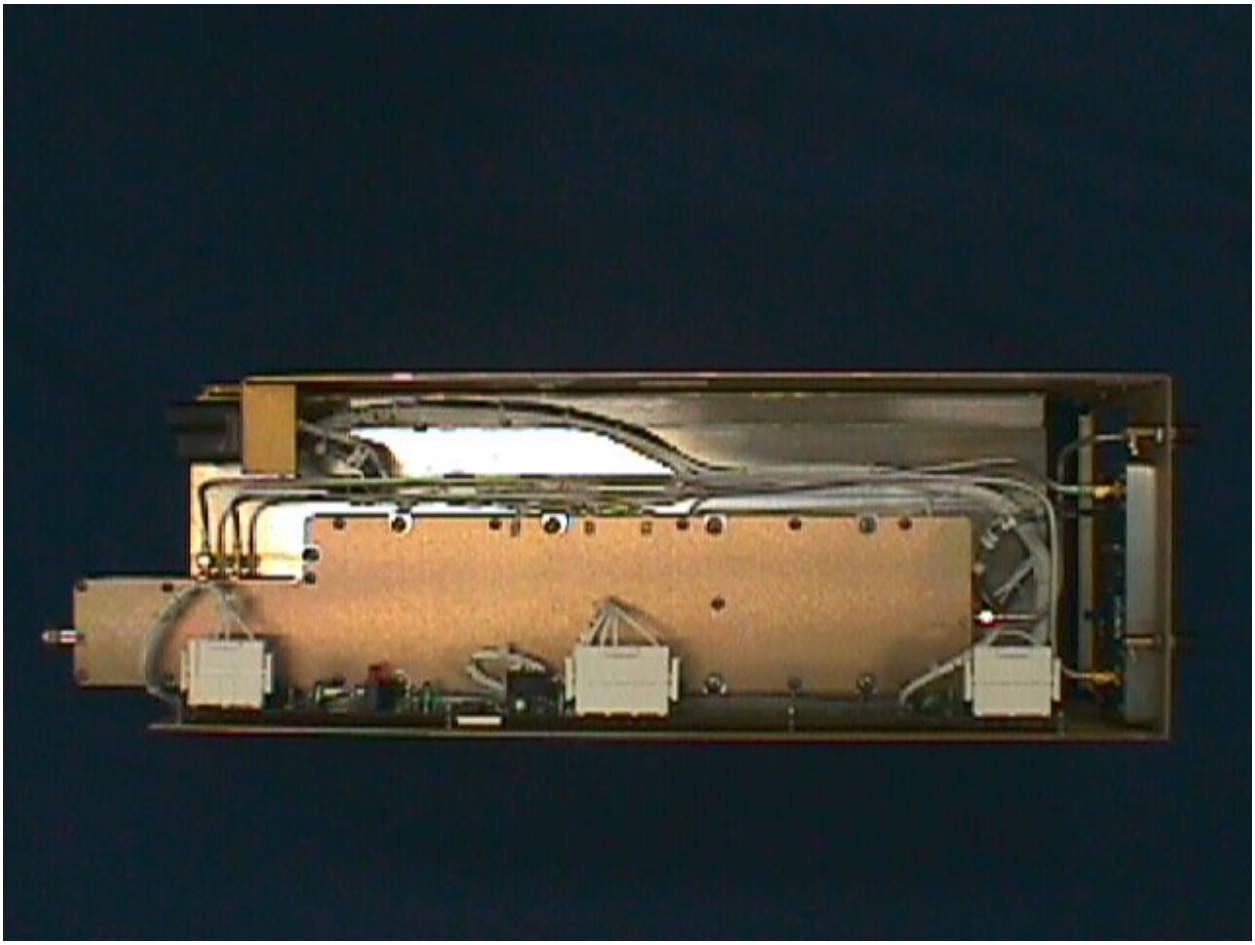


4.4.6 Top view, 5721, Power Supply Module

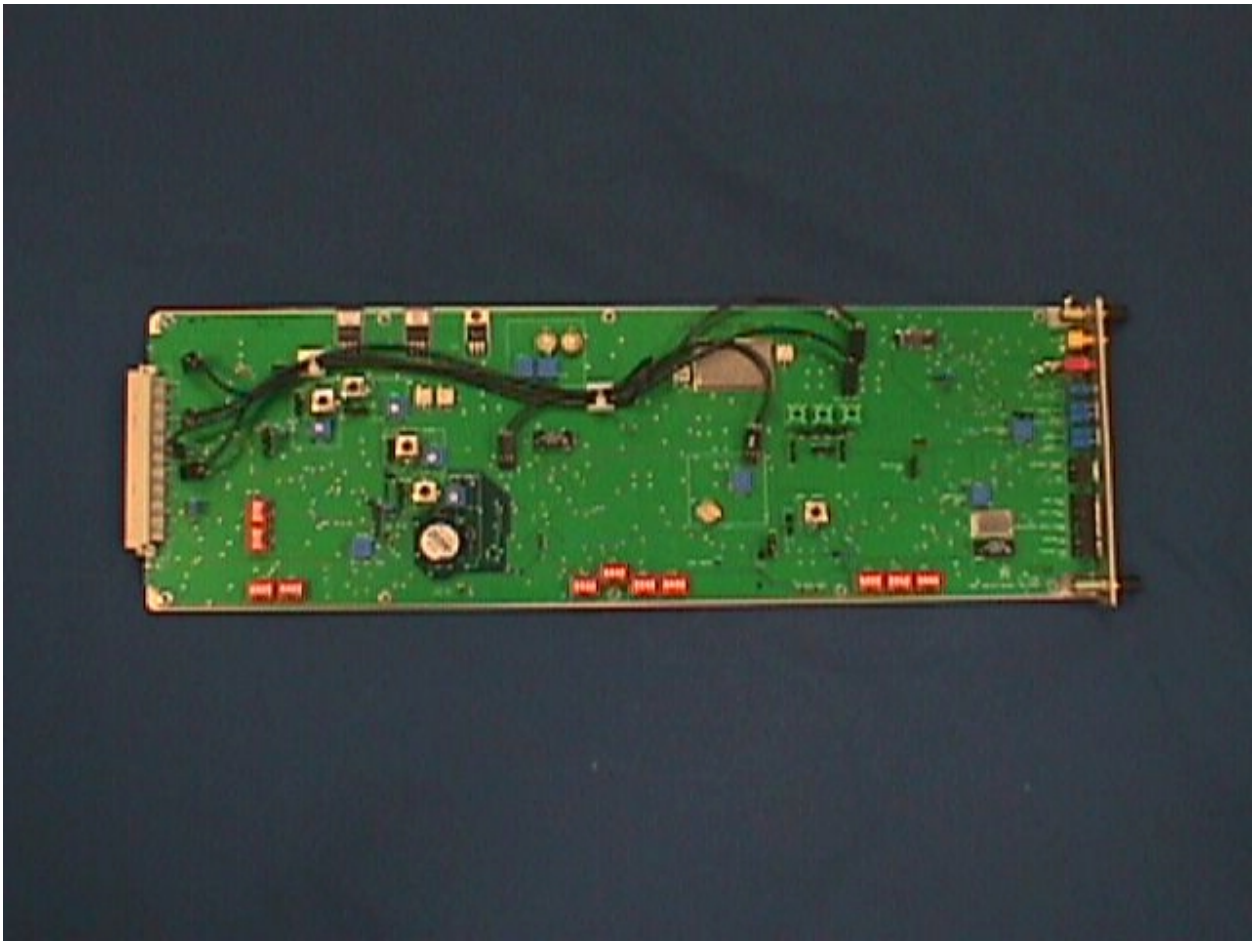
4.4.7 Top view, 5721, Transmitter Control and Monitoring Module



4.4.8 Top view, 5721, Power Amplifier Module



4.4.9 Top view, 5721 NTSC Modulator Module



5.0 CERTIFICATION OF TEST DATA

This equipment has been tested in accordance with the requirements contained in the appropriate Commission regulation. To the best of my knowledge, these tests were performed using measurement procedures consistent with industry or Commission standards and demonstrate that the equipment complies with the appropriate standards. Each unit manufactured, imported or marketed, as defined in the Commission's regulations, will conform to the sample(s) tested within the variations that can be expected due to quantity production and testing on a statistical basis. I further certify that the necessary measurements were made by ADC Telecommunications, 102 Road, McMurray, Pennsylvania 15317.

David Urban 2-15-2K

Dave Urban, Chief Engineer

Todd Anderson 2/15/2000

Todd Anderson, Engineer