Note: This Operational Description was taken from Section 2.4 of the report

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description

The superband multi-channel input signal is applied to the inuput of the translator (J4) and fed to the SuperBand Bandpass Filter w/ Amplifier module (1509-1107) which consist of two lumped element bandpass filters and two MAV-11 amplifiers. The ouput of this module is padded and applied to the IF input of the mixer (ZFM-15) where it is mixed with the LO signal.

The LO signal is generated on the VHF Generator Board (1500-1102). This board is comprised internally of a voltage controlled crystal oscillator circuit that is a modified Colpitts design . The crystal is mounted in an oven set at 60° C and operates at 1/24 of the local oscillator frequency. A PLL circuit on the VHF generator board divides a sample of the channel VCXO frequency and compares it to a divided down reference frequency generated by the 10 MHz Oscillator module (1519-1037) or to an external precise reference. The difference between the phase of the reference frequency and the divided down VCXO frequency sample causes the PLL IC to create an error output voltage or Automatic Frequency Control (AFC) voltage which is used to bias a variable capicitor in the VCXO circuit.

The output signal from the VHF Generator board is applied to the input of the X* Multiplier Board (1607-1109) which consist of three x2 broadband doublers ($2^3 = 8$). The output signal is applied to a X3 Multiplier board which consist of multiplier board that generates harmonics if the inut signal and a two section cavity filter tuned to select the third harmonic. The LO (2278 MHz) output signal of the X3 Multiplier is fed to the LO input of the mixer where it is mixed with the IF signal to produce the RF output signal.

The RF output of the mixer is fed to a Four Section Bandpass Filter (2140-1033) then to the Broadband Filter Module (2500-2700). The output of the filter is fed to the Amplifier Attenuator Module (1132-11509) input (J1). The input signal is AC coupled and amplified then applied to a "tee" configuration Pin Diode attenuator circuit. By controlling the gain of this attenuator, the output power can be regulated, maintaining a constant output regardless of minor changes in the input signal.

An external ALC bias voltage is generated by the Peak/Average Detector Board (1510-1105), which detects the peak envelope power of the combined output signal. This bias voltage is fed to the input (J1) of the ALC Control Board (1510-1103).

On this board the signal is amplified and adjusted in level by ALC potentiometer R9 and buffered to three output jacks (J2, J5, an J6). One output (J5) is fed to the input of the ALC Fault Sense Board (1132-1501). The ALC Fault Sense Board compares the ALC bias voltage to reference voltages, set by on board potentiometers, and will light front panel LED indicators should an out of range ALC condition occur.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description -continued

A second output from the ALC Control Board (J6) is fed to the front panel meter providing external monitoring. The third output of the board (J2) provides the ALC bias voltage for the PIN Diode attenuator in the Amplifier/Attenuator Module (1132-1509). The ALC circuit may be bypasses by moving W1 on J8 to the manual position. When the ALC is disabled, the loss through the PIN Diode attenuator is adjusted by the Manual Gain potentiometer R12, which then directly controls the output in a manual fashion.

The output of the Amplifier/Attenuator Module is connected to the Three stage Amplifier Module (1510-1106) driver amplifier, which consist of three cascaded GaAs FET amplifiers (FLLFSX52WF driving a FLL171ME driving a NES2527-20B-3) with an overall gain of approximately 40 dB. The output of the Three Stage Amplifier Module is fed to the input of the 50 Watt Amplifier Module (1506-1107).

The signal is input to the 50 Watt Amplifier Module at J1 and amplified by GaAs FET Q101 (FLM2527L-20XXA). Then the signal is split four ways by three by a Wilkinson in phase couplers and amplified by four parallel GaAs FET amplifiers, Q201 and Q301, Q401 and Q501 (all FLM2527L-20XXA's). The signal is then combined by a three additional Wilkinson in phase couplers and fed through a circulator then to the RF output of the module at jack J2.

A 20 dB microstrip directional coupler provides a forward power sample of the final output signal. A reflective power sample is obtained from the circulator. Both samples a sent to the Peak/Average Detector Board which detects both samples and produces a forward and reflected metering voltage which drives the booster's front panel meter.

The DC bias drain to source currents of each FET within the Three Stage Amplifier Module and the 25 Watt Amplifier Module are set by adjusting the negative gate to source voltages which are adjusted by potentiometers located next to the corresponding FET.

The Six Section Bias Protection Board (1500-1104) supplies the two amplifier modules with both +10 VDC (operating voltage) and -5 VDC (bias voltage).

The Transmitter Control Board (1510-1103) provides the capability to control and monitor the operating status of the translator. The board is designed to protect the booster in the event of the following faults: overtemperature, loss or reduction in output power and loss of the -5 VDC GaAs FET bias voltage. The Transmitter Control Board also provides the capability to remotely control and monitor the translator status through remote operate/standby commands and remote forward power metering.

2.0 TECHNICAL DESCRIPTION

2.4 Circuit Description -continued

The unit may be configured to be powered by either a 115 VAC/60 Hz or 230 VAC/50 Hz source. The AC source enters the tray at jack J1 and is distributed to a terminal block (TB2). Varistors VR1, VR2, VR3 and VR4 provide transient and overvoltage protection to the booster. The rear panel circuit breaker (CB1) applies AC voltage to the input of the toriod transformer.

The Toroid transformer provides two 15 VAC secondary windings. The first winding is sent to a full wave bridge rectifier which supplies a positive 18 VDC to several positive voltage regulators located on the ±12 VDC Power Supply Board (1500-1145). The second winding is supplied to a full wave bridge rectifier circuit located on the ±12 VDC whose output is sent to a negative voltage regulator. One +12 VDC switching supply (SPL250-1012), rated at 21 amperes, is used to supply the GaAs FET amplifier modules with power.