2.0 TECHNICAL DESCRIPTION

2.5 Alignment Procedure

In the following procedure, the complete transmitter is adjusted for optimum performance, beginning with the start up procedure of the CM720M modulator, followed by the upconverter/amplifier, starting at the IF input and adjusting each circuit for its specified performance while observing the appropriate output parameters of the board or subassembly being adjusted.

Because of the broadband nature of most of the amplifier stages, this is a straightforward procedure, easily accomplished if base-band, IF, and RF test equipment is available. In this procedure, the input signals are first connected and each circuit is adjusted in sequence by connecting the test equipment to the specified point.

Modulator Tray

Follow the step listed below to bring the CM720M modulator online.

1. Turn on the tray by connecting the AC power cable the unit and observing the front panel LEDs. The front panel lights flash through a consistent sequence when the unit is first powered on. when power-up is complete, the four seven-segment LEDs will illuminate, and the Fault LEDs will not illuminate.

2. Verify that the power-up message is displayed on the front panel LCD. If necessary, adjust the LCD contrast by pressing the increase/decrease buttons on the front panel.

3. Set the time/date.

4. Set the transmit power to -40 dBm to -50 dBm.

5. Confirm that transmit power is enabled.

6. Use the front panel to verify that the AQM mode is at the desired setting.

7. Use the front panel to verify that the scrambler, Reed-Solomon encoder, interleaver, and differential encoder are all enabled.

At this point the CM720M modulator has been powered up and the output spectrum may be observed.

Using a spectrum analyzer verify the proper shape and center frequency (44 MHz) of the spectrum at the IF output port (J5). Verify that the power level corresponds to that set in step 4 above.

2.0 TECHNICAL DESCRIPTION

2.4 Alignment Procedure - continued

Upconverter/Amplifier Tray

Connect a suitable load to the output of the Upconverter/Amplifier tray. Turn the circuit breaker (CB1) located on the back of the tray to the on position. Place the Upconverter/Amplifier in standby by pressing the standby switch on the front panel. The amber front panel indicator will light indicating that the Upconverter/amplifier is in standby.

Connect the output of the MMDS Receiver tray (J4) to the IF input of the Upconverter/Amplifier tray (J2) through a 30 dB pad.

Make the connections and switch settings on each of the boards indicated below as follows.

IF Delay Equilizer Board (A3)	Jumper from J1 to J2 (out of circuit)
Response Corrector Board (A5)	S1 and S2 to out
ALC/AGC Board (A6)	S1 and S2 to Manual
Linearity Corrector Board (A33)	S1 to disable
Phase Corrector Board (A34)	J9 and J10 to disable
Response corrector Board (A32)	S1 and S2 to out

Place the Upconverter/Amplifier into operate by pressing the operate switch on the front panel. The green front panel indicator will illuminate indicating that the Upconverter/Amplifier is in the operate mode.

IF Amplifier Board (A1) 1521-1101

The IF Amplifier Board consist of a transformer coupled input for impedance matching to 50 Ω or 75 Ω signals and a two stage amplifier providing about +24 dB of gain. Place W1 and W2 on pins 1 and 2 of J10 and J11 (50Ω). Place jumpers W7 and W8 on pins 1 and 2 of J 12 and J13 (attenuator out). The output of this board is approximately 6 dBm.

2.0 TECHNICAL DESCRIPTION

2.4 Alignment Procedure - continued

Upconverter/Amplifier Tray - continued

ALC/AGC Board (A6) 1022-1102

Disconnect J2. With SW1 and SW2 in the Manual position, adjust Manual ALC gain potentiometer R17 for about - 8 dBm at J2. Measure and record voltage at TP3. Switch S1 to the ALC position. Reconnect J2 and adjust ALC Gain potentiometer for the recorded voltage at TP3.

Using an appropriate directional coupler, connect a power meter to the RF output of the tray (J10). Adjust Manual AGC potentiometer R101 for the rated output power (4 watts average) of the unit.

Dual Peak Detector Board (A22) 1522-1147

With the front panel selector switch in the Forward Power position, adjust Metering Adjust potentiometer R35 for 100% on the front panel meter.

ALC/AGC Board (A6) 1022-1102

Adjust Inner Loop potentiometer R63 for 0.8 volts at TP7. Place switch SW2 into the AGC position. Adjust AGC potentiometer R96 for 100% on the front panel meter.

Linearity Corrector Board (A33) 1034-1201

The Linearity Corrector Board corrects for non-linearities in the amplifier stages. This board has been factory aligned and should not be adjusted without the proper equipment.

Phase Corrector Board (A34) 1227-1250

The Phase Corrector Board corrects for phase non-linearities of the amplifier stages later in the system. This board has been factory aligned and should not be adjusted without the proper equipment.

2.0 TECHNICAL DESCRIPTION

2.4 Alignment Procedure - continued

Upconverter/Amplifier Tray - continued

Response Corrector Board (A32) 1034-1205

Switch S1 and S2 into the in position.

Connect a sweep signal to the input of the Upconverter/Amplifier tray (J2). Monitor the output of the Upconverter/Amplifier with a spectrum analyzer. Adjust C6, C7, and C8 for the frequency of the correction notch being applied to response of the transmitter. R13, R15, and R17 are used to adjust the depth and width of the correction notch. Adjust C6 and R13, C7 with R15, and C8 with R17 as needed to flatten the response.

IF Delay Equalizer Board (A3) 1165-1018

The IF Delay Equalizer Board contains two sections of delay equalization that compensates for the group delay created by external band pass filters (waveguide) and should not be adjusted without the proper test set-up and equipment.

The IF enters the board at J1 and is applied to first section of the IF Delay Equalizer Board. The delay equalizer is adjusted by removing W1 on J5 and tuning L1 for a notch at center frequency. Replace W1 and adjust C8 for the best response. The output of the first section at J2 connects to the input of the second section at J3. The second section of the group delay equalizer circuit is adjusted by removing W2 on J6 and tuning L2 for a notch at center frequency. Replace W2 and adjust C10 for the best response.

VHF Generator Control Board (A14) 1519-1112

1. Disconnect the PLL reference frequency by removing the plug at J5 and/or J6.
2. Connect a digital volt meter between TP4 (+) and ground (-). Adjust the manual bias potentiometer (R87) for a reading of -3 VDC at TP4.
3. Connect a frequency counter to J11 to measure the VHF frequency (if frequency adjustments are necessary, follow the above procedure for the UHF Generator board).
4. Set PLL programming per required channel frequency (See programming chart on following page).
5. Connect an oscilloscope between pin 28 of U2 or TP9 (+) and ground (-).
6. Reconnect the plugs at J5 and/or J6 and minimize the spike amplitude that will be observed on the oscilloscope using the phase detector balance potentiometer R70.

2.0 TECHNICAL DESCRIPTION

2.5 Alignment Procedure - continued

MMDS PROGRAMMING CHART FOR VHF GENERATOR CONTROL BOARD (1519-1112)

CHANNEL NUMBER	VISUAL CARRIER (MHz)	L.0. = (F_V+45.75 MHz)	OSCILLATOR FREQUENCY = (L.O./24 MHz)	(1 = HIGH) (0 = LOW) (S1)	(S2)	(S3)	(S4)
A1	2501.25	2547.00	106.125	1101	1000	1100	1111
A2	2513.25	2559.00	106.625	1111	1000	1100	1101
A3	2525.25	2571.00	107.125	1100	0100	1100	1110
A4	2537.25	2583.00	107.625	1110	0100	1100	1100
B1	2507.25	2553.00	106.375	1011	1000	1100	1011
B2	2519.25	2565.00	106.875	1000	0100	1100	1001
B3	2531.25	2577.00	107.375	1010	0100	1100	1010
B4	2543.25	2589.00	107.875	1001	0100	1100	1000
C1	2549.25	2595.00	108.125	0101	0100	1100	1111
C2	2561.25	2607.00	108.625	0111	0100	1100	1101
C3	2573.25	2619.00	109.125	0100	1100	1100	1110
C4	2585.25	2631.00	109.625	0110	1100	1100	1100
D1	2555.25	2601.00	108.375	0011	0100	1100	1011
D2	2567.25	2613.00	108.875	0000	1100	1100	1001
D3	2579.25	2625.00	109.375	0010	1100	1100	1010
D4	2591.25	2637.00	109.875	0001	1100	1100	1000
E1	2597.25	2643.00	110.125	1001	1100	1100	1111
E2	2609.25	2655.00	110.625	1011	1100	1100	1101
E3	2621.25	2667.00	111.125	1000	0010	1100	1110
E4	2633.25	2679.00	111.625	1010	0010	1100	1100
F1	2603.25	2649.00	110.375	1101	1100	1100	1011
F2	2615.25	2661.00	110.875	1111	1100	1100	1001
F3	2627.25	2673.00	111.375	1100	0010	1100	1010
F4	2639.25	2685.00	111.875	1110	0010	1100	1000
G1	2645.25	2691.00	112.125	0001	0010	1100	1111
G2	2657.25	2703.00	112.625	0011	0010	1100	1101
G3	2669.25	2715.00	113.125	0000	1010	1100	1110
G4	2681.25	2727.00	113.625	0010	1010	1100	1100
H1	2651.25	2697.00	112.375	0101	0010	1100	1011
H2	2663.25	2709.00	112.875	0111	0010	1100	1001
H3	2675.25	2721.00	113.375	0100	1010	1100	1010

NOTE: ON SWITCHES S1, S2, S3 AND S4. THE HIGH (1) AND LOW (0) SETTINGS ARE READ AS MARKED ON THE CIRCUIT BOARD.

2.5 Alignment Procedure - continued

MDS PROGRAMMING CHART FOR VHF GENERATOR CONTROL BOARD (1519-1112)

CHANNEL NUMBER	VISUAL CARRIER (MHz)	L.0. = (F_V+44.75 MHz)	OSCILLATOR FREQUENCY = (L.O./24 MHz)	(1 = HIGH) (0 = LOW) (S1)	(S2)	(S3)	(S4)
MDS1	2151.25	2196.00	87.875	1100	1001	0100	1000
MDS2	2157.25	2203.00	88.125	0010	1001	0100	1111

2.0 TECHNICAL DESCRIPTION

2.5 Alignment Procedure - continued

UHF Generator Board (A15-A1) 1512-1101

1. Connect the main output from the channel oscillator section of the UHF Generator Board (J1) to a spectrum analyzer, tuned to the crystal frequency and peak the tuning capacitors C6 and C11 for maximum output. Tune L3 and L2 for maximum output. The output level should be +5 dBm ±2 dB.

While monitoring with a DVM, maximize each of the following test point voltages by tuning the broadband multipliers in sequence.

2. Monitor TP1: Tune C32 for maximum (Typical 0.6 VDC).
   Monitor TP2: Tune C34 and C38 for maximum (Typical 1.2 VDC).
   Monitor TP3: Tune C40 and C44 for maximum (Typical 2.0 VDC).
   Monitor TP4: Tune C46 for maximum.
   Monitor TP4: Re-peak C38, C40, C44 and C46 (Typical 3.5 VDC).

3. Connect a spectrum analyzer, tuned to 8 times the crystal frequency, to the UHF Generator output (J3). Monitor the output while peaking the tuning capacitors for maximum output.

4. The output level at J2 should be +15 dBm ±2 dB.

x3 Multiplier (A16) 1003-1004

1. While monitoring the x3 output (24 times the crystal frequency) with a spectrum analyzer, peak the four tuning capacitor for maximum output. Typical output is about +3 dBm ±2 dB.

The output of the x3 Multiplier is fed to the input of the Upconverter Board.

Upconverter Board (A4) 1519-1125

This board does not contain any RF tuning adjustments. The Upconverter Module produces an RF output at J2 by mixing two input signals (L.O. and I.F.), which are applied to J1 and J4 respectively.

The L.O. signal (+3 dBm) enters the module at J1 and is split into (2) separate and equal signals by a Wilkinson splitter. One output from the splitter is amplified to provide a buffered output sample (0 dBm) at J3. The second output from the splitter is also amplified and applied to the input of a mixer.

The IF signal enters the module at J4 and is applied to the input of a mixer. The output of the mixer produces a difference signal (L.O - IF) which is then amplified and sent to the to the RF output jack J2 (+4 dBm). The RF output from the board is sent a four-section cavity filter.

2.0 TECHNICAL DESCRIPTION

2.5 Alignment Procedure - continued

Upconverter Board (A4) 1519-1125 - continued

Biasing for the amplifier stages is accomplished by the setting of potentiometers.

The board receives DC power (-5 VDC and +12 VDC) from an external source. +5VDC is produced on the board by applying +12 VDC to the input of + 5VDC regulator.

Four Section w/Trap Cavity Filter (A15) 2000-1240

This filter has been factory swept for a 6 MHz bandwidth and should not be tuned without proper equipment. The filter has a typical loss of approximately 3 dB. The output of the filter is sent to a three stage amplifier module.

Three Stage Amplifier Module (A10-A1) 1516-1108

This amplifier does not contain any RF tuning adjustments. The module contains three cascaded broadband GaAsFET amplifier stages providing a nominal gain of 36 dB. The operating current for each device (Q101, Q201, Q301) is controlled by a pot mounted on a bias board within the module and can be set by measuring the voltage drop across the across the .05 ohm resister on the Six Section Bias Protection Board (Q301) and the voltage drops across the .22 ohm resistors (R14, R15) on the Drain Daughter Board (1516-1114) (Q101 and Q201).

1. With no RF signal applied and with the transmitter off, unsolder the drain leads located near the ferrite beads of Q201 and Q301 on the drain Daughter Board (1516-1114). Connect a digital voltmeter across R14 on the drain Daughter Board. Apply AC power to the transmitter and place the transmitter into the Operate mode.

2. Adjust the bias control (R103) for a reading of .04V across R14 on the drain Daughter Board (1516-1114). This voltage represents a bias current of .18 amps on Q101.

3. Place the transmitter into the standby mode and then turn the transmitter off. Unsolder the drain lead of Q101 and resolder the drain lead of Q201. Apply AC power to the transmitter and place the transmitter into the Operate mode. Adjust the bias control (R203) for a reading of .16V across R15 on the drain Daughter Board. This voltage represents a bias current of .720 amps on Q201.

4. Place the transmitter into the standby mode and then turn the transmitter off. Resolder the drain leads of Q101 and Q301. Apply AC power to the transmitter and place the transmitter into the Operate mode. Adjust the bias control potentiometer R303 for a reading of .24V across R1 on the Six section Bias Protection Board. This represents a bias current of 4.8 amps on Q301.

The output of this amplifier is fed to the 50-Watt Amplifier Module (A10-A3).

2.0 TECHNICAL DESCRIPTION

2.5 Alignment Procedure - continued

50 Watt Amplifier Module (A10-A3) 1512-1107

This Amplifier module does not contain any RF tuning adjustments. The module contains two cascaded broadband GaAs FET amplifier stages (FLL200-3 driving four parallel FLL200-3 's) providing a nominal gain of 18 dB. The operating current for each device (Q101, Q201, Q301, Q401 and Q501) is controlled by a pot mounted on a bias board within the module, next to each corresponding FET, and can be set by measuring the voltage drop across the .05 Ω resistors (R2, R3, R4, R5, and R6) on the bias protection board. See chart below.

GaAs FET Transistor	Potentiometer Adjustment	Bias Protection Board Resistor	Voltage Across Bias Protection Resistor Calculated	Drain Current
Q101	R902	R2	.24	4.8
Q201	R802	R3	.24	4.8
Q301	R902	R4	.24	4.8
Q401	R802	R5	.24	4.8
Q501	R902	R6	.24	4.8

The output of this amplifier is sent through a circulator (A50), then to the RF output jack (J10) at the rear of the tray.

The voltages needed to operate the amplifier modules are provided by the +12V/21 amp switching supplies (A9 and A10) and the ±12VDC Power Supply Board (A26) which produces the -5VDC bias voltage.

The -5VDC supply is non-adjustable with a regulated output. To prevent damage to the GaAs FET amplifiers, the +12VDC Supplies will not turn on until the -5VDC bias supply is operating.

The +12VDC/21 amp switching, regulated power supplies do not require any adjustment.

Six Section Bias Protection Board (A20) 1519-1124

This board does not contain any RF tuning adjustments. Indicators DS1, DS2, DS3, DS4, DS5, and DS6 will illuminate if the amplifier circuits are operating correctly with normal biasing and operating voltages.

2.5 Alignment Procedure - continued

SWITCH POSITION AND STATUS FOR NORMAL OPERATION

ALC/AGC Board	S1 set to "ALC" position. S2 set to "AGC" position. DS2 not lit (signal presence). DS5 not lit (RF mute). DS3 not lit (ALC fault).
Response Corrector Board	S1 set to "In" position. S2 set to "In" position.
DC Power Supply Board	DS1 - DS7 lit
Linearity Corrector Board	S1 to "enable" position
Front Panel	DS3 (PLL Locked) lit DS4 (Output Fault) not lit DS5 (Thermal Interlock) lit DS6 (PLL Reference Present) lit
Six Section Bias Protection Board	DS1 - DS6 (Bias OK) lit
Meter Selection Switch	Selects metering between % of forward power and % of reflected power.

2.0 TECHNICAL DESCRIPTION

2.6 Block Diagrams

System Block Diagram:

The following is a system block diagram for the ITS digital transmitter (ITS-5523). Detailed Block Diagrams and Schematics are included in exhibit II.