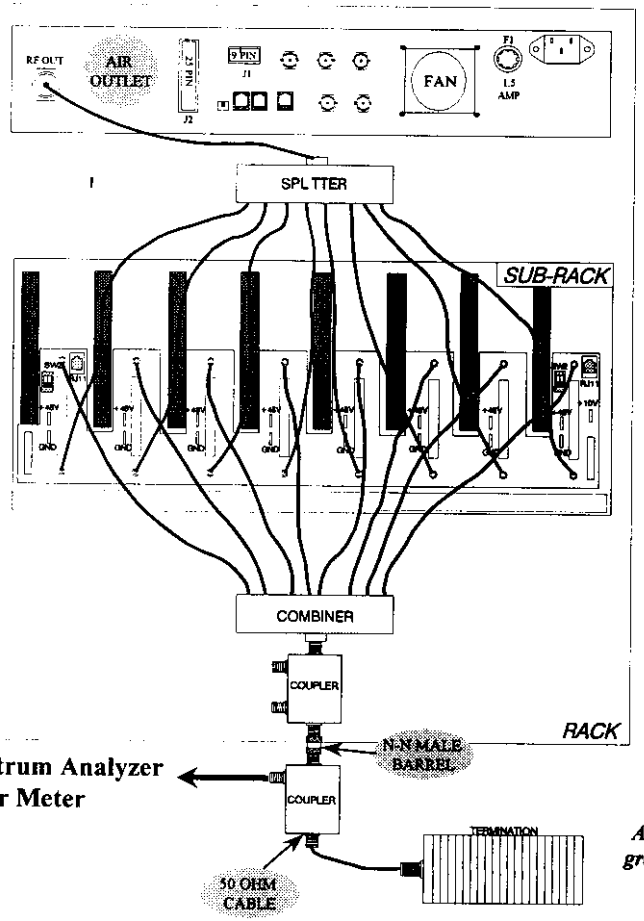
POWER CALIBRATION TEST SETUP

One to 16 Power Amplifier Segments are used in each transmitter, depending upon the power output



A termination which is equal to or greater than the output power of the transmitter should be used.

Created by: Kimberly Simeone 9/15/98	*Checked by:* 10/08/98	*Released by:* 10/12/98

Document #: DOC22-0018

REV: A

SECTION 4

Now that your system is up and running, it is time for a brief description of each module/board found within the system.

This section will break your system down into individual segments. You will find theory of operations for individual sections of your system, along with specifications if available. It is recommended that you contact Comwave customer service when you need repairs.

Additionally, schematics may be included in this section, if available.

RACK THEORY OF OPERATION

The rack is an integral part of the transmitter assembly. It supplies three-phase or phase-to-phase AC power to the transmitter, DC power to the sub-rack, and the cooling for the power amplifier segments. The rack is available in different sizes to accommodate the various physical configurations of the high power series of transmitters/boosters and to allow for future upgrades to higher output power levels.

Three-phase or phase-to-phase AC power enters the AC power distribution box, which is located on the top of the rack. It is connected to the AC power harness, which distributes both three-phase and phase to phase power to the entire rack.

Each transmitter requires an AC to DC front-end converter to supply the DC power to the sub-rack. This power supply is connected to the power amplifier segments via the DC power harness. The DC power harness connects the AC to DC front-end converter and the sub-rack. Fans attached to the rear door of the rack supply cooling for the power amplifier segments. Each fan pulls cool air from the front of the rack to the rear. The transmitters will be automatically placed into standby when the rear door of the rack is opened. This will prevent thermal shutdown of the power amplifier segments. ***Note: The number of fans is dependent upon transmitter configuration.***

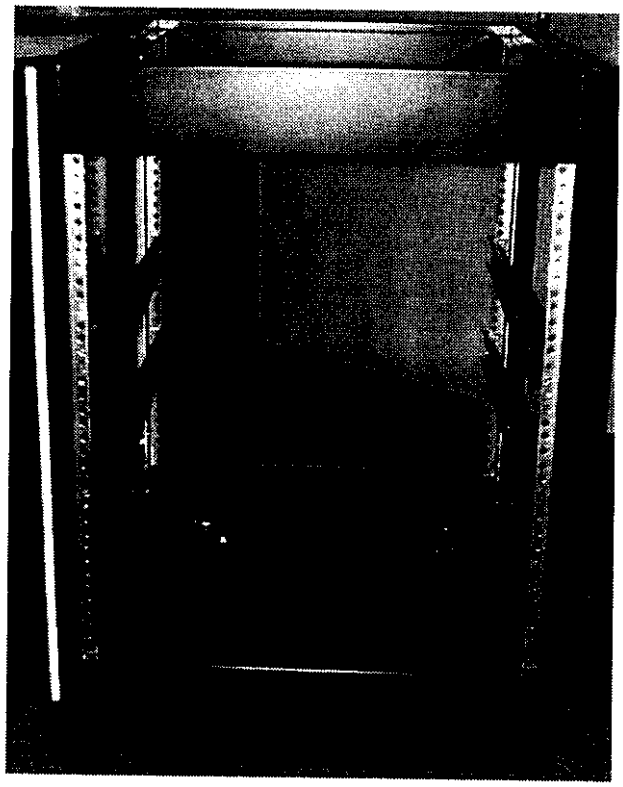
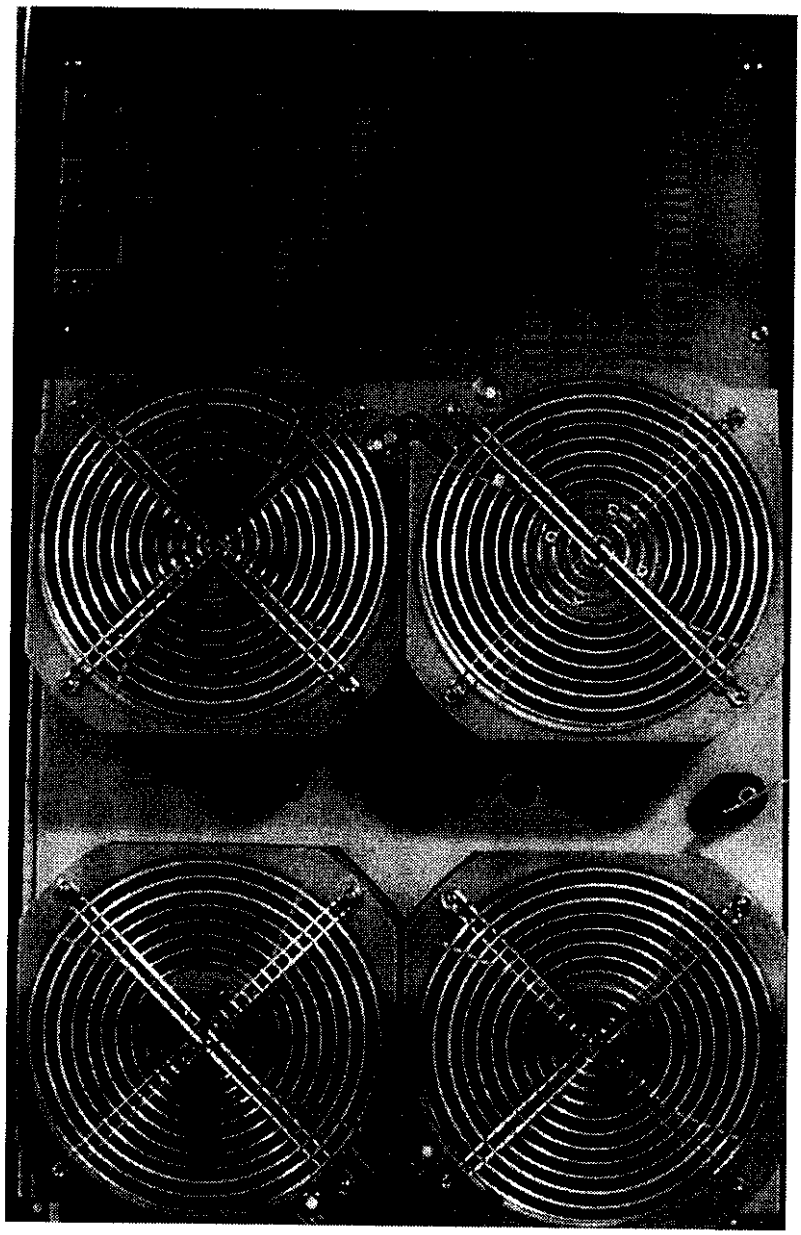


FIGURE 14-0005-1

SBM/HPB SERIES REAR VIEW



Created by: Kimberly Simeone 10/3/98	*Checked by:* 10/6/98	*Released by:* 10/19/98

SUB-RACK THEORY OF OPERATION

The sub-rack, figure 14-0006-1, is the unit that houses the power amplifier segments and provides an interface between the segments and the entire system. It is capable of housing up to 16 individual segments. The sub-rack consists of one or more *motherboards, (35-080) guide rails, protective Lexan overlay, and miscellaneous sheet metal parts. Each segment slides into the sub-rack on nylon slides and connects to the motherboard(s) via floating connectors. The key-lock switch, located on the segment's front panel, must be in the OFF position in order to plug the segment into the sub-rack. This is to ensure that there is no arcing between connections before the segment is fully engaged. Once the segment is slid into place, thumbscrews on the segment's front panel are fastened to the sub-rack to secure it and provide a reliable ground connection. The key-lock switch may now be turned to the ON position to apply power to the segment.

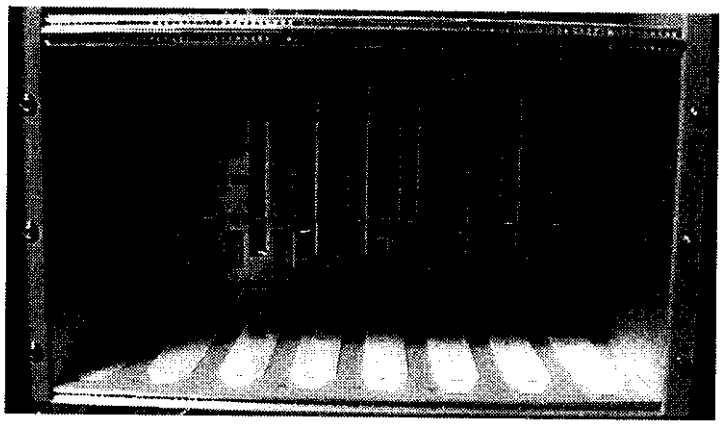


FIGURE 14-0006-1

Note that one motherboard is needed for up to eight segments, and two motherboards are needed when more than eight segments are used.

The interface for RF input and output is provided by floating OSP connectors which are mounted on the back panel of the sub-rack and the back side of the power amplifier segment.

MOTHERBOARD TO SYSTEM INTERFACE:

Power, ground, and data interface between the motherboard(s) and the system are discussed below. ***Note that numerical references to the diagram of the sub-rack rear panel are provided to make the test easier to follow.***

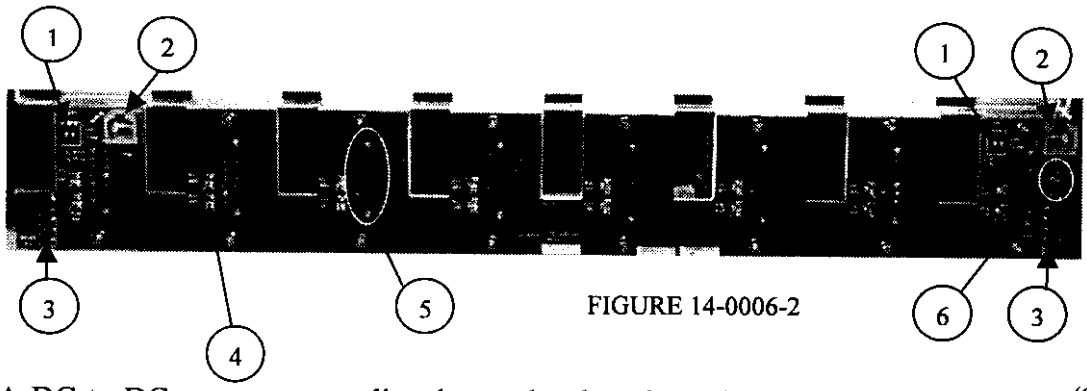


FIGURE 14-0006-2

A DC to DC converter supplies the mother board(s) with one 10 V_{DC} connection(6). A separate 48 V_{DC} and ground connection(4) for each power amplifier segment is supplied to the motherboard(s) from the main system power supply. A ten-position single-row header(3) affords data input from the driver and a six position RJ-11 connector(2) provides communication of control and diagnostics data to the motherboard(s). A two position DIP switch(1) located on the motherboard(s) can be set to OPEN for communication, or CLOSED for termination.

MODULE TO MOTHERBOARD INTERFACE:

Power, ground, and data interface between the segment and the motherboard(s) is provided through a float-mounted, blind mating, receptacle on the segment and a blind-mating header(5) on the motherboard(s).

VHF TO MICROWAVE DRAWER THEORY OF OPERATION (VHF/UHF BLOCK UPCONVERTER) OR (DRIVER)

The multicarrier driver receives a block of VHF/UHF signals typically at –15dBm/ carrier, which is upconverted to an S-band frequency. To prevent transmission of noise the driver will shutdown in the absence of input signal. The driver stage is capable of producing an output power of 24dBm per carrier when loaded with 31 channels. Refer to the block diagram 66-321-01 for RF signal path.

The input signal being received is sent to a variable attenuator. The attenuator regulates the signal level prior to predistortion. A high level mixer is applied to transition the signal block to microwave. The magnitude of the signal is then increased by the intermediate amplifier stages. The signal is filtered to prevent out-of-band products from being amplified and transmitted.

An RF precorrector reduces the intermodulation products, which occur at the output of the power amplifiers. Overall power regulation is provided by a second feedback loop. An external coupler provides an RF metering sample to an envelope detector for forward and reflected power measurement. The detected voltage represents the output power. The RF precorrector module uses this voltage to regulate the drive level needed by the power amplifier array

FRONT PANEL FEATURES, REFER TO DOCUMENT # DOC23-0038 FOR NUMBER REFERENCES.

1. ***METER:*** Provides a visual indication of transmitter status and performance of +11 V switching power supply, forward power, reflected power, or AGC. The meter is calibrated to display relative measurements. The seven position rotary selector switch controls meter function.

2. ***FUNCTION SWITCH:*** A seven position, user selectable, rotary switch that controls front panel meter monitoring. The following parameters are selectable for monitoring by the function switch.

RESET:	Transmitter in a state of interrupt.
STANDBY:	Disables transmitting. Power remains applied to all circuits, except the microwave amplifier modules. Meter will read approximately 0 %.
METER OFF:	Transmitter is enabled. Metering disabled. Meter will read approximately 0%.
+ 11 V PS:	Provides status of main switching power supply.

Meter reads 100 % indicating proper switching power supply voltage.

AGC: Provides status of incoming IF signal. Meter reads 100% indicating nominal signal level.

REFL PWR: Relative reflected power measurement. Readings of less than 10 % are typical.

FWD PWR: Relative forward output power measurement. 100 % meter reading confirms correct output power.

3. ***LED's:*** Status monitoring LED's which provide visual indication of operating parameters and internal diagnostics. The following status monitoring LED's illuminate GREEN during normal operation. Absence of an LED indicates missing signal or parameter that results in a controlled automatic transmitter shut down.

IN SIGNAL: Illuminates GREEN with presence of input signal.

INTERLOCK: Illuminates GREEN when interlock logic conditions are satisfied. Interlock Logic conditions are satisfied when all Microwave Amplifier Modules have -12 V gate bias.

TRANSMIT: Illuminates GREEN when in transmit mode.

The following status monitoring RED LED's remain OFF during normal operation. When a failure is detected, the appropriate LED will illuminate RED. Controlled automatic transmitter shut down is a function of failure severity. Presence of a RED status LED with normal meter readings and/or normal transmitter operation indicates an out of tolerance condition with that circuit.

LOCAL OSCILLATOR: Absence of the local oscillator reference signal. Transmitter shut down occurs.

TEMPERATURE: Internal chassis temperature exceeds +140 degrees Fahrenheit (+ 60 degrees Celsius). Transmitter shut down occurs. Allow transmitter to cool. Transmitter reset can be attempted by rotating the front panel function switch to RESET.

LO AGC: The local oscillator loses level. Transmitter shut down occurs.

IPA 1:	Indicates a failure or an out of tolerance condition with the intermediate power module. Transmitter usually operates at reduced output power.
IPA 2:	Indicates a failure or an out of tolerance condition with the intermediate power module. Transmitter usually operates at reduced output power.
RF POWER:	Indicates a failure or an out of tolerance condition with the driver module. Transmitter usually operates at reduced output power.
POWER SUPPLY:	A failure in the +11 volt power supply or an out of tolerance condition. Transmitter shut down occurs.
FINAL:	Indicates a failure or an out of tolerance condition with the intermediate power module. Transmitter usually operates at reduced output power.

4. ***OCS TP:*** A front panel mounted test point used to monitor the local oscillator.

REAR PANEL FEATURES, REFER TO DOCUMENT # DOC23-0039 FOR NUMBER REFERENCES.

1. ***J2:*** Female 25 pin D-Sub connector for diagnostics monitoring.

2. ***J1:*** Female 9 pin D-Sub connector for system monitoring and control.

3. ***RF OUT:*** RF output connector (Female N type).

4. ***ACCESS HOLES:*** For phone jack connectors and a termination switch from the RS 485 Board used for communication to Comview Network.

INPUT CONNECTORS (FEMALE BNC'S):

5. ***REFLECTED SAMPLE:*** Input from external coupler for measurement of VSWR in the system.

6. ***FORWARD SAMPLE:*** Input from external coupler for maintaining proper output power of the system.

7. ***VHF IN***: Input signal from an external system (combining network or IF to VHF upconverter)

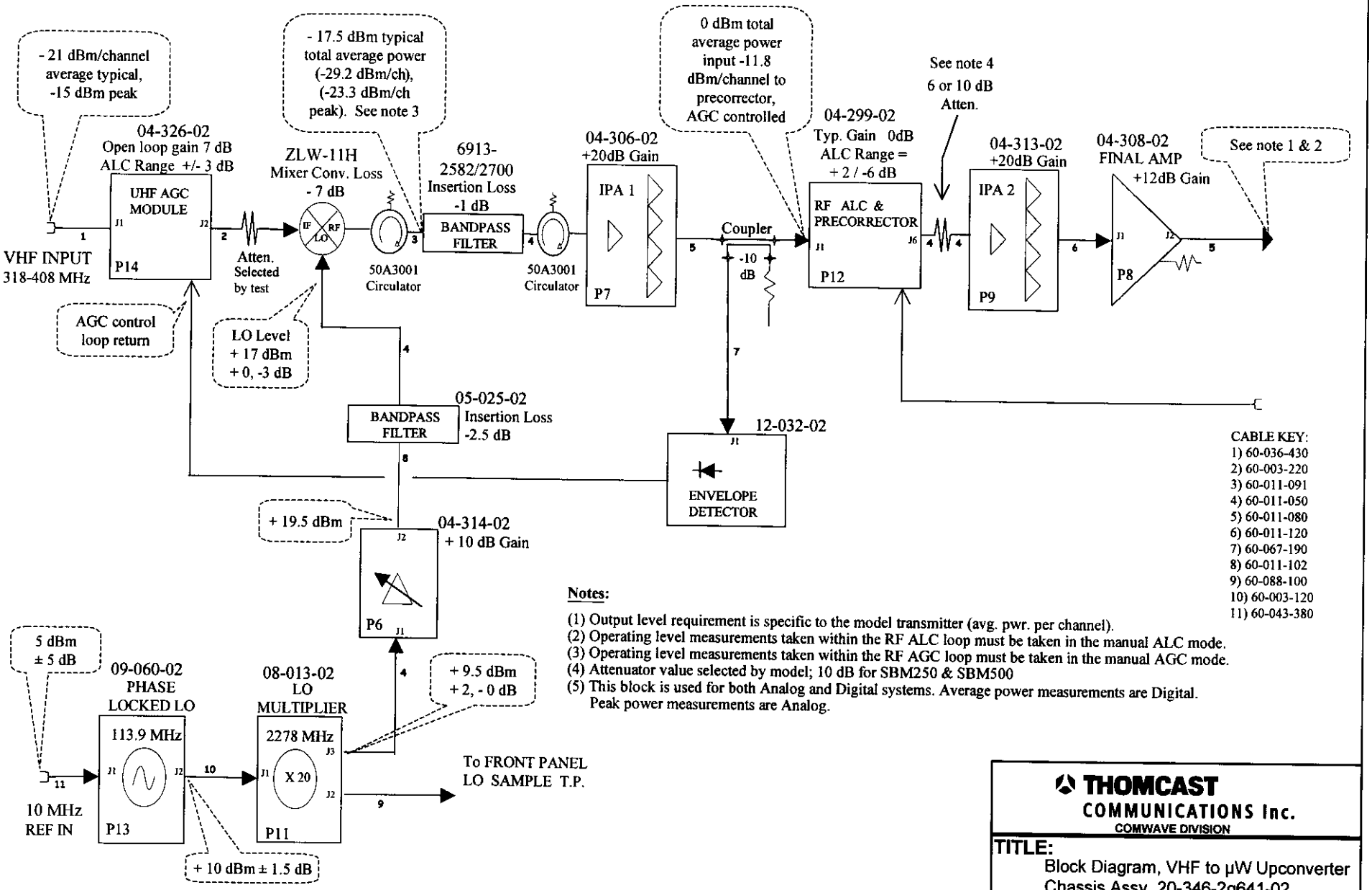
8. ***FREQ REF:*** Input signal from an external frequency reference source.

9. ***POWER SWITCH:*** Turn power on and off.

10. ***FUSE:*** Main line fuse location (7amperes).

11. ***AC INPUT:*** AC Line input power cord connector.

12. ***FAN:*** A rear mounted DC Fan provides switching power supply cooling.



CABLE KEY:
1) 60-036-430
2) 60-003-220
3) 60-011-091
4) 60-011-050
5) 60-011-080
6) 60-011-120
7) 60-067-190
8) 60-011-102
9) 60-088-100
10) 60-003-120
11) 60-043-380

Notes:

(1) Output level requirement is specific to the model transmitter (avg. pwr. per channel).
(2) Operating level measurements taken within the RF ALC loop must be taken in the manual ALC mode.
(3) Operating level measurements taken within the RF AGC loop must be taken in the manual AGC mode.
(4) Attenuator value selected by model; 10 dB for SBM250 & SBM500
(5) This block is used for both Analog and Digital systems. Average power measurements are Digital. Peak power measurements are Analog.

REV	Description	ECO# NAME/DATE

THOMCAST COMMUNICATIONS Inc.
COMWAVE DIVISION

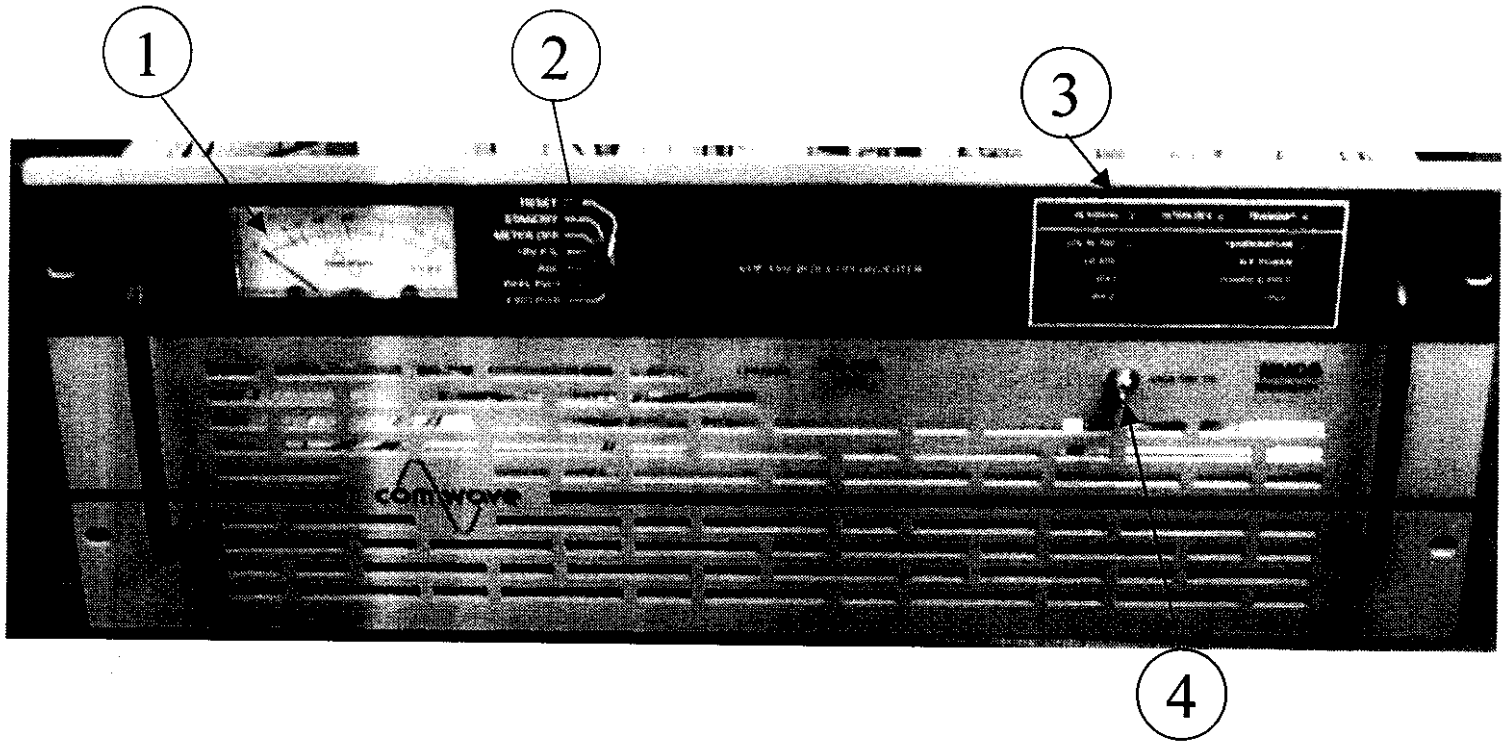
TITLE: Block Diagram, VHF to µW Upconverter Chassis Assy, 20-346-2g641-02

DRAWN: D.Wike / 1/9/98
CHECKED: J.Fisher / 3/2/99
RELEASED: D.Wike / 3/9/99

DWG. NUMBER: DOC15-0043

Scale: none | Sheet 1of 1 | REV: A

VHF/UHF BLOCK UPCONVERTER (DRIVER) FRONT PANEL

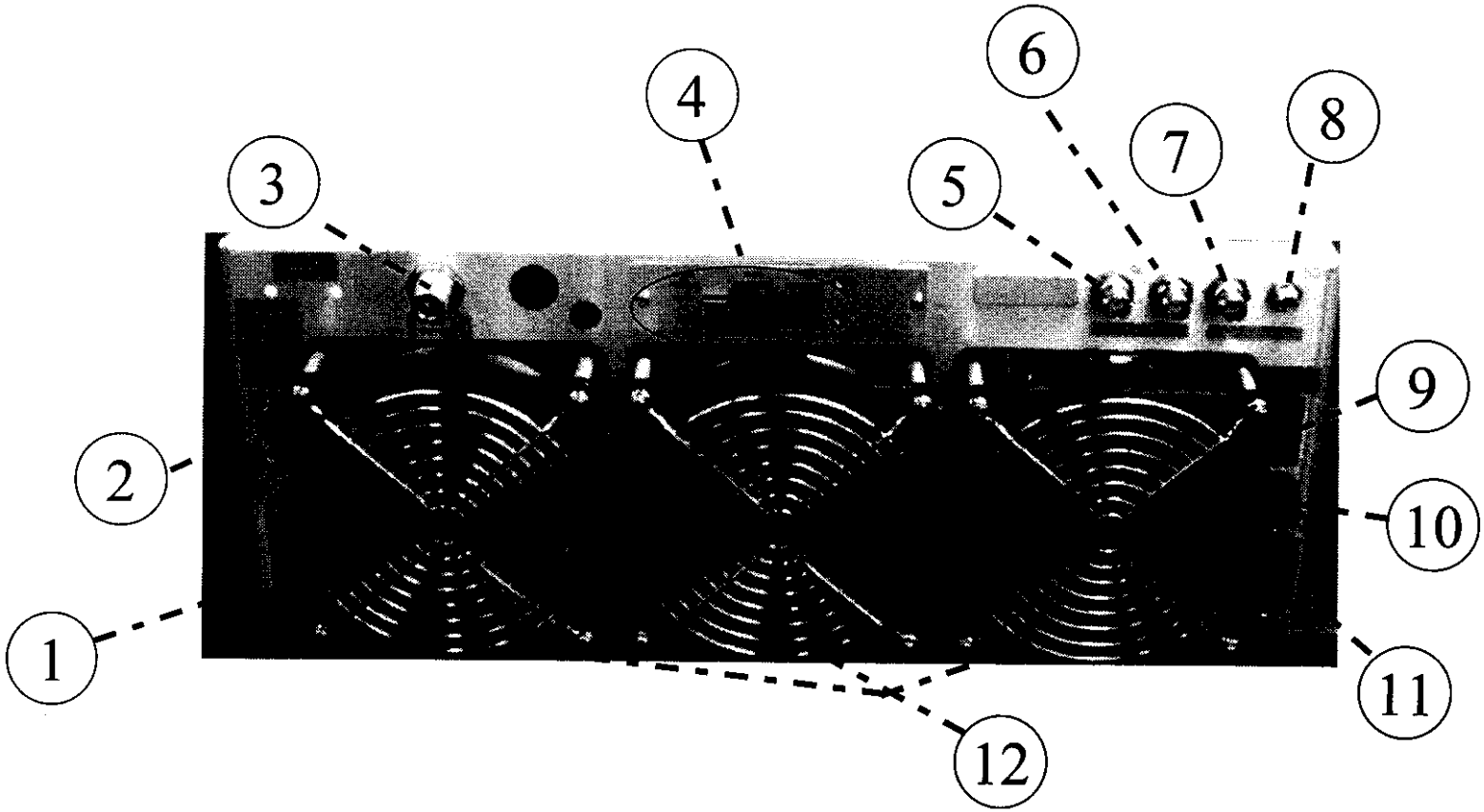


Created by: Kimberly Simeone 9/24/98	*Checked by:* 10/08/98	*Released by:* 10/19/98

Document #: DOC23-0038

REV: A

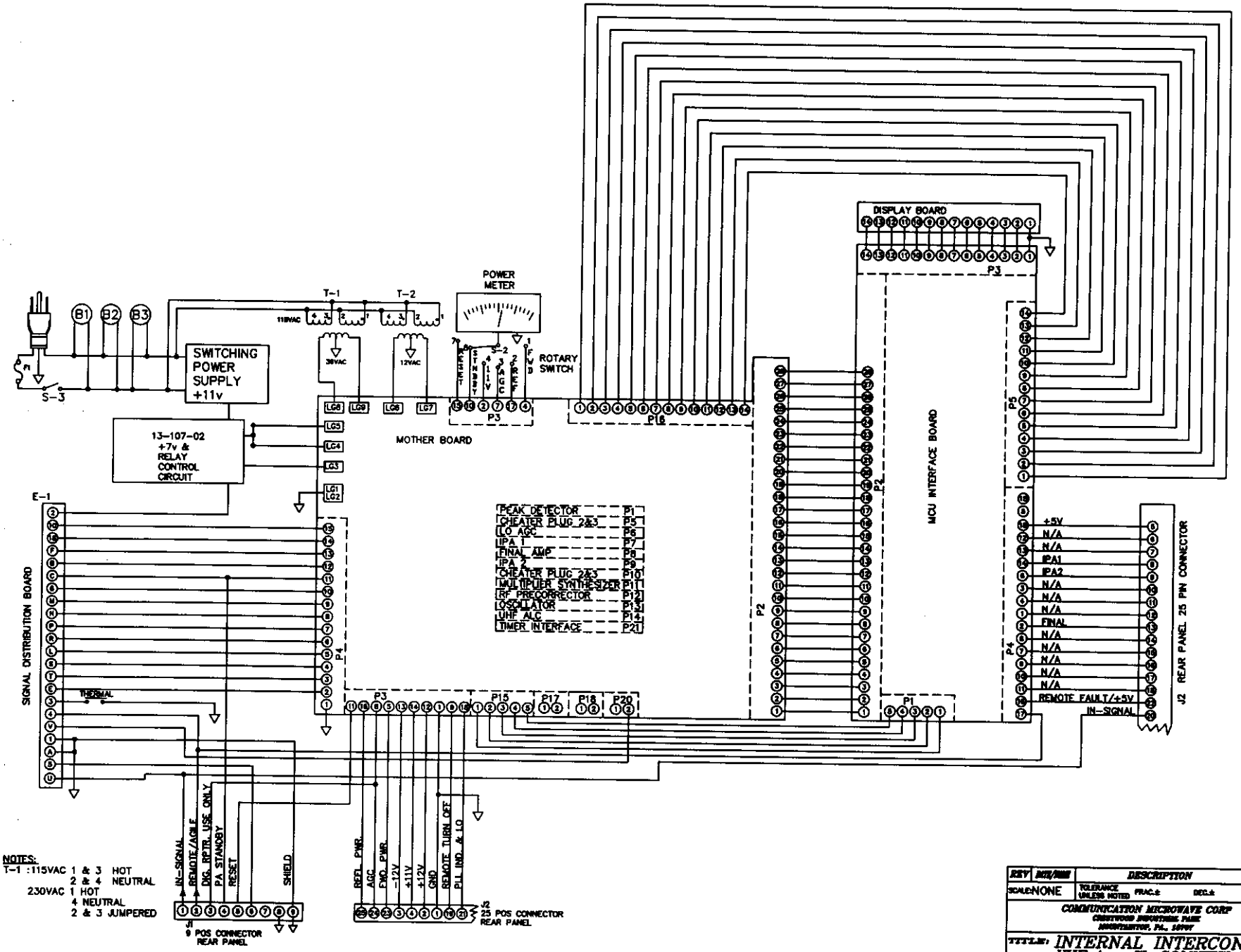
VHF/UHF BLOCK UPCONVERTER (DRIVER) REAR PANEL



Created by: Kimberly Simeone 9/24/98	*Checked by:* Daniel Ortiz 10/08/98	*Released by:* Paul G Greiss 10/19/98

Document #: DOC23-0039

REV: A



NOTES:
T-1 :115VAC 1 & 3 HOT
2 & 4 NEUTRAL
230VAC 1 HOT
4 NEUTRAL
2 & 3 JUMPERED

KEY	DATE/INIT	DESCRIPTION	ECO No.

SCALE:NONE TOLERANCE UNLESS NOTED FRAC.± DEC.± ANG.±

COMMUNICATION MICROWAVE CORP
CHESTNUT INDUSTRIAL PARK
MORRISTOWN, PA., 19707

TITLE: INTERNAL INTERCONNECT VHF to uW. COMVIEW READY

DRAWN	03/31/98	D. WIKE	DWG. NO. C-66-323-01
DESIGNED			SHEET 1 OF 1
PCB LAYOUT			
PCB ART WORK			
ENGINEER APPROVAL	08/29/98	D. WIKE	PCB NO. P1 REV. A

SBM-SERIES DRIVER SPECIFICATIONS

Reference Input: (Other CCIR systems available)

Parameter	*Specification*	*Notes/Test Conditions*
Frequency	10MHz	
Impedance	75 ohms	
Level	10 dBm ± 3 dB or +58 dBmV ± 3 dB	
Connector	F	

VHF/UHF Input: (Other CCIR systems available)

Parameter	*Specification*	*Notes/Test Conditions*
Frequency Range	222 to 408 MHz	Other frequency options available upon request
Impedance	75 ohms	
Level	-18 dBm ± 3 dB or +30 dBmV ± 3 dB	Power measured per channel.
Connector	BNC	

MMDS Output: (Other CCIR systems available)

Parameter	*Specification*			*Notes/Test Conditions*
Frequency Range	2.0 GHz to 2.7 GHz			Nominally 10% bandwidth over 2000-2700 MHz. Available bands: 2000-2200 MHz; 2200-2400; 2500-2700 MHz. Contact factory for other specialty bands.
Frequency Response	≤ ±1 dB			
Impedance	50 ohms			
C/N Carrier to Noise	≥ -52 dBc			
Level	SBM-250	SBM-500	SBM-1000	
15 channels 31 channels	2.5 dBm -1 dBm	5.5 dBm 2 dBm	8.5 dBm 5 dBm	
Connector	N female			
Local Oscillator Front Panel Sample	+ 9dBm ±2dB			

Created by: Kimberly Simeone 12/14/98 ECO #: 98-164	*Checked by: Donald Wike 12/14/98*	*Released by: Andre Castro 12/21/98*

Parameter	*Specification*	*Notes/Test Conditions*
Phase Noise @ 10KHz offset	≤110 dBc/Hz	
Conversion Accuracy	≤±500 Hz ≤±3 Hz (Optional LORAN C) ≤±1 Hz (Optional GPS)	Frequency Stability depends upon the modulator selected. Refer to the Modulator Manual for Frequency Stability Specifications.

General

Parameter	*Specification*
Power Requirement	117/230 V_{AC}, 50/60 Hz (<200 VA)
Functional Operating Temperature	0°C to 50°C
Normal Operating Temperature Range	13°C to 33°C
Relative Humidity	95% non-condensing
Dimensions	6.97"H x 19.00"W x 22.50"D 17.70 cm H x 48.30 cm W x 57.20 cm D
Shipping Weight[1]	56 LB. (25.4 kg)

Notes:

1. ***Shipping weight includes transmitter and shipping material.***

LOCAL OSCILLATOR MULTIPLIER

The Local Oscillator Multiplier module receives an input signal at J1 and provides a frequency multiplied output at J2 and J3. The output frequency is 20 times the input at +7 dBm ± 2 dB.

Multiplier action is based upon the operation of step-recovery diode D1. The diode is biased to conduct during a portion of the input cycle. The depletion layer of the junction is charged during this period. When the signal changes polarity, the diode is biased off and produces a sharp pulse rich in harmonics. The bandpass filter is tuned to select the 20th harmonic.

The signal is then amplified and split to form the two outputs of the module. The LO signal is detected within the module providing a DC signal proportional to the output power for monitoring by diagnostics.

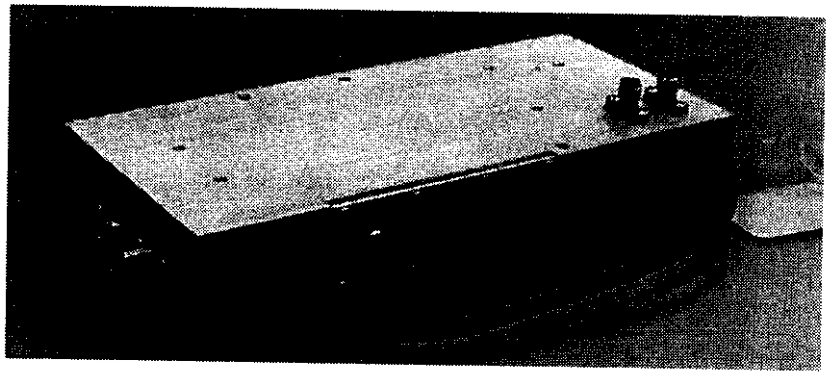


FIGURE 13-0060-1

LOCAL OSCILLATOR MULTIPLIER SPECIFICATIONS

Local Oscillator Multiplier Specifications	
Input Level	+10 ± 3 dB
Input Frequency Range	95 MHz – 137.5 MHz
Output Level	+9 ± 3 dB
Output Frequency Range	1.9 GHz + 2.75 GHz
Power Level Detectors (@ 10K Ω load)	.4 VDC @ + 6 dBm output level
Input/Output Impedance	50 Ω
VCC	12 VDC @ 450 mA

DOCUMENT #: DOC19-0030
REV: A

Created by: Kimberly Simeone 10/19/98	*Checked by: Donald Wike 10/23/98*	*Released by: Paulo Correa 10/23/98*

VCXO PLL

The Voltage Controlled Crystal Oscillator (VCXO) Phase Locked Loop and Local Oscillator Multiplier modules determine the microwave upconverter mixer input frequency. The initial frequency is determined by a VCXO crystal. Crystal frequency is dependent upon the desired transmitter output frequency. Crystal frequency stability is a function of the applied 10 MHZ input reference (J1). The VCXO output level at J3 is +7 dBm ± 2 dB. This signal is applied to the Local Oscillator Multiplier (J1) which multiplies it by a factor of 20.

The VCXO PLL board generates a DC control voltage proportional to the offset to return the oscillator to the selected frequency. The VCXO circuit uses dividers that are programmed by miniature board mounted switches to achieve the 12.5 KHz frequency reference. This signal is then applied to one input of a Phase Detector. The other input to the Phase Detector is derived through a sample of the VCXO frequency. A second dual prescaler divides the frequency again to achieve the desired 12.5 KHz. Should the VCXO deviate in frequency, this change is seen at the Phase Detector input and an error correction voltage is generated to pull the VCXO back to the desired frequency. The step size of the module is 12.5 KHz, which results in a step size of 250 KHz once multiplied to the microwave LO.

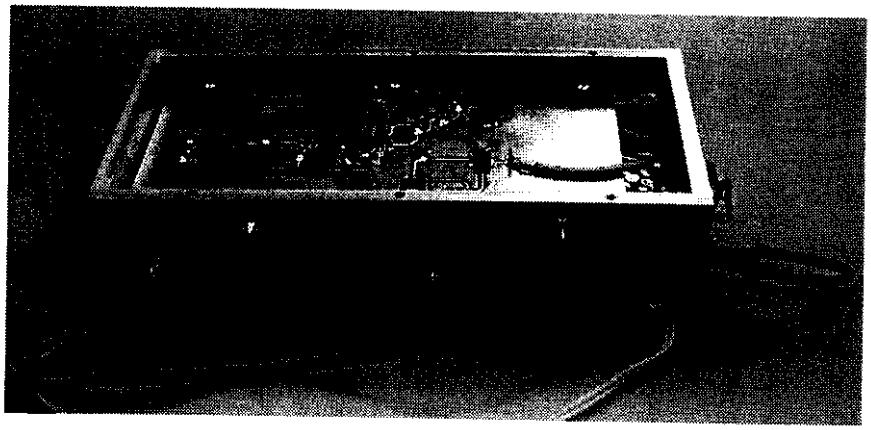


FIGURE 13-0059-1

VCXO PLL SPECIFICATIONS

VCXO PLL Specifications	
Frequency Reference Input	10 MHz
Frequency Reference Level	+5 dB ± 5 dB
Reference Input Impedance	75 Ω
Output Level	+10 dB ± 3 dB
Output Frequency Range	95 MHz – 137.5 MHz
Output Impedance	50 Ω
Ø Lock Alarm TP1	Logic high indicates Ø Lock
Voltage Control TP2	Nominal 5.5 VDC
VCC	+12 VDC @ 300 mA

DOCUMENT #: DOC19-0031
REV: A

Created by: Kimberly Simeone 10/1/98	*Checked by: Donald Wike 10/23/98*	*Released by: Paulo Correa 10/23/98*

BANDPASS FILTER

This filter consists of a four-section bandpass filter with variable input and output loading probes. It is used to remove undesired signals following theLO. Tuning elements are variable length lines inside each cavity. Coupling between each section consists of fixed apertures, which set the bandwidth. A fifth section is coupled into the last section of the filter. This section forms a notch filter, which is not used in this application.

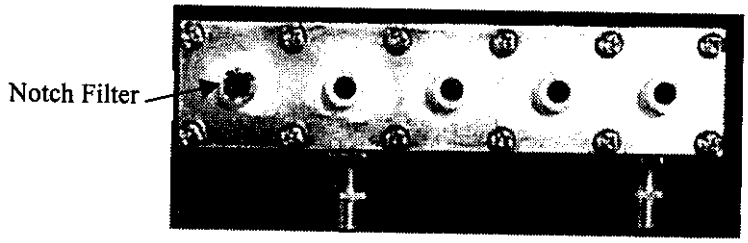


FIGURE 13-0051-1

BANDPASS FILTER SPECIFICATIONS

Specification	
Bandwidth (1 dB)	20 MHz
Insertion Loss	1 dB ± 0.5 dB
Tuning Range: MMDS/ITFS	2.05 – 2.4 GHz

DOCUMENT #: DOC19-0022
REV: A

AMPLIFIER WITH ALC

The ALC modules for the local oscillator are broadband output level controlled modules with a dynamic range of P1dB=+21dBm based on MMIC technology devices. These blocks have a gain range from 5 to 14dB and are fed by a +12V power supply at .4A maximum current. Access for the RF signal is made by means of J1 and J2 respectively input and output. Distinct controls are available for both manual and automatic modes, which can be set by means of an external switch.

AMPLIFIER WITH ALC SPECIFICATIONS (04-305, 04-314)

RF SPECIFICATIONS (04-308-02/04-314-02)

Parameter	*Typical*	*Limit*	*Notes/Test Conditions*
S_{11} (dB)	-15	-12maximum	2.0 GHz to 2.7 GHz
S_{21} (dB)	5 to 14	-	2.0 GHz to 2.7 GHz
Total Flatness (dB)	0.5	1 maximum	2.0 GHz to 2.7 GHz

DC SPECIFICATIONS (04-305-02/04-314-02)

Parameter	*Specifications*	*Notes/Test Conditions*
Total current (mA)	400 maximum	
Power Supply Voltage (V)	12	

Document #: DOC19-0028
REV: A

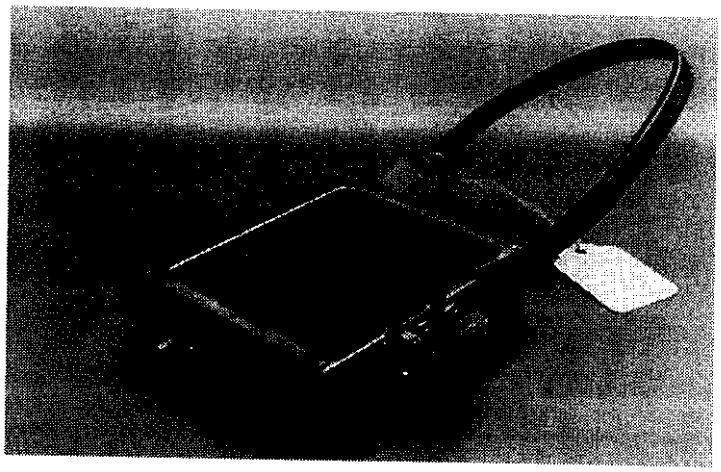


FIGURE 13-0057-1

Created by: Andre Castro 9/1/98	*Checked by:* 10/22/98	*Released by:* 10/22/98

VHF/UHF ALC MODULE

The VHF/UHF ALC module performs two functions in the system, automatic level control and detection of the incoming signal. It accepts a range of frequency from 60MHz to 422MHz. Once internal the VHF/UHF signal is split two ways, one path leads to a signal detector, the other is the main path which forms the ALC section of the module. The ALC can be set to capture and maintain a signal ±4dB of the nominal input. User adjustments for calibrations of AUTO level control as well as MANUAL control is accessible from the module exterior other meter calibrations are adjustable within the chassis. A selector switch dictates the mode of operation. The control loop for ALC extends beyond the module. A sample of RF signal level is sampled at the transmitter's mid section. This sample is converted to a DC voltage in a detector circuit (which should not be confused with the level detector on board) and feedback to the ALC section of this module is via pin 5 of the harness. Once calibrated the module will provide for approximately 8dB of gain from input to output.

FIGURE 13-0066-1

The on board detector is a feature which enables external diagnostic monitors to view the incoming signal level. This level is compared to a threshold set via an adjustment on the front side of the module. If the level is to low the module indicates this condition by changing it's output from a TTL logic level high to a logic level low. This DC indication exits the module through the harness on pin 6.

VHF/UHF ALC MODULE SPECIFICATIONS

VHF/UFH ALC Module Specifications	
Input Frequency Range	60 – 422 MHz
Input Attenuation Range	15dB
Nominal Gain	8 dB
ALC Capture Range	±4 dB
Input Level Detection	Signal presence is indicated by TTL logic high
Input/Output Impedance	75 Ω

DOCUMENT #: DOC19-0032
REV: A

Created by: Don Wike 10/9/98	*Checked by:* 10/23/98	*Released by:* 10/23/98

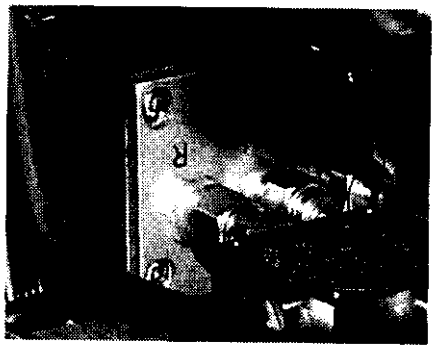
MIXER

This module consists of a balanced mixer being driven from the LO injection input via the SMA connector labeled "L" on the module top cover and an IF input via an SMA connector labeled "I". The heterodyned product exits the module through the port labeled "R".

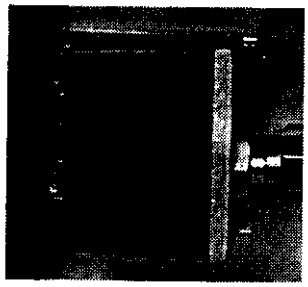
SPECIFICATIONS

FREQUENCY MHz		CONVERSION LOSS dB				LO-RF ISOLATION, dB						LO-IF ISOLATION, db					
LO/RF	IF	MID-BAND			TOTAL RANGE	L		M		U		L		M		U	
f_L - f_U																	
10-3000	10-1000	6.83	.09	10	12	27	20	25	18	23	16	27	20	25	18	23	16

FIGURE 13-0065-1



FRONT VIEW



SIDE VIEW

FIGURE 13-0065-2

Created by: Kimberly Simeone 10/9/98	*Checked by:* Donald Arthur 10/09/98	*Released by:* Paula Cruz 10/19/98

BANDPASS FILTER

This filter consists of a multi-section bandpass filter with fixed input and output loading probes. It is used to remove out-of-band mixing products following the mixer. Tuning elements are variable length lines inside each cavity. Coupling between each section consists of fixed apertures, which set the bandwidth.

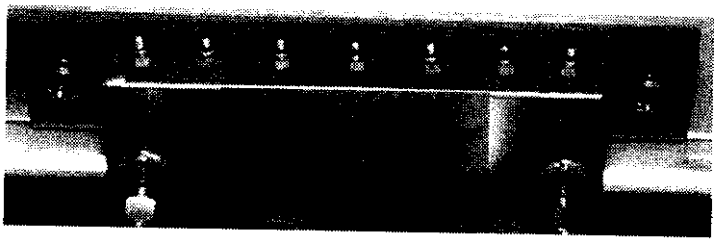


FIGURE 13-0050-1

BANDPASS FILTER SPECIFICATIONS

*Specification****	
Bandwidth (1 dB)	200 MHz/118 MHz
Insertion Loss	1 dB ± 0.5 dB
Tuning Range: MMDS/ITFS	2.5 – 2.7 GHz/2.582 – 2.7 GHz

DOCUMENT #: DOC19-0021
REV: A

****NOTE: Other frequencies are available.***

Created by: Kimberly Simeone 9/24/98	*Checked by:* Donald Ruhl 10/20/98	*Released by:* Paul Bruce 10/20/98

Document #: DOC13-0050
REV: A

INTERMEDIATE POWER AMPLIFIER

The intermediate power amplifier modules are amplifiers with a low noise figure (5dB) high dynamic range (P1dB=+28dBm) based on MMIC technology devices. With an internal configuration of one device driving four, these blocks have a typical gain of 20dB and are fed by a +7V power supply at .75A. Access for the RF signals is made by means of J1 and J2 respectively input and output.

INTERMEDIATE POWER AMPLIFIER SPECIFICATIONS
(04-306-02 & 04-313-02)

RF SPECIFICATIONS

Parameter	*Typical*	*Limit*	*Notes/Test Conditions*
S_{21} (dB)	20	19.5 minimum	2.00 GHz to 2.75 GHz
S_{11} (dB)	6dB	5dB minimum	2.00 GHz to 2.75 GHz
Total Flatness (dB)	0.5	0.75	2.00 GHz to 2.75 GHz

DC SPECIFICATIONS

Parameter	*Specifications*	*Notes/Test Conditions*
Power supply (V)	7 ± 0.5	
DC Current (A)	0.76 maximum	

DOCUMENT #: DOC19-0023
REV: A

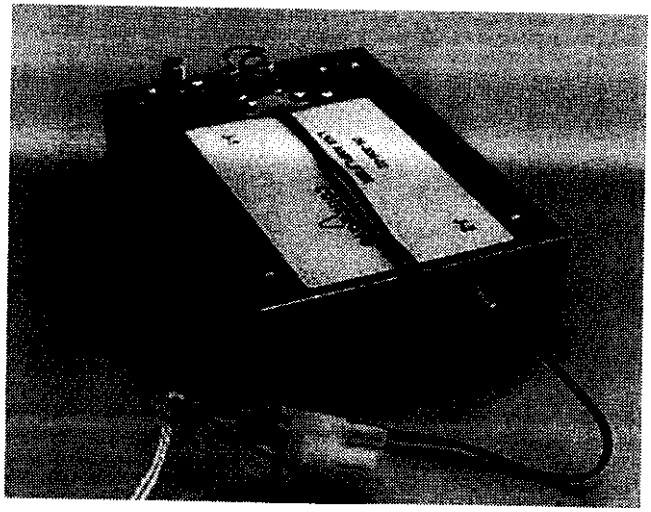


FIGURE 13-0052-1

Created by: Andre Castro 9/1/98	*Checked by:* 10/20/98	*Released by:* 10/20/98

Document #: DOC13-0052
REV: A

ENVELOPE DETECTOR

The envelope detector is a single input module that receives a forward power sample from a -10 dB coupler connected between IPA1 and RF precorrector. The forward sample is applied to SMA J1. The circuit detects the RF sample converting it into representative DC voltage. This voltage is sent to the motherboard for peak detection and/ or feedback control for the front end ALC system.

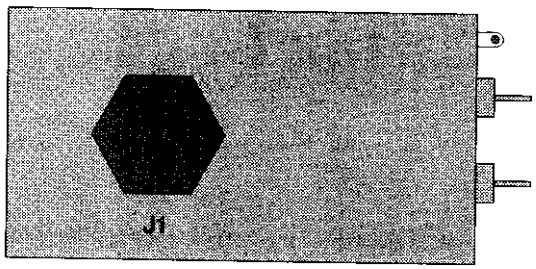


FIGURE 13-0023-1

BROADBAND PRECORRECTOR

The precorrector module contains correction circuitry and an automatic level control. Linearity correction circuitry precorrects mainly for third order products developed in the solid state power amplifier. The ALC maintains 100% output power over a ±2dB input variation. An RF frequency range based processor improves its overall performance over the IF type because it avoids the bandwidth limitations imposed by the band/channel filter.

Correction made is applied to J1, by means of subtraction of a pre-generated distortion from the one present at the output of the system. A RF input signal about 0dBm. This signal is amplified and split in two ways. One goes through a linear path while the other goes through the circuitry that generates the desired distortion. Both signals are combined and amplified to recover the losses of their processing. Finally, the resulting signal goes through the broadband attenuator that performs the ALC.

The module has two switches, one for turning on/off the pre-correction (1) and the second one to set the system into ALC or Manual mode (2). Five internal controls are accessible from exterior of the module. First is the control (3) for pre-distortion signal amplitude, second (4) is for module internal adjustment, third (5) is for superposing pre-distortion and output distortion signals, fourth (6) is to adjust output power in ALC mode and the fifth control (7) is to adjust output power in Manual mode. The 12V power-supply, the detected voltage, proportional to the output power, and a sample of the ALC voltage transit in/out the module through connector P1 (8).

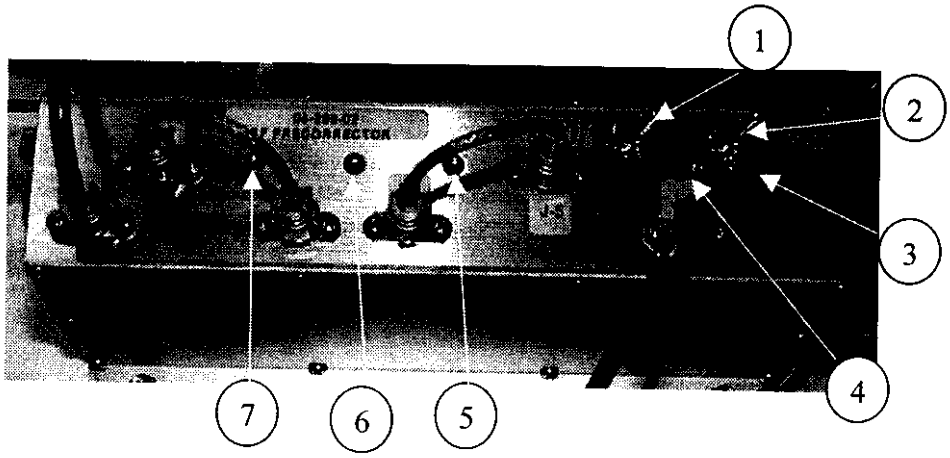


FIGURE 13-0062-1

FOR AGILE SYSTEMS ONLY:
This option is only available for agile transmitters and requires changes in the configuration of the jumpers (9) inside the module. The first four controls mentioned in the above paragraph can be set externally with the help of a personal computer, the pre-distortion calibration software and the 34-015 board. In that case, up to 31 different sets

of pre-correction can be set and stored into the 34-015 board. All voltages that control pre-correction externally reach the module through connector P2 (10). Refer to figures 13-0062-1 and figure 13-0062-2 for numerical references.

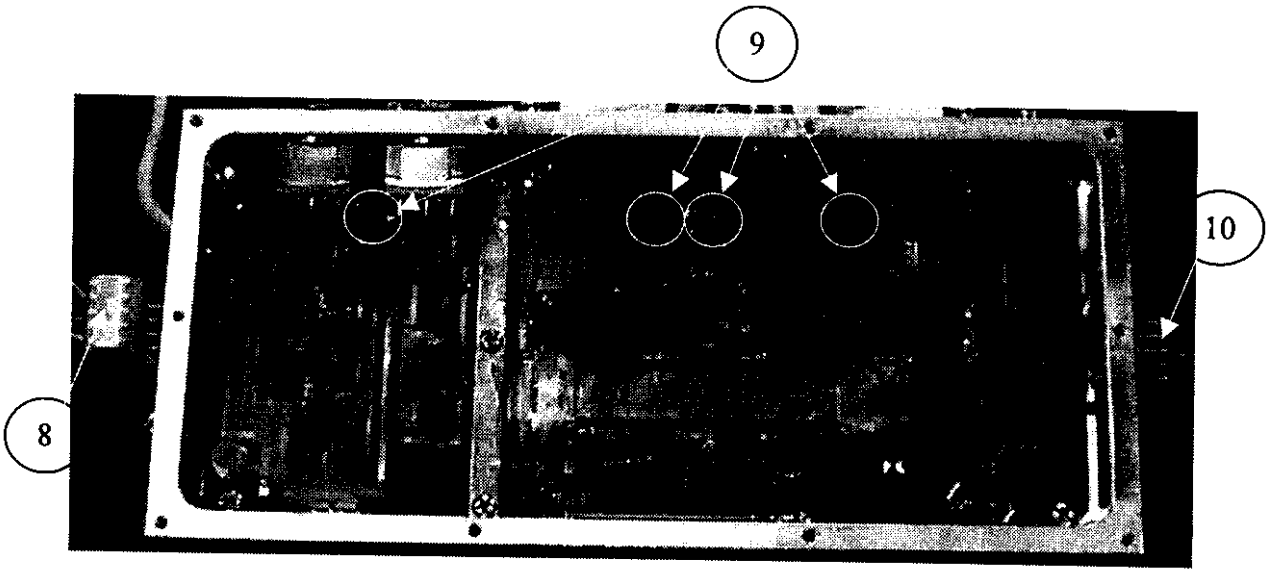


FIGURE 13-0062-2

RF SPECIFICATIONS
(04-299-02)

Parameter	*Typical*	*Notes/Test Conditions*
S_{21} (dB)	3	2.0GHz TO 2.8GHz
S_{11} (dB)	7dB	2.0GHz TO 2.8GHz
S_{21} Range (dB)	$-3<S_{21}<7$	2.0GHz TO 2.8GHz
Total Flatness (dB)	±1	2.0GHz TO 2.8GHz

DC SPECIFICATIONS
(04-299-02)

Parameter	*Specifications*	*Notes/Test Conditions*
Power Supply (V)	12 ± 0.5	-
DC Current (A)	.700	S21 = 2dB; Maximum pre-distortion

Document #: DOC19-0026
REV: A

INTERMEDIATE POWER AMPLIFIER

The intermediate power amplifier module is a broadband amplifier with high dynamic range (P1dB=+22dBm) based on GaAs technology devices. With an internal configuration of two devices in parallel, this block has a typical gain of 10dB and is fed by a +10.5V power supply at 1.44A. Access for the RF signals is made by means of J1 and J2 respectively input and output, while J3 is an output for RF sample 10dB below.

INTERMEDIATE POWER AMPLIFIER SPECIFICATIONS
(04-308-02)

RF SPECIFICATIONS

Parameter	*Typical*	*Limit*	*Notes/Test Conditions*
S_{11} (dB)	-17	-15 maximum	2.0 GHz to 2.7 GHz
S_{21} (dB)	10	9.5 minimum	2.0 GHz to 2.7 GHz
Total Flatness (dB)	0.3	0.5	2.0 GHz to 2.7 GHz

DC SPECIFICATIONS

Parameter	*Specifications*	*Notes/Test Conditions*
ID_1, ID_2 (mA)	1440	
VD_1, VD_2 (V)	10.5	

DOCUMENT #: DOC19-0024
REV: A

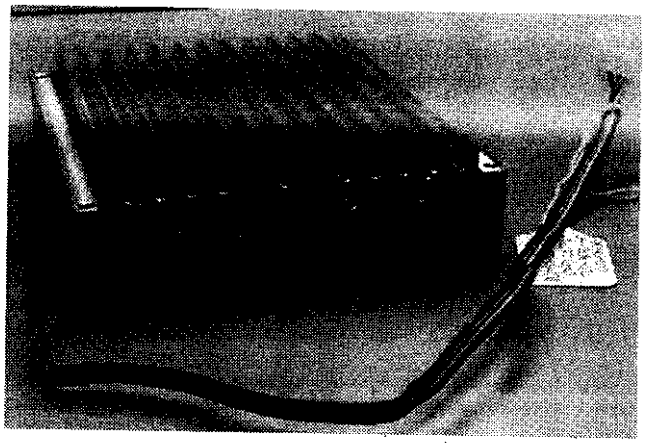


FIGURE 13-0053-1

Created by: Andre Castro 9/1/98	*Checked by:* 10/20/98	*Released by:* 10/20/98

MOTHERBOARD

The Mother Board performs a variety of functions allowing operation for both analog and digital applications. Located on the underside of the transmitter, it provides the majority of the interconnections among other circuit boards and modules. The board contains linear power supplies, current sampling resistors, metering adjustments, one +12 volt power supply fuse, and three +11 volt power supply fuses.

Jumper configurations: The motherboard is factory set with all jumpers positioned in accordance to the system architecture. Changing these jumpers is only necessary if upgrading to/from digital transmission. In the case of Common Amplification, configure as a digital transmitter. The following will help in choosing the proper settings.

Note: If a two position jumper is to be opened, attach the plastic jumper cap to one of the pins so you will not lose it.

- Jumper JK1: (3-pin jumper) Allows for operation with an Aural Final amplifier in analog applications providing the signal path for the power detector, and in the case of digital completes the logic path for the IF Detector module.

Setting	Description
1 & 2	Aural Final
2 & 3	IF Detector

- Jumper JK2: (3-pin jumper) This jumper provides +11 volt power to the aural driver module, or +12 volt power to the IF Equalizer for use in a digital transmitter.

Setting	Description
1 & 2	Aural Driver
2 & 3	Dig, IF. EQ.

- Jumper JK3: (2-pin jumper) Remains shorted in analog and digital applications. However, in a digital repeater system removing the jumper allows for the AGC voltage of the receiver to be monitored.

Settings	Description
shorted	Analog & Digital TX.
Open	Digital Repeater

- Jumper JK4: (3-pin jumper) This high current jumper provides +11 volt power to the Aural final in analog applications and +12 volt power to the IF Detector module in digital operation.

Settings	Description
1 & 2	Aur. Final Pwr.
2 & 3	IF Det. Pwr.

Interconnections: Power and logic signals are routed to/from various module or circuit card assemblies via the motherboard and main harness. Consult the interconnection diagram for guidance. The Synthesizer, IF Processor, and amplifier modules plug directly into this board for DC supply and monitoring.

Linear Power Supplies: -12, + 12, and +5 volt linear power supplies are located on this printed circuit board. These DC power supplies provide power to operational amplifiers, comparitors, gating circuits, and other modules.

- The negative 12 volt circuit consists of a center tapped full wave rectifier, filtering capacitors, and an adjustable regulator. The voltage can be calibrated adjusting VR5 on the board, while monitoring TP1. Short circuit protection is provided internal to the regulator.

Note: This adjustment should only be done in operation mode, due to FET gate pinch off during transmitter turn on. While in a standby or reset condition the negative supply will read approximately -15 vdc. When rotated from standby a small time delay will occur before returning to - 12 volts.

- The positive 12 volt circuit consists of a center tapped full wave rectifier, filtering capacitors, fixed 12 volt regulator and a current boost transistor. The current boost transistor, when conducting, provides a parallel path for added current to the 1.5 amp. regulator. A fuse (F4) is provided on the motherboard for short circuit protection. A voltage test point (TP2) is provided for monitoring.

- The positive 5 volt circuit consists of a full wave rectifier, filtering capacitor, and a fixed 5 volt regulator. Short circuit protection is provided internal to the regulator. A voltage test point (TP3) is provided for monitoring.

Sampling Resistors: The +11 volt switching power supply connects to screw terminals 3, 4, & 5 to distribute power to the driver, prefinal, and final A/B amplifier modules. Power is distributed through series current sample resistors. These resistors develop voltage drops proportional to the supplied drain current. Samples are routed to the diagnostics board for processing.

Envelope Detector: Integrated onto the motherboard, the envelope detector is responsible for stripping off the carrier signal. Serving as an average detector, it receives

samples of both forward and reflected RF power; then, it converts this energy to a proportional DC voltage composed of a DC level and an AC component.

+11 Volt Power Supply Fusing: The motherboard contains three fuses that protect the switching power supply. F1 (15 Amperes) provides power to the driver and prefinal. F2 (25 Amperes) provides power to final amplifier B and F3 (25 Amperes) to final amplifier A.

Metering Calibration: The front panel analog meter or LCD display is calibrated by trim potentiometers located on the motherboard. These adjustments calibrate the +11 V_{DC} switching power supply (VR1), Aural (VR2) when applicable, Reflected (VR3), and Forward (VR4). These potentiometers are accessible when the transmitter's cover is removed. Consult the Calibration section of the manual for detailed procedure.

MICROCONTROLLER INTERFACE BOARD

The optional Microcontroller interface board is a second generation diagnostic and control interface function. It, along with the GCB-11, provides full diagnostics and control, along with network communications capabilities required to support the ComView monitoring system.

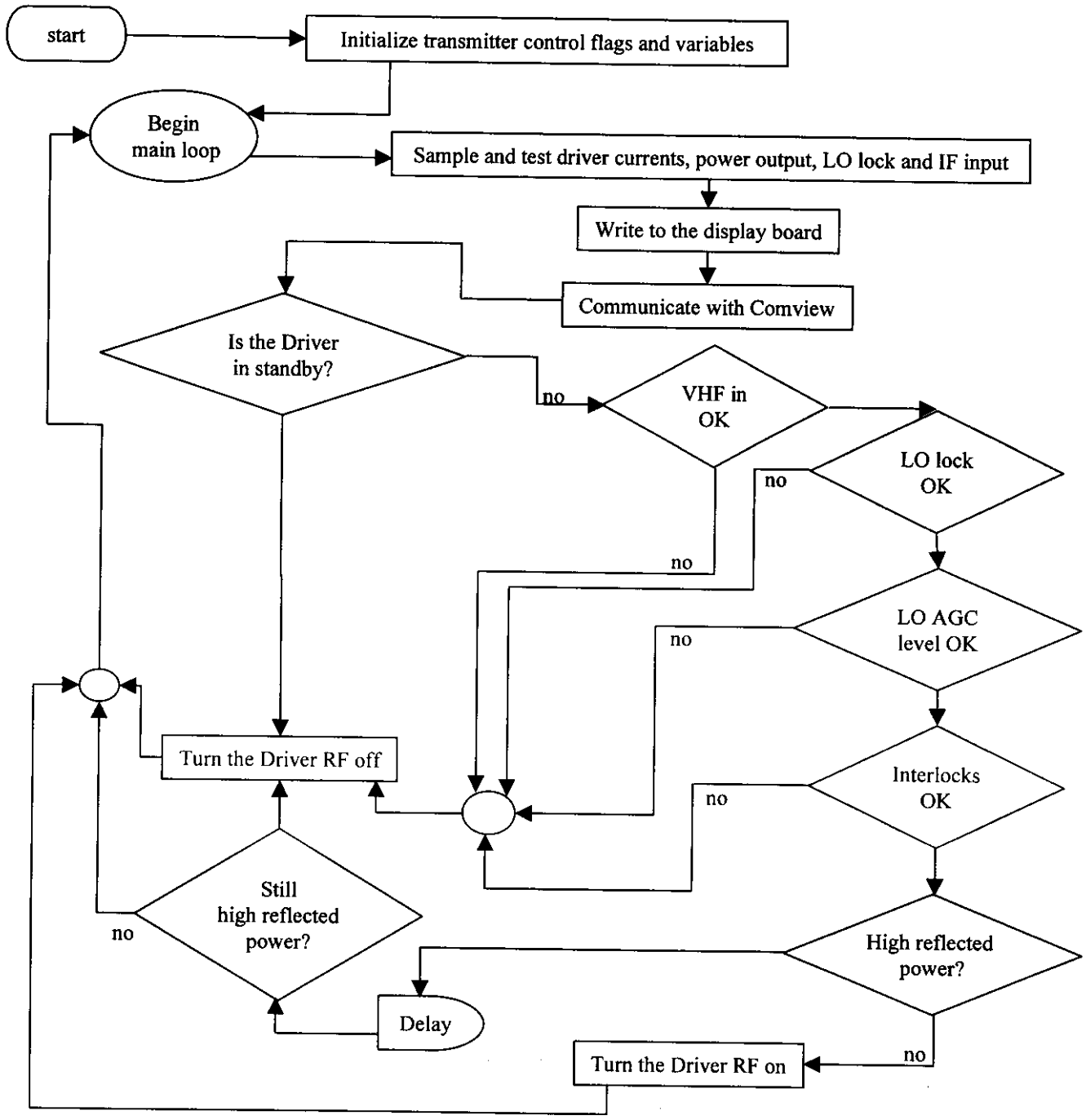
The Microcontroller Interface Board controls the front panel LED or LCD display, MUX addressing, and interlock, transmit functions through octal latches. The MCU receives various input signals, scales these inputs, and forwards them over a multiplex buss to the Microcontroller unit (MCU, GCB11) for processing. The scaling amplifiers receive current converted voltage samples from amplifier modules, amplifying them by appropriate factors for common working levels. Scaled outputs are sent to 16 channel analog multiplexers. The multiplexers receive addressing information from the Microcontroller through a hex level translator. The multiplexed output is further scaled (reduced by a voltage divider network and is sent to the Microcontroller for processing).

The following chart cross references the signal, scaling amp, and multiplex output.

INPUT SIGNAL	*SCALING AMP*	*MULTIPLEX OUTPUT*
Final A (Q2, 6, 7)	U1D	MUXBUS1 11
Final A (Q1, 3, 4, 5)	U2A	MUXBUS1 12
Final B (Q2, 6, 7)	U3A	MUXBUS1 14
Final B (Q1, 3, 4, 5)	U3C	MUXBUS1 13
Driver #1 (Q2, 3)	U2C	MUXBUS1 08
Driver #2 (Q4, 5)	U2D	MUXBUS1 07
Mixer (Q1)	U2B	MUXBUS1 09
PreFinal (Q2)	U3D	MUXBUS2 03
LO Locked	U1A	MUXBUS1 05
ALC IN	U1B	MUXBUS1 10
+12 V_{DC}	U1C	MUXBUS2 04
-12 V_{DC}	U3B	MUXBUS2 08
+11 V_{DC}	U4B	MUXBUS2 02
Thermal	U5D	MUXBUS2 01
IN SIGNAL	U5C	MUXBUS2 00
PS INTERLOCK	U17A	MUXBUS1 06
Gate 1	U17B	MUXBUS2 09
Gate 2	U17C	MUXBUS2 10
Gate 3	U17D	MUXBUS2 11
Gate 4	U18A	MUXBUS2 12
Gate 5	U18B	MUXBUS2 13
Forward Power	U18C	MUXBUS2 07
N/A	U18D	MUXBUS2 06
REFL Power	U19A	MUXBUS2 05

Created by: Kimberly Simeone 9/30/98	*Checked by:* 10/08/98	*Released by:* 10/19/98

FIRMWARE FLOWCHART
VHF/UHF TO uW UPCONVERTER



Created by: Kimberly Simeone 10/26/98	*Checked by:*	*Released by:* 10/26/1998 Carl P. Ungvarsky

Document #: DOC21-0003

REV: A

CHASSIS MONITORING AND CONTROL FUNCTIONS

The microcontroller (MCU) board and its operating program (firmware) handle internal monitoring and control functions in the chassis. The microcontroller board firmware begins execution after a RESET or power-up. The firmware instructs the MCU board hardware to collect samples of various chassis parameters, such as voltages and currents. Refer to the document following this for a table with a list of the parameters monitored in this chassis. The firmware determines the pass/fail status of each parameter by testing the sample values against fixed limits. The results of these tests are used to update the chassis front panel LED diagnostics.

The firmware uses the pass/fail state of some critical parameters to determine the control state of the chassis. For example, failure of one of these critical parameters may cause the chassis to disable RF power output. See the above-mentioned table for a description on the control action caused by failures of these parameters.

The chassis may be interfaced to a ComView master control station (MCS), allowing centralized monitoring and control; see document # DOC30-0005 in section 4 of this manual, for interconnections. The chassis and its internal MCU board are interfaced to the ComView RS485 network through the RS485 board at the rear panel and chassis internal harnesses; see document # DOC13-0009 in section 4 of this manual, for more information on the RS485 board. Messages sent by ComView are received by the MCU board and firmware and are processed by the firmware. The firmware responds to a ComView S*tatus Query* message by sending the current values of the parameters, listed in the above-mentioned table, over the network interface to ComView. The parameter names, current values, and other relevant information are displayed on ComView's *Detailed Status* screen.

ComView control commands are received and processed by the firmware, and the appropriate control action is taken by the firmware and MCU board. For example, if ComView sends the *STANDBY* command to the chassis, the firmware will instruct the MCU board to change the control state of the chassis to *STANDBY*. This will cause the RF power output to be disabled. Furthermore, a change in the chassis control state is indicated in the status information provided to ComView. ComView displays the current control state and the time that the last change in state occurred. For example, if the user sets the front panel control switch to the *STANDBY* position, the chassis will go to the *STANDBY* control state, and ComView will indicate that the chassis is in *STANDBY* and is generating no RF power.

For a more detailed discussion of ComView system functions and features, refer to the *ComView User's Guide*, document # 97-01030, which can be obtained from Comwave.

LIST AND DESCRIPTION OF PARAMETERS MONITORED IN VHF/UHF TO MICROWAVE UPCONVERTER CHASSIS

Parameter Name	*Test Type*	*Description*	*Priority (high: FAIL causes SHDN)*	*Latching in MCU (Cleared by STBY or RESET)*	*Latches the Fault Alarm Relay*
Transmit Status	PASS (in TRANSMIT state) if value is logic 1	Indicates the current state of the chassis. A zero indicates that this chassis is not outputting RF power, either because the chassis is in STANDBY or there are failures.			
Standby Switch Status	ON AIR if above low limit STANDBY if below low limit	Indicates control state from Front panel standby switch. A zero value indicates a shutdown command from this source. When chassis is in STANDBY, no RF power is output.			
Reflected Fault (shdn)	PASS (no refl fault) if value is logic 1	Failure of this logic parameter indicates high reflected power in this chassis. Failure causes shutdown of this chassis (see Reflected Power). This parameter is latching and may be cleared by cycling the equipment in and out of STANDBY or RESET.	High priority	Yes	Yes
VHF Detect	PASS if above low limit	Failure indicates loss of VHF input, resulting in shutdown of this chassis.	High priority		
LO Lock	PASS if above low limit	Failure indicates loss of LO phase lock, resulting in shutdown of this chassis.	High priority		
LO AGC	PASS if above low limit	Failure indicates that the LO signal is outside of its AGC range (level too low), resulting in shutdown of this chassis.	High priority		
AGC Signal	PASS if value is between low limit and high limit	Measurement of the VHF AGC level. Reading outside of limits will not result in shutdown of this chassis.	Medium priority		
ALC Signal	PASS if value is between low limit and high limit	Measurement of the RF output ALC level. Reading outside of limits will not result in shutdown of this chassis.	Medium priority		Yes

Created by: Kimberly Simeone 10/23/98	*Checked by:* Chris Smith 10/23/98	*Released by:* Carl P. Ungvarsky 10/23/1998

Parameter Name	*Test Type*	*Description*	*Priority (high: FAIL causes SHDN)*	*Latching in MCU (Cleared by STBY or RESET)*	*Latches the Fault Alarm Relay*
RF Power	PASS if value is between low limit and high limit	Value above or below limits indicates forward output power above or below 100% power. Value of approx. 1.4 indicates 100% power. Reading outside of limits will not result in shutdown of this chassis.	Medium priority		
Fault Alarm Relay	PASS if value is logic 0	If one or more of a selected group of parameters fails (see Latches the Fault Alarm Relay column), a hardware relay in this chassis will be actuated. The actuated state is controlled and latched by the MCU. For example, if Reflected Power fails, the chassis will shut down and the Reflected Power condition will not continue; however, the Fault Alarm Relay parameter will indicate FAIL since the relay is latched. Failure will not result in shutdown of this chassis.	Medium priority	Yes	
Thermal	PASS if above low limit	If chassis internal thermostat becomes excessively hot, value will rise above 2.5V (failure). Failure causes shutdown of this chassis.	High priority		
Remote A Remote B	If either value is logic 0, equipment will go into STANDBY state	Indicates state of control inputs from the switching control drawer. A zero value indicates a STANDBY command from this source.			
Interlock Status	PASS if value is logic 1	Logical ANDing of the states of the gate interlocks and PS Interlock (see below). Failure causes shutdown of this chassis.	High priority		

Parameter Name	*Test Type*	*Description*	*Priority (high: FAIL causes SHDN)*	*Latching in MCU (Cleared by STBY or RESET)*	*Latches the Fault Alarm Relay*
Gate Interlock 1 Gate Interlock 2 Gate Interlock 3 Gate Interlock 4 Gate Interlock 5		Measurements of the negative voltage fed back by an internal module to the chassis diagnostics. Failure of a parameter indicates short circuit, open circuit, of fault condition in chassis internal interlock harnessing. These parameters may indicate WARNING during stabliization of the chassis after turn-on. Failure causes shutdown of this chassis.	High priority		
PS Interlock	PASS if value is between low limit and high limit	Failure of this parameter indicates chassis internal switching power supply voltage is above or below safe limits. Failure causes shutdown of this chassis.	High priority		
Negative12V PS Positive11V PS Positive12V PS	PASS if value is between low limit and high limit	Measurements of output voltages of power supplies. Readings outside of limits will not result in shutdown of this chassis.	Low priority		
IP1 IP2 Final Current	PASS if value is between low limit and high limit	Measurements of amplifier currents. Readings outside of limits will not result in shutdown of this chassis.	Low priority		Yes
Fwd Output Power	PASS if value is between low limit and high limit	Indicates overall system power (forward) output. Reading outside of limits will not result in shutdown of this chassis.	High priority		
Reflected Output Power	PASS if below high limit	Indicates system reflected power. Typical value should be close to 0V. Failure occurs when value rises above 0.632V, resulting in shutdown of this chassis. Following a shutdown due to high reflected power, the Reflected Fault (shdn) parameter will indicate failure.	High priority		Yes

SIGNAL DISTRIBUTION BOARD

The signal distribution board receives and distributes various interlock and turn on signals that control transmit operation. The board contains 3 LED's and a switch. Under normal operating conditions all LED's illuminate.

DS2	green:	Video input signal is present.
DS3	yellow:	Power supply enable present.
DS4	red:	Interlock conditions present.

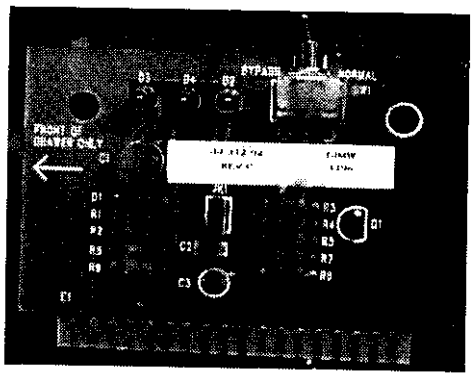


FIGURE 13-0064-1

Switch SW1 is a video bypass enable switch. It provides +5 VDC to bias Q1 on thereby enabling DS2. The normal position for this switch is OFF. When the switch is OFF, an external input video presence signal must be supplied to turn the transmitter ON. This signal typically originates from a video presence board contained inside the modulator. When this switch is positioned ON, this places the transmitter into BYPASS mode or in a constant ON condition. This enables the transmitter to continue transmitting even though there is no video signal present.

The following chart cross-references these input/output signals:

SIGNAL	INPUT	OUTPUT	ORIGIN/DESTINATION
PS Enable		X	Switching Power Supply
Thermal	X		Thermal Relay
Remote A	X		External Connector J1-2
PS Interlock	X		Motherboard P4-10
Remote A		X	Motherboard P4-15
IN-Signal		X	Motherboard P4-14
Interlock	X		Motherboard P4-12
TX-ON	X		Motherboard P4-11
Stand-by	X	X	Motherboard P4-2
Thermal		X	Motherboard P4-13
+ 5 VDC	X		Motherboard P4-5
Gate 5	X		Motherboard P4-9
Gate 4	X		Motherboard P4-8
Gate 3	X		Motherboard P4-7
Gate 2	X		Motherboard P4-6
Gate 1	X		Motherboard P4-4
Remote B	X		Motherboard P4-3
Video Presence	X		External Connector J1-1

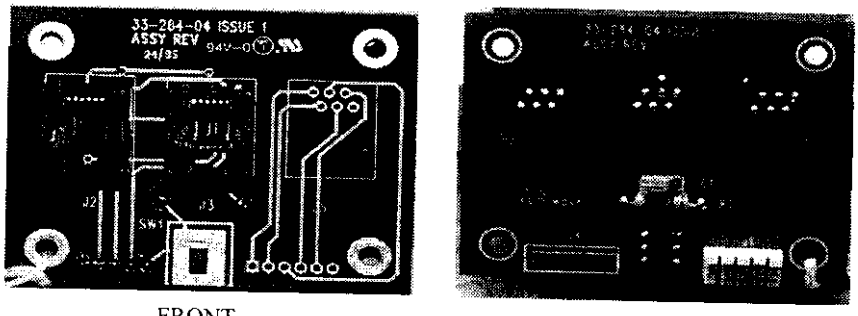
FIGURE 13-0064-2

RS-485 COMMUNICATIONS BOARD

An RS-485 communications board is mounted to the inside rear of the chassis. It interfaces each drawer's microcontroller unit (MCU) to a communications bus for status monitoring with a common computer/master control station. The system is capable of monitoring up to 32 individual units.

The board has a 5 pin input connector with connections to two rear panel mounted 6 pin telephone type receptacles (RJ11). It functions as the interface between the drawer's MCU, the communications bus, and a computer monitoring system. The bus consists of a double twisted shielded pair cable which daisy-chain links (parallels) drawers to a common computer for complete system status monitoring.

A board mounted mini DPDT DIP switch labeled as NETWORK END TERMINATION is accessible on the RS-485 communications board located on the rear of the sub-rack. When a status monitoring computer system is used, all RS-485 communications boards ordinarily have this switch set to the "OUT" position with the exception of the last RS-485 communications board in the daisy chain series. The last board normally has the switch set to "TERM". This action terminates the communications bus at the last RS-485 communications board of the daisy link chain establishing proper bus impedance. The interconnection is shown in Document # DOC30-0005.



FRONT 33-284 BOARD BACK

FIGURE 13-0009-1

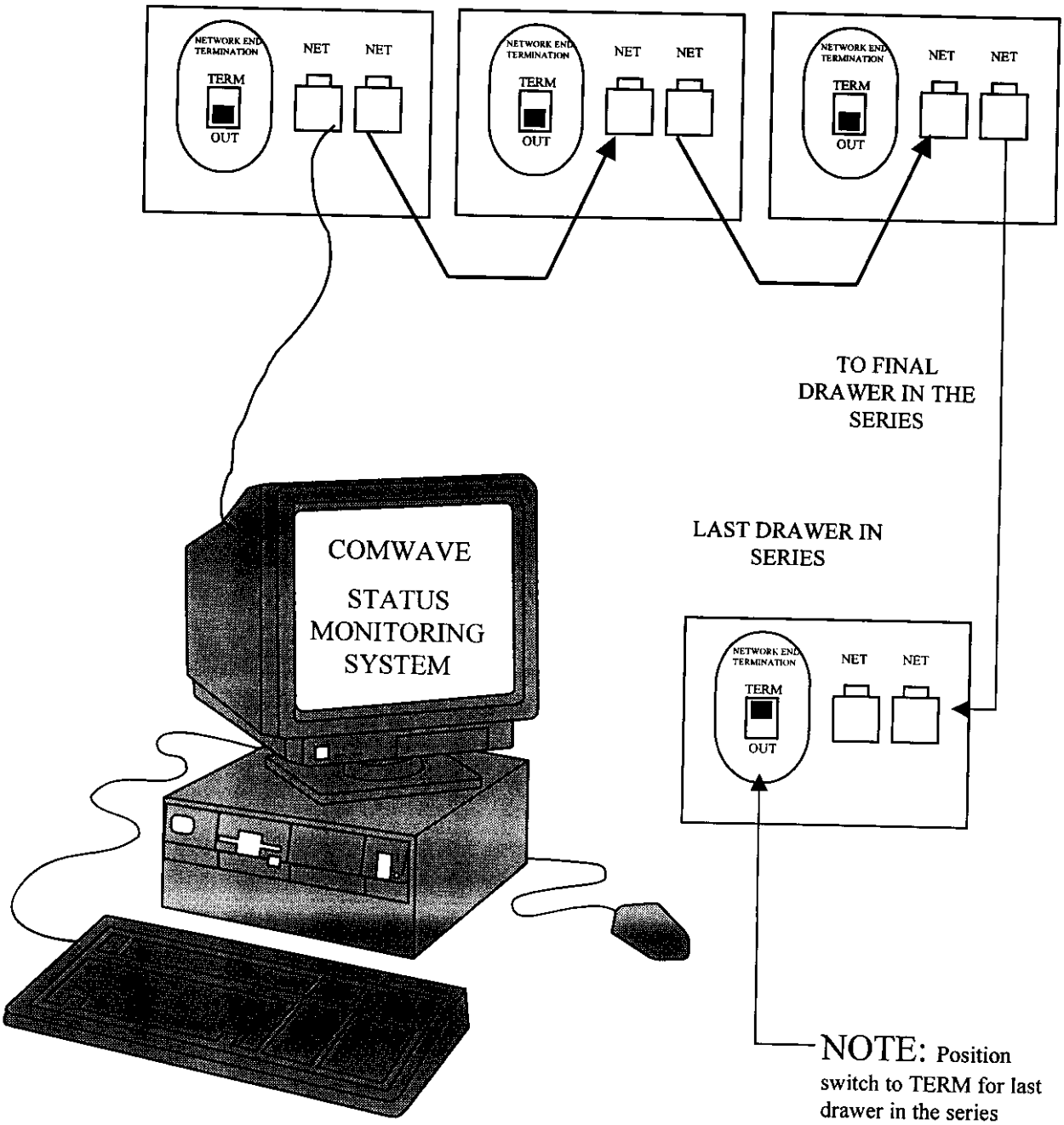
FRONT 33-304 BOARD BACK

FIGURE 13-0009-2

Created by: Kimberly Simeone *9/15/98 ECO #: 98-116*	*Checked by:*	*Released by:* 10/20/98.

Document #: DOC13-0009
REV: C

COMVIEW STATUS MONITORING INTERCONNECTIONS



IBM COMPATIBLE
WITH RS-485 CARD

Created by: Kimberly Simeone 9/3/98	*Checked by: Jeanette Mulligan 9/4/98*	*Released by:* Paul Lewis 10/19/98

Document #: DOC30-0005

REV: A

POWER AMPLIFIER SEGMENT THEORY OF OPERATION

POWER AMPLIFIER SEGMENT GENERAL DESCRIPTION:

The power amplifier segments of the high power single channel transmitter series or broadband booster series use the latest technology in power FET's. The transistors provide high output power, as well as more linearity and higher efficiency. Mechanically, the power amplifier segments have a plug-in architecture that allows hot replacement. In addition to hot replacement, the architecture of the amplifier enables flexibility to tailor the system to higher output power levels and can be easily upgraded.

The power amplifier segment consists of a microwave amplifier(2), control board(1), DC to DC converter(3), and a front panel. A microcontroller system, located on the control board, supervises and controls the power amplifier segment in each of its functions. The DC to DC converter reduces 48 V_{DC} front-end power supply input to the nominal amplifier voltage of 10.5 V. The front panel displays the status of the amplifier segment and interfaces the control board to a computer by means of a serial RS-232 port(4).

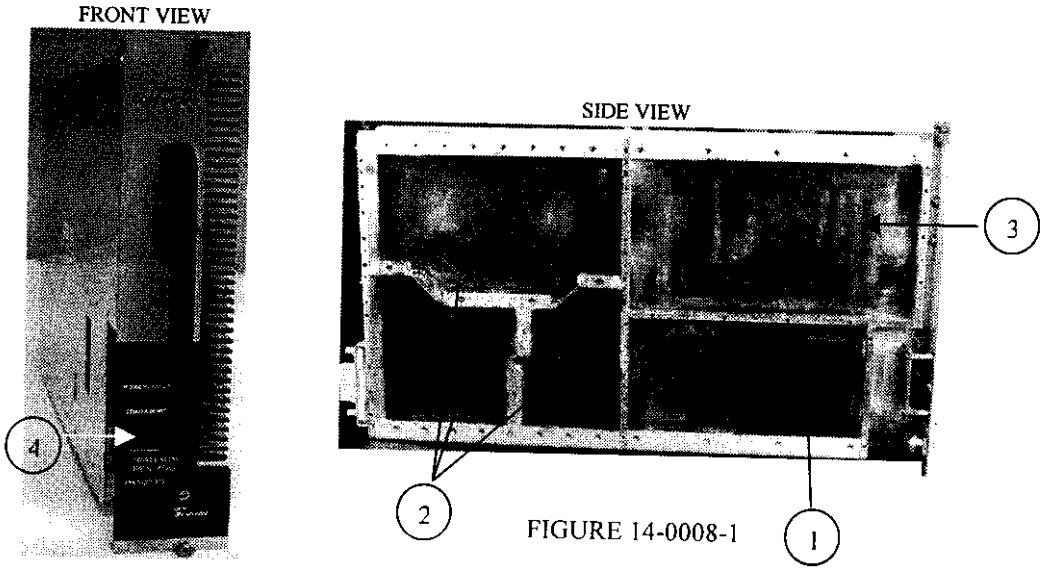


FIGURE 14-0008-1

POWER AMPLIFIER SEGMENT OPERATION

The amplifier segment is equipped with a key lock switch on the front panel to retain it in place. When pushing-in or pulling-out the Segment, turn the key lock switch to the OFF position. After plugging the amplifier segment into the sub-rack and tightening the front panel thumbscrews, turn the key-lock switch to the ON position. The 10 V_{DC} secondary power supply will start up the control board, which applies a negative voltage to the gates of the FET's and turns the DC to DC converter on. It also adjusts the transistor's current

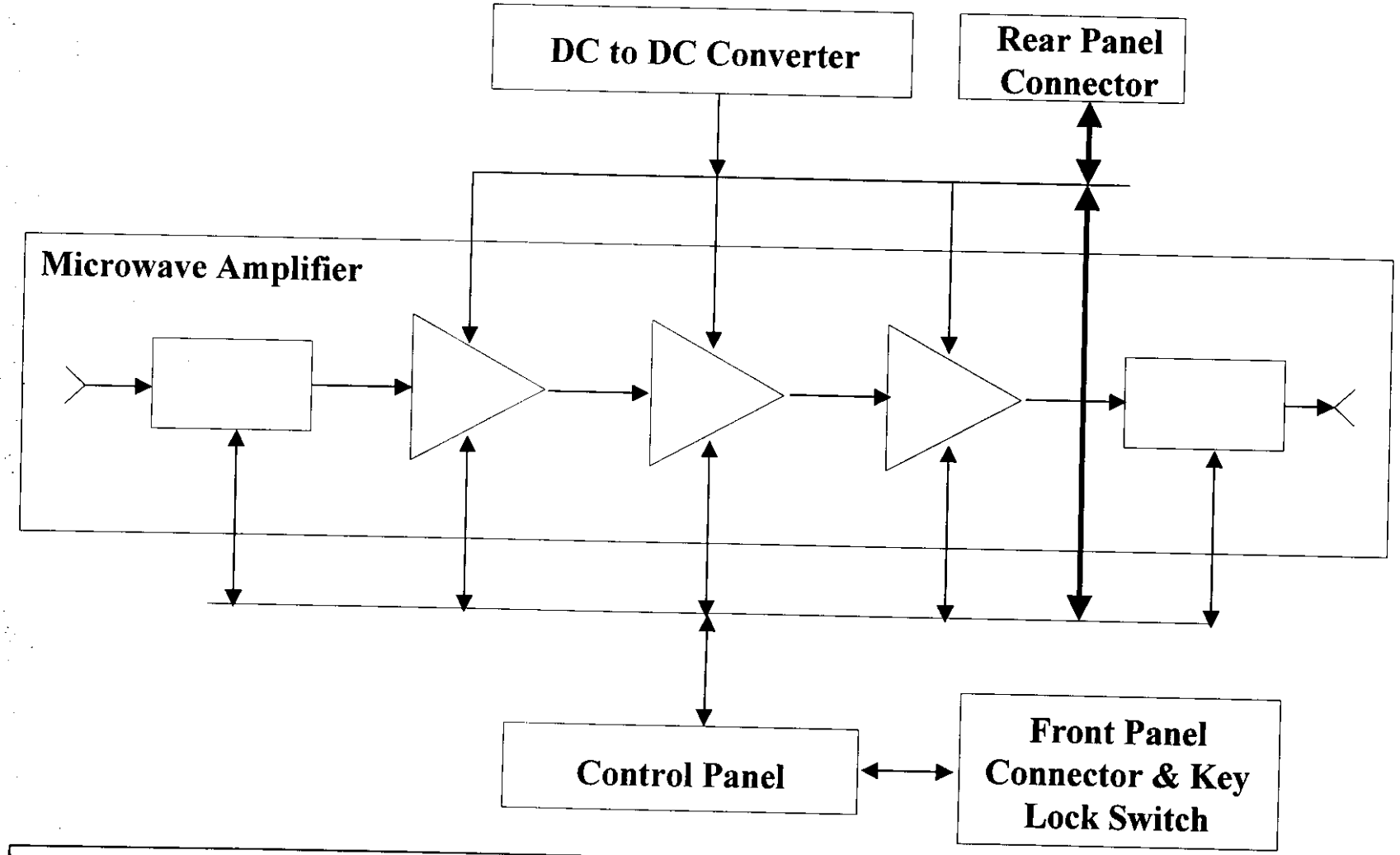
and releases the input signal to the microwave amplifier. The airflow passes through the heatsink from the front to the rear of the sub-rack. The airflow loss to the other power amplifier segments during hot replacement is negligible.

POWER AMPLIFIER SEGMENT SPECIFICATIONS

Parameter	*Specification*
Primary DC Voltage	48 V
Primary DC Current	4.9 A
Secondary DC Voltage	10 ±0.5 V
Secondary DC Current	0.4 A
Communication Port	RS-232 and RS-485
Input Power	Digital 12.0 dBm Analog 17.5 dBm (@ P1 dB)
Output Power	Digital 41.5 dBm Analog 47.0 dBm (P1 dB)
Dimensions	2.1"H x 10.3"W x 17.1"D 5.3 cm H x 26.1 cm W x 43.4 cm D
Weight	9 lbs (4 Kg)

DOCUMENT #: DOC19-0014
REV: C

POWER AMPLIFIER SEGMENT BLOCK DIAGRAM



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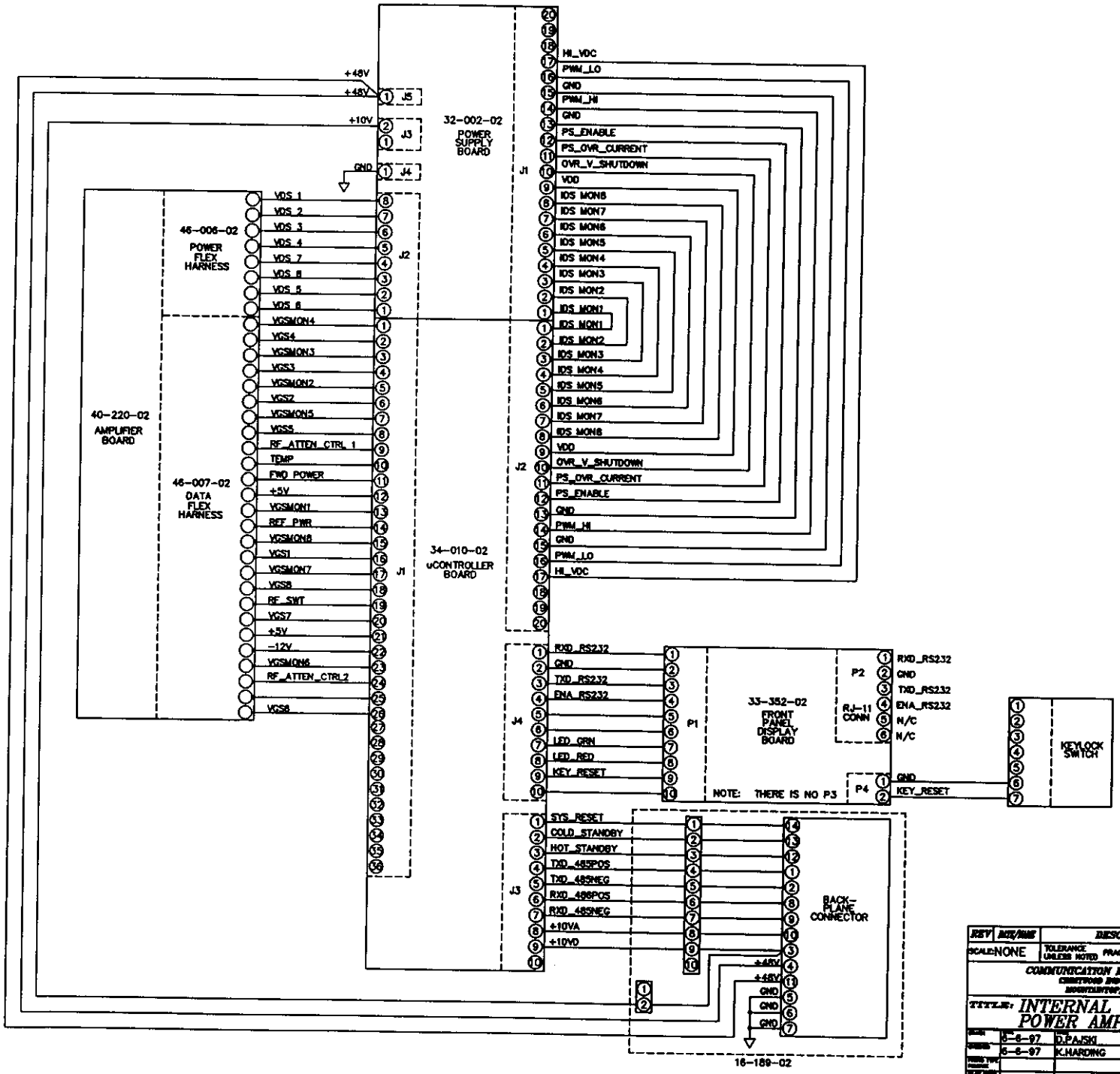
REV: C



REV	BOE/DME	DESCRIPTION	ECO No.
SCALE: NONE	TOLERANCE UNLESS NOTED	FRAC.± 1/8 DEC.± .005 ANG.± 5	

COMMUNICATION MICROWAVE CORP
CRESTWOOD INDUSTRIAL PARK
MONTGOMERY, PA., 18707

TITLE: INTERNAL INTERCONNECT, POWER AMPLIFIER SEGMENT

DRAWN	6-6-97	D.PAJSKI	DWG NO. C-66-306-01
CHECKED	6-6-97	K.HARDING	SHEET 1 OF 1
MANUFACTURING APPROVAL	6-11-97	A.BRAGALONE	APPLICABLE PART NUMBERS PT=A

REV. A

POWER AMPLIFIER BOARD

POWER AMPLIFIER BOARD GENERAL DESCRIPTION

The power amplifier board has a high gain architecture, providing 29.5 dB gain and an output 1-dB compression of 47 dBm. The input signal passes through a microwave switch for hot stand by operation. This feature allows the control board to set up all DC parameters and check for proper amplifier operation without the influence of an RF signal. The signal then passes through a pin diode attenuator that sets the overall gain of the amplifier.

In the first stage, a 3-dB hybrid provides a reliable load to the driver and a flat broadband frequency response to the amplifier. The second and third stages of amplification provide the proper output power with minimum distortion and high efficiency. A low output VSWR (Voltage Standing Wave Ratio) is provided by the 3 dB combining system. The directional coupler provides a sample signal proportional to the forward and reflected power. This measurement ensures that the amplifier delivers the correct power. An IC measures the operating temperature of the amplifier that is monitored by the MCU. The amplifier is placed in a faulted state if the temperature exceeds a limit set by the MCU.

POWER AMPLIFIER BOARD OPERATION

The control board acknowledges the input signal presence from the driver. It places the microwave switch in the hot stand-by mode and adjusts the current of each FET. The current sensor, located on the power supply, provides the current samples to the control board to check for proper operation of the transistors. The control board sets the variable attenuator to the correct amplifier gain, and removes the microwave switch out of "STANDBY" and into the through path.

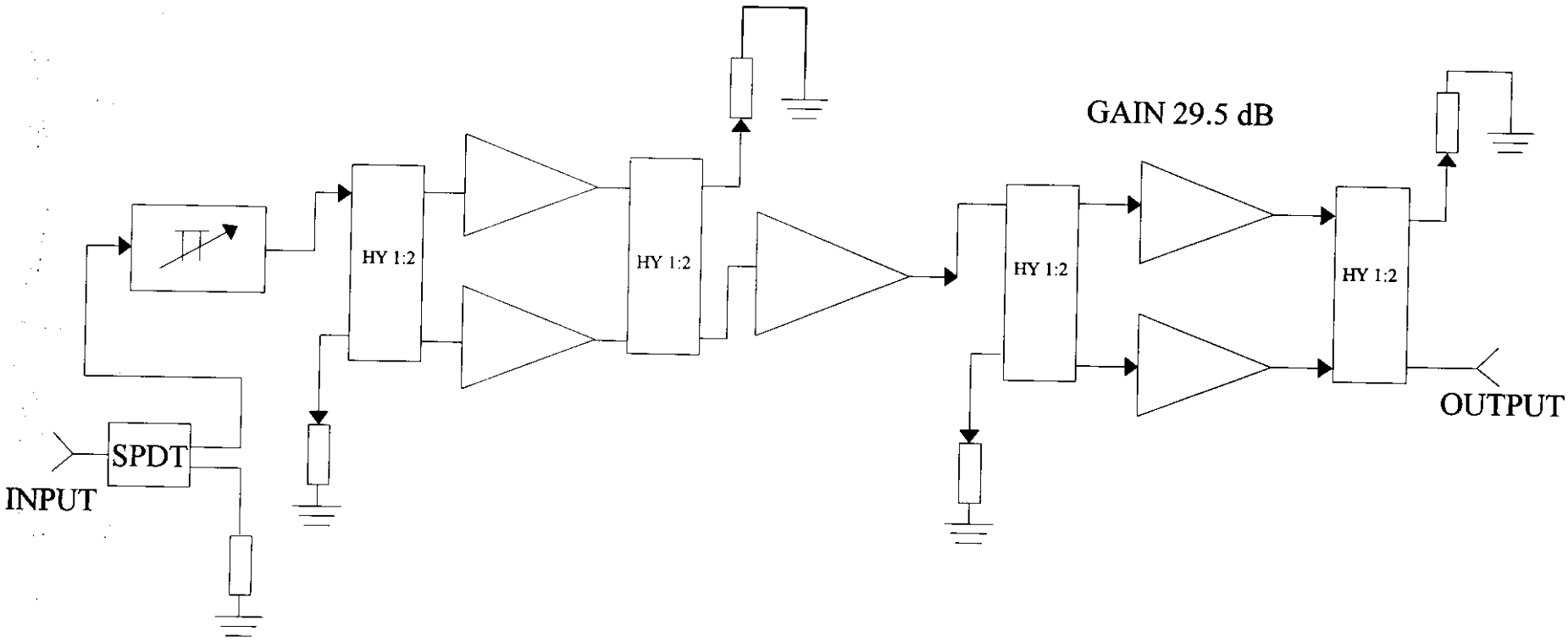
The microwave circuit amplifies the input signal with high linearity performance and broadband frequency response. This feature allows the amplifier to be used for any channel without retuning. An IC on the amplifier board protects the FET's from catastrophic failure. The temperature sensor supplies the control board with a voltage proportional to the heatsink temperature. The microcontroller will sense this voltage and protect the amplifier against high temperature or from failure of the cooling system. The output directional coupler measures the forward and reflected power. These measurements provide the microcontroller with the information needed to verify the status of the amplifier.

POWER AMPLIFIER BOARD SPECIFICATIONS

Parameter	*Specification*
Input DC Voltage	10.5 V
Input DC Current	19.8 A
RF Gain	29.5 dB
Output Power	47 dBm
Flatness (BW 200 MHz)	±.5 dB
Input VSWR	1: 1.6
Output VSWR	1: 1.5

DOCUMENT #: DOC19-0015
REV: C

POWER AMPLIFIER BOARD BLOCK DIAGRAM



Created by: Kimberly Simeone 9/15/98 *ECO #: 98-116*	*Checked by:* Donald Ahn 10/08/98	*Released by:* Paul Lowie 10/9/98

Document #: DOC15-0014

REV: B

300 WATT POWER SUPPLY BOARD

300 WATT POWER SUPPLY GENERAL DESCRIPTION

The power supply board consists of two DC/DC converters, input and output voltage monitoring, standby switching, over-voltage protection, and current sensing. All functions of the power supply board are interfaced with the control board.

The power supply reduces the high voltage, low current front-end power supply input to the nominal output voltage of 10.5 volts. The DC/DC converters are high power density, high efficiency, switching power supplies. The over voltage protection consists of a voltage detector, a crowbar, and the fusing. The standby switching uses a high efficiency FET.

300 WATT POWER SUPPLY GENERAL OPERATION

After engaging the power amplifier segment, the control board checks the input voltage and turns the FET switch on. The DC/DC converter has a master/slave configuration, which provides the total current for the RF amplifier. This configuration allows for accurate current sharing between the master and the slave.

The control board will then detect the output voltage. If the output voltage rises above the nominal value to a preset value, the crowbar will be activated and cause the fuse to open. When this occurs the control board will disable the standby switch and the DC/DC converters. The power supply distributes eight lines of power with current sensing. These lines are monitored by the control board and used for the current control loop.

300 WATT POWER SUPPLY BOARD SPECIFICATIONS

Parameter	*Specification*
Primary Input Voltage	48 Volts DC Nominal
Primary Input Voltage Range	36 to 76 Volts DC
Primary Input Current	7.5 Amps DC @ 48 Volts DC
Primary Input Current Range	10.0 to 4.7 Amps DC
Secondary Input Voltage	9 Volts DC
Secondary Input Current	10 Milliamps DC
Output Power	300 Watts maximum
Output Current Limit	105 to 135% of Max. rated power
Efficiency	83 to 88%

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REV: C

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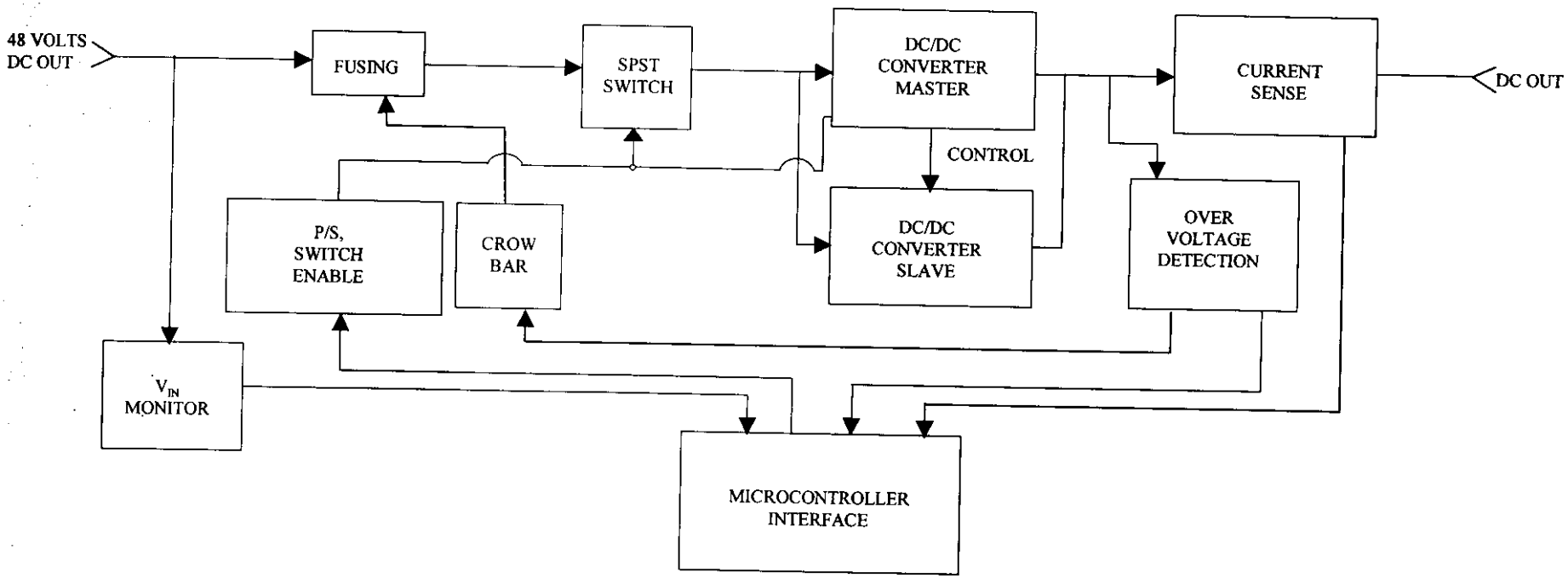
POWER SUPPLY BLOCK DIAGRAM



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Document #: DOC15-0016

REV: C

CONTROL BOARD

Monitoring and control of the power amplifier segment is accomplished through a control board located within a section of the segment housing. The control board utilizes an 8-bit microcontroller unit (MCU) with on-board memory to perform the monitoring and control functions. The control board circuitry includes analog signal conditioning, A/D and D/A converters, supply voltage regulation, and two serial data interfaces.

Monitoring operations involve collecting analog signals and logic data from the power amplifier segment. Analog inputs - forward power, reflected power, and temperature are received from the RF power amp connector J1. Analog inputs drain supply voltage (V_{DD}) and high voltage DC are received from the power supply connector J2. Forward power and reflected power inputs are amplified by op-amps with a gain of approximately 3, while temperature, drain supply voltage (V_{DD}) and high voltage DC are buffered by unity gain stages. Following the V_{DD} buffer stage, a resistor divider network scales V_{DD} to 1/4 its input voltage, followed by a second unity gain buffering stage. Each of these inputs are voltage-limited to 5.1 V_{DC} by means of Zener diodes at the input to the control board. They are protected from voltages more negative than -0.4 V_{DC} by Schottky diodes at the output of the op-amp gain stages to protect the MCU A/D converter inputs.

The control board monitors drain currents drawn by FETs in the RF power amplifier section of the power amplifier segment. The control board achieves this by monitoring the voltages dropped across series resistors in the drain supply circuits on the power supply board. The control board from the power supply connector J2 receives these eight voltages. Each signal is selected by the MCU and related CPLD logic through an 8-channel analog multiplexer (MUX) IC, and in turn compared to V_{DD} by a differential amp/gain op-amp stage. The resulting outputs are 10 times greater than the voltages dropped across the series monitoring resistors. These outputs are protected from voltage excursion greater than 5.1 V_{DC} by Zener diodes, and from excursion more negative than -0.4 V_{DC} by Schottky diodes. The resulting signal is connected to input AN0/IDSMON on the MCU A/D converter. This signal varies through time with each of the eight monitored signals as selected by the MCU.

The control board generates negative FET gate supply voltages with a D/A converter and analog voltage inverter circuits. The 8-bit D/A IC is provided with a 2.5 V_{DC} reference and with data from the MCU to set the output voltage on each of 8 channels to a positive voltage of the same value as the absolute value of the desired gate voltage. Unity gain inverter op-amp circuits to negative voltages (e.g. -Vgs) then invert these positive voltages (e.g. +Vgs). The negative gate voltages are output to the RF amplifier section on RF power amplifier connector J1.

The negative FET gate supply voltages supplied to the RF power amplifier section are returned to the control board through internal segment harnessing. These returned gate voltages provide the control board with monitoring of the gate voltages arriving at the RF

amplifier section, allowing incorrect gate voltage or gate interlock break to be detected. A MUX IC in a manner similar to that for the drain MUX described above multiplexes the monitored gate signals, input on RF power amplifier connector J1. A unity gain inverter op-amp circuit to provide a positive voltage to the AN1/VGSMON input on the MCU A/D converter inverts the time-varying MUX output, which generally carries negative voltages.

The control board provides various logic inputs and outputs. A drain supply enable logic signal, PS_ENABLE, is output from the control board on J2. The state of PS_ENABLE is controlled by the MCU, which tests other signals such as Standby and Gate Voltage Interlocks, to determine if it is safe to enable the power supply. The MCU outputs the Enable Signal to the CPLD, which in turn outputs the PS_ENABLE on J2. If the MCU detects a condition in which it would be improper or unsafe to allow the drain supply to operate, the CPLD will be made to output a logic-LOW on the PS_ENABLE control output.

Output signals, which control the RF power amplifier section RF switch and attenuator, are generated on the control board. Signal RF_SWT, output on connector J1, controls the terminated or unterminated state of the RF power amplifier section RF switch. RF_SWT is driven to a logic-HIGH when the power amplifier segment is set to the TRANSMIT state. This logic-HIGH will cause the RF switch to route the RF amp microwave input signal into the amplifier circuitry. Signals RF_ATTEN_CTRL1 and -2 are analog outputs that reciprocate to control the branches of the RF attenuator network located in the RF amplifier section. These analog voltages are developed in a D/A converter IC and NPN and PNP transistors.

The serial input/output (I/O) capabilities of the power amplifier segment originate on the control board and the MCU's SCI port. In general, the power amplifier segment may be connected on an RS-485 multidrop network as an individually addressed node with other power amplifier segment nodes. Node address switch SW1 is a DIP multi-pole switch, which is programmed with a power amplifier segment's unique node address in binary form. While present on the network, a power amplifier segment may be issued specific commands from and return formatted responses to a master communications device. By default, the RS-485 driver IC is enabled and RS-485 serial I/O is available at the board's J3 backplane connector. An RS-232 serial I/O port is also available but the RS-232 driver IC is disabled by default. This port is interfaced through an RJ-11 connector on the power amplifier segment front panel. When the ENA_RS232 control input line is given a logic-LOW (as when the proper interface cable is plugged into the power amplifier segment RJ-11 connector), the RS-232 port is enabled. At this time, the RS-485 port is disabled, causing a loss of communications with the RS-485 network. The same power amplifier segment command and response capabilities available on the RS-485 port are provided on the RS-232 port.

A computer operating properly 'watchdog' function is provided on the control board to safeguard against loss of MCU program control. Under normal circumstances, MCU IC input lines RESET and XIRQ will be provided with a logic-HIGH by an on-board

watchdog IC. If Jumper JK3 is in place, the CPLD device must provide a toggle in the CPLD WDI Output line every 1.6 seconds to indicate to the watchdog IC that the MCU is operating properly. The CPLD will interpret a PG3/WDI input from the MCU, or activity on the UC_RS485_ENA control line, or activity on the RS-485 communications lines, as indications that the MCU is operating properly, and will toggle the CPLD WDI output line. If a toggle in the WDI line does not occur within 1.6 seconds, it is assumed the MCU is no longer executing the desired program properly. The watchdog IC will drive low the XIRQ signal, which will ultimately result in a reset of the MCU and restart of the MCU program.

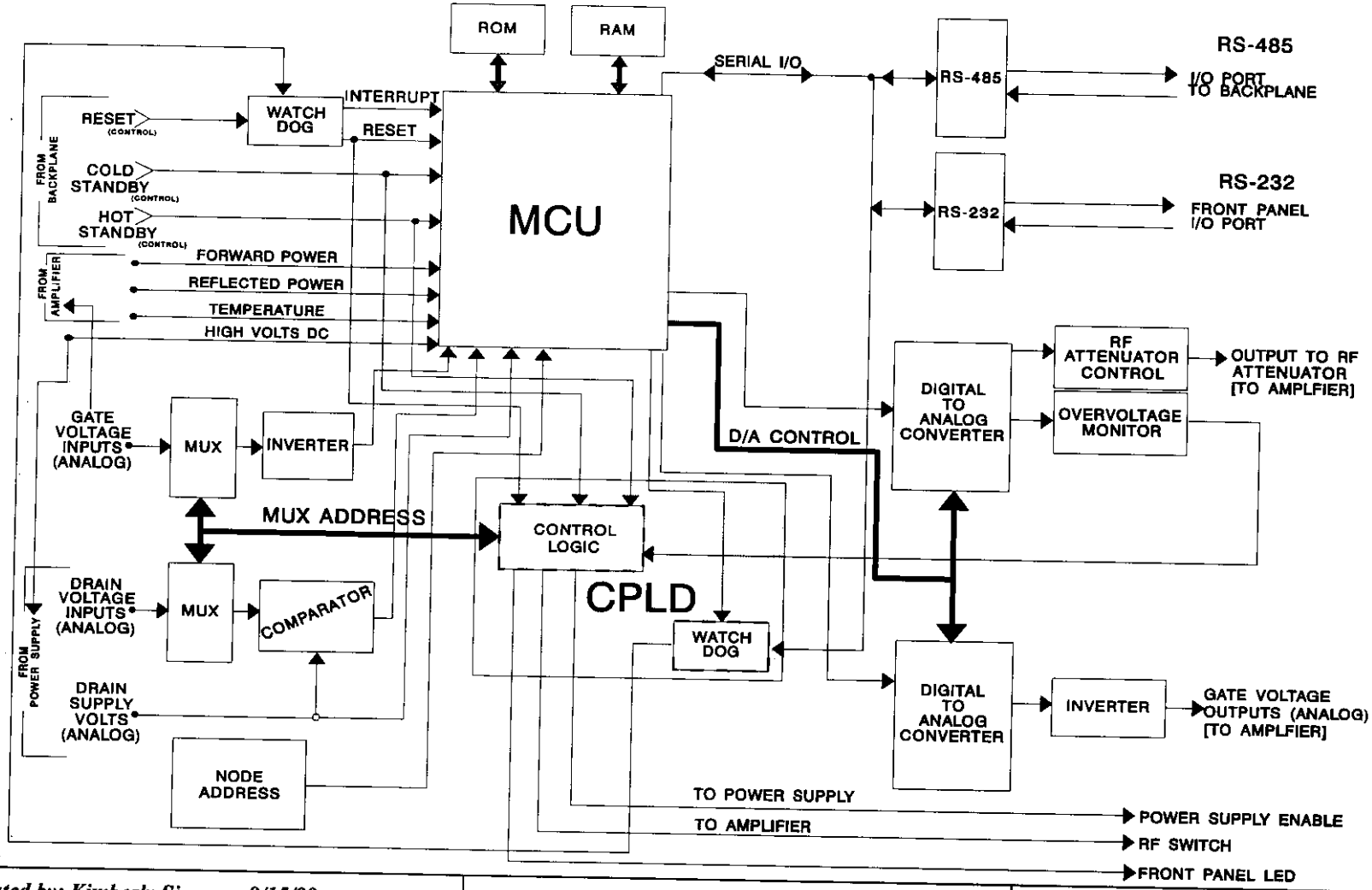
Two power supply voltage inputs of approximately +10 V_{DC} are provided to the Control Board to supply the digital regulator and analog regulator circuits. The digital regulator circuits are fused by F1 at their +10 V_{DC} input. A linear voltage regulator develops +5V_{DC} for the digital circuitry. The +5 V_{DC} digital circuit has a separate ground plane for the digital devices. A switching regulator IC and associated components develop DC output voltages of approximately ±14.5 V_{DC} which are then regulated by linear regulators to +12 V_{DC} and -12 V_{DC} for various digital and analog circuitry. The +5 V_{DC} analog regulator is supplied from a +10 V_{DC} input separate from the digital +10 V_{DC} input, and is fused by F2. Another linear voltage regulator develops +5 V_{DC} for the analog circuitry. The +5V_{DC} analog circuit has a separate ground plane for the analog devices.

CONTROL BOARD SPECIFICATIONS

Parameter	*Specification*
Microcontroller type	8-bit MCU with 64 K address space
DC Input Voltage	10.0V ± 0.5 V
DC Input Current	400 mA typical @ 10.0 V
Operating Temperature	0° C to +50 ° C
Communication Ports	1: RS-485; 1: RS-232
Program stall time before COP Watchdog Reset	1.6 seconds
Number of Analog Inputs	21
Number of Logic Inputs	7
Number of Analog Outputs	10
Number of Logic Outputs	6
Physical Dimensions	5.125" H x 3.50" W x 0.58" D typ 13.0 cm H x 8.9 cm W x 1.5 cm D typ

DOCUMENT #: DOC19-0016
REV: C

CONTROL BOARD BLOCK DIAGRAM



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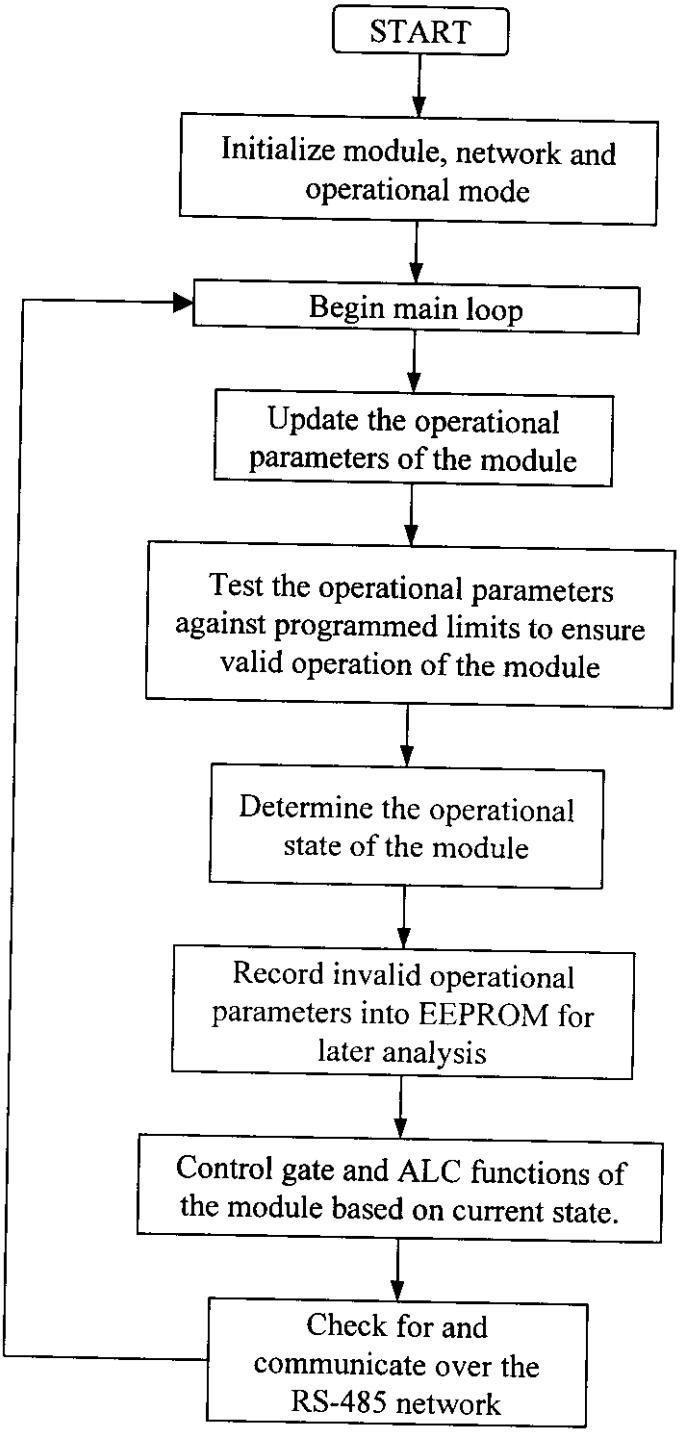
Document #: DOC15-0015

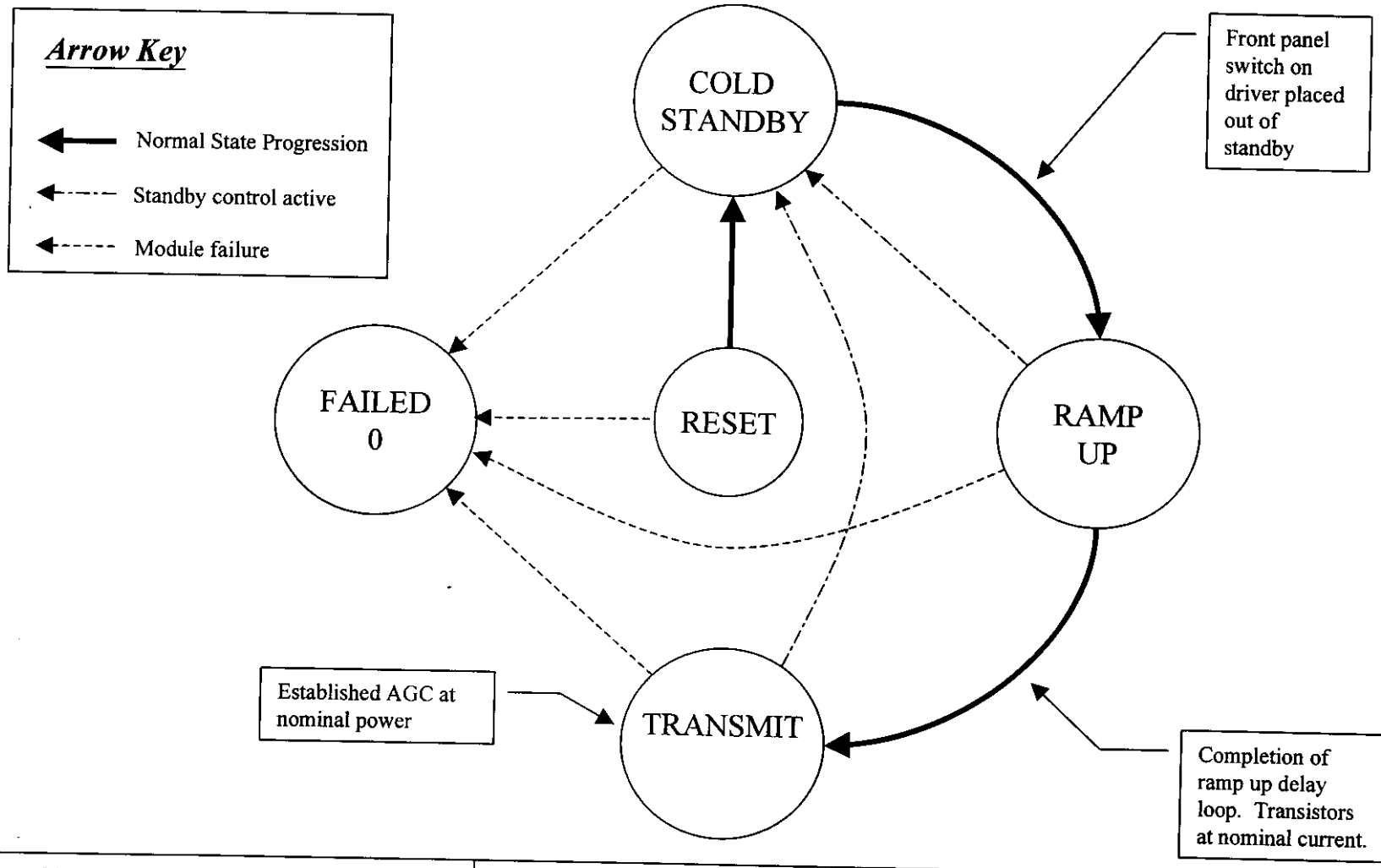
REV: C

FIRMWARE FLOWCHART



Created by: Kimberly Simeone 11/20/98	*Checked by: Christian Smith 11/23/98*	*Released by: Donald Wike 11/23/98*

AMPLIFIER SEGMENT STATE FLOW DIAGRAM



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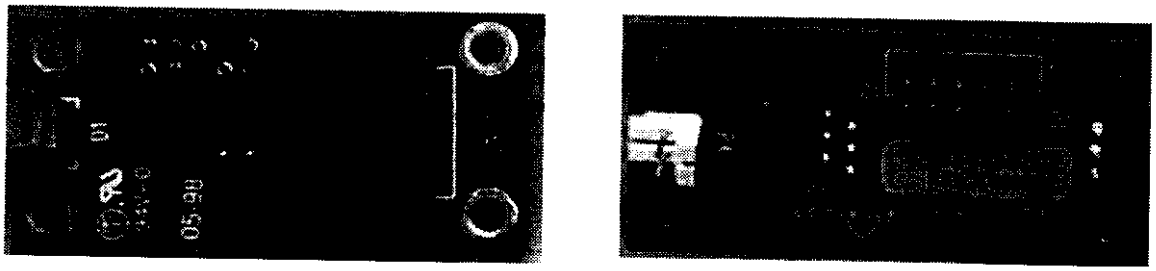
Document #: DOC21-0006

REV: A

RS-232 COMMUNICATIONS BOARD

An RS-232 communications board is mounted to the inside front of the chassis. It allows the drawer to be interfaced to a personal computer for both monitoring and control.

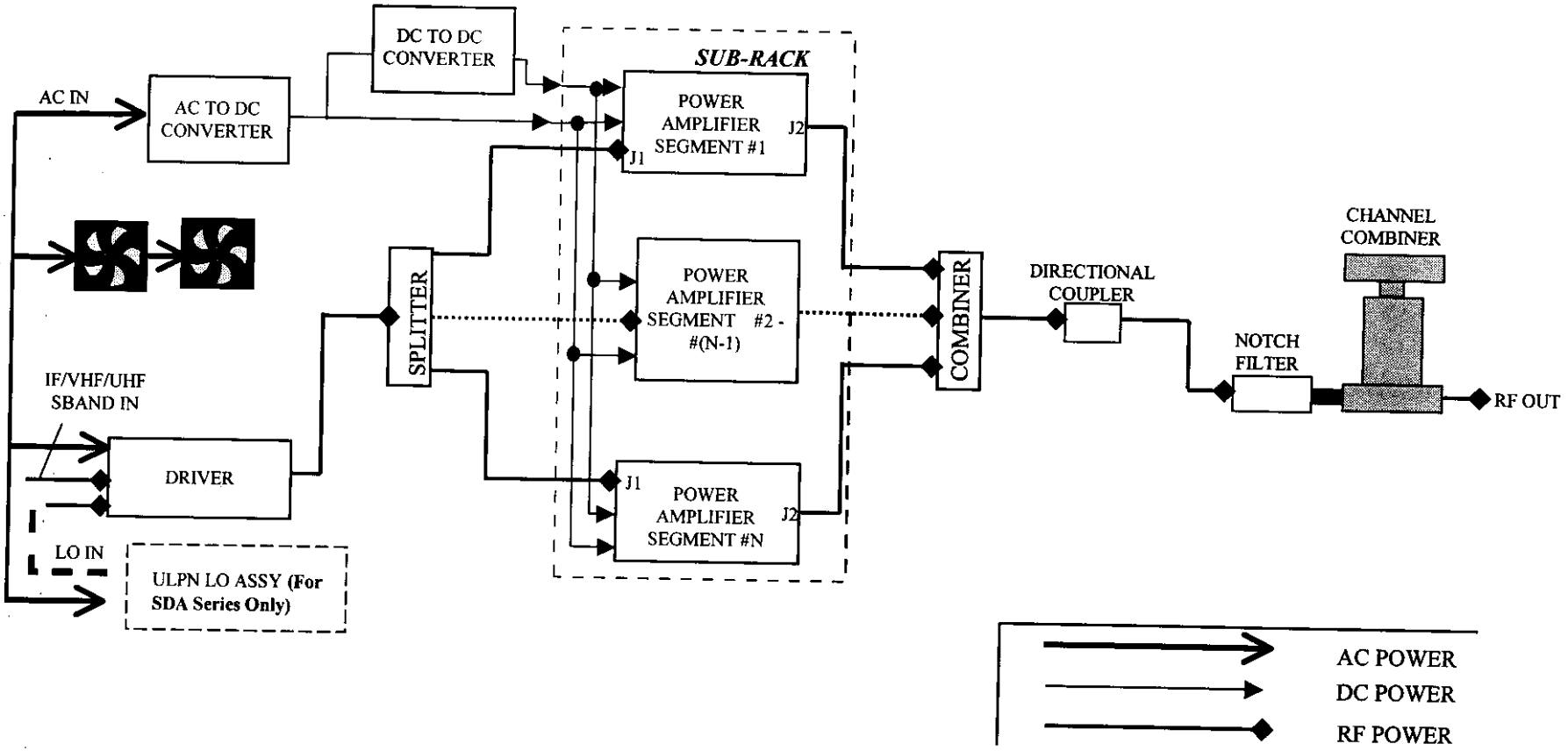
The board has a 10 pin input connector with connection to a 6 pin telephone type connector (RJ11). Additionally, the board has a bi-color LED that can be used to indicate the overall status of the drawer in which it is being used, and/or whether the drawer is receiving power.



FRONT 33-352 BOARD BACK

FIGURE 13-0010-1

SBM/HPB/SD/SDA HIGH POWER SERIES BLOCK DIAGRAM OF RACK SINGLE TRANSMITTER SHOWN



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Document #: DOC15-0009

REV: E