PROFESSIONAL TESTING
EUT DESCRIPTION AND OPERATION

1.0 EUT DESCRIPTION

The **Trimble Navigation (Limited) TS100 ATCRBS Transponder** is a Mode C navigation transponder. The TS100 is intended for use in general aviation aircaft. The device responds to Mode C compliant radar navigation interrogations with a 127 watt peak code pulse. Altitude of the aircraft is automatically reported as part of the interrogation response with the aircaft ID code. This equipment is not marketed with an antenna or associated wiring or adapters.

2.0 MODE(S) OF OPERATION

The transceiver was tested in the normal mode of operation. With no interrogation input signal, the EUT is in the receiver mode of operation. A one meter cable with a 50 ohm load was placed on the end of the EUT to simulate a wiring load. For antenna conducted emissions tests, the antenna port was connected directly to the spectrum analyzer input.

3.0 Theory of Operation

The theory of operation for this device is described in the following pages. These pages were extracted from the Manual for the **TS100**. It should be noted that some references may appear for the TRT250D. The TRT250D was the initial reference designator for the **TS100**.

The manual pages shown on the following pages are from the maintenance manual for the **TS100.** The EUT does not possess any operator adjustable components which would affect the frequency or output power level of the device. The operator may change the format and content of the reply message, but does not have the capability to change the frequency, bandwidth or power of the reply.

SECTION V

THEORY OF OPERATION FOR THE TERRA TRT 250D

The TERRA TRT 250D is divided into six functional subassemblies. The subassemblies are; 1) Receiver, 2) Digital Board, 3) Modulator/Power Supply, 4) Transmitter, 5) Controller and, 6) Display.

5.1 RECEIVER

Use Schematic #9-1100-0006-04 and Component Locator #9-1120-0002-02 to aid in understanding the following circuit description.

The input RF is filtered in a four pole microstrip filter with tuning adjustments made with C29-C32. The balanced mixer, comprised of CR1 and associated coupling elements, converts the 1030 MHz RF signal to 60 MHz. The local oscillator, Q1, is tuned by a microstrip 1/4 wave resonator and C28, L13, C39 form a 30 MHz trap then the local oscillator is coupled to the mixer through the balun made with hard line coax.

The first IF amplifier, Q2, is coupled to the input through a wide band single-tuned filter, L1, C38 and R23. The output is coupled with the double-tuned circuit consisting of C33, T2, C9, C12 and T3. The output double-tuned circuit is over-coupled to provide an essentially flat bandpass when combined with the input coupling circuit.

Following the first IF amplifier is the log IF amplifier. The logarithmic characteristic of the amplifier is achieved by use of successive detection in each amplifier stage. Under small signal conditions the amplifiers Q3-Q6 act as linear amplifiers driving the detector stage comprised of Q7, C24 and R22. As the input signal level is increased, Q6 will be over-driven and collector saturation will occur. The increase in collector current will be increased as each preceding stage reaches saturation and adds a linear increase in the total output current. Since each stage has the same gain of approximately 10dB, a linear increase of the output is achieved for a logarithmic change in the input. The interstage coupling consists of a series resonant circuit tuned for 60 MHz.

5.2 DIGITAL BOARD

Use Schematic #9-1100-0005-04 and Component Locator #7050-1128-02 for units S/N 1305 and below, or schematic 9-1100-0129-04 and component locator 7050-0053-03 for units, S/N 1306 and above, to aid in understanding the following circuit description.

The detected video output from the Receiver is filtered with R16 and C7, then amplified and inverted in the video amplifier, Q4. The signal is then processed in the "ditch digger" circuit comprised of Q3, R8 and C4. R28 and C11 are included in the circuit to sharpen the pulse rise time and reduce overall delay jitter.

The application of a pulse to Q3 causes C4 to be charged to the peak amplitude of the pulse and the collector of Q3 to have a large negative pulse corresponding to the input pulse. R8 will discharge C4 at a controlled rate so that small pulses occurring very soon after the first pulse will not cause an output pulse on the collector of Q3. This controlled discharge rate provides

5.2 DIGITAL BOARD (Continued)

or the rejection of small P2 pulses, but will still allow the detection of large P2 pulses. The presence of P3 pulses will always be detected since they will be at the same amplitude as the P1 pulses.

A differential pair, comprised of Q1 and Q2, provides a temperature compensated, level detector circuit for the pulses appearing on the collector of Q3.

By applying a bias voltage, to the emitter of Q3, the minimum detection level of the circuit may be controlled. R18 provides the Minimum Triggering Level (MTL) adjustment for the transponder. The bias voltage level is coupled to Q3 through CR2.

U1 contains the decoding circuitry for the input pulses so that only the proper interrogations generate a reply. U1 contains a decoder that is initiated upon receipt of a pulse when the system is in a reset condition. Three acceptance "windows" are then generated to determine the existence of subsequent pulses. The first "window" is to detect the presence of P2. If P2 occurs, the unit goes into an inactive state and times out through a suppression period. If P2 is not detected, the second "window" is activated.

The second "window" will allow the detection of a pulse delayed by about 8 usec from P1. If the pulse is detected, the reply circuits in the system are activated in the "A" mode. If the pulse is not detected a third "window" is generated.

The third "window" will allow the detection of a pulse at about 21 usec from P1. If a pulse is detected in this "window" the reply circuits will be activated in the "C" mode.

Since random pulses may initiate the system, a second decoder is included and will be activated as soon as the first decoder receives its first pulse. If either decoder receives a P2 pulse, the system will be suppressed. If either decoder receives a valid "A" or "C" interrogation, the other decoder is immediately suppressed so that only one interrogation may be received.

Once a valid interrogation is received, the selected output pulse train is generated using the inputs provided from the Front Panel switches for "A" mode and from the external altitude inputs for the "C" mode. U1 provides a reply output to U3 so that the reply rate may be measured and compared to the preset level from R25. If the preset level of reply rate is exceeded the detection level of Q3 will be increased so that only the stronger signals will be accepted.

If an Ident pulse is selected on the Front Panel, C8 and R20 will provide a timing period to activate the proper pulse. Q5 will turn on the "T" in the Front Panel display during the active period.

U2 in conjunction with Y1 forms the clock required for the timing of U1.

At any time that the transponder is in a reply mode, U1 will trigger Q6 to send an external suppression signal that can be used for DME suppression.

5.2 DIGITAL BOARD (Continued)

If the unit has a 40 pin VLSI U1 then there is a P_4 modification board attached to the digital board. The following circuit description will not apply to units with a 44 pin PLD U1.

5.2.1 P4 MODIFICATION BOARD

The voltage comparator, U1, monitors a Pin on U1 of the Digital Board. This pin will have a negative going spike when valid P_1, P_3 pulse is detected. R1 sets a reference level that determines the voltage at which the output of U1 will toggle and create a blanking pulse.

U2C and U2D are configured as invertors to add delay to this blanking pulse. The blanking pulse is then combined with the detected and processed video from the receiver in U2A. The resulting output has P_3 clipped in length and no detected pulses for 6 µseconds. This signal is inverted in U2B and then sent to U1 of the Digital Board as received data.

5.2.2. P4 MODIFICATION (ALTERNATIVE)

NOTE: This theory is used for TRT 250D units S/N 1306 and above.

Upon power up of the board, Q6 is turned on and kept on until a valid interrogation (detection of a valid P_3) is determined. By keeping Q6 on, this provides a low to the 2.7K Ω base resistor of Q4, and allows the detected video to pass. Upon receipt of a valid P_3 Q6 is shut off for approximately 29µ seconds. This removes the ground from the base resistor and allows the 15 volt pull up voltage to shut off Q4, thereby blanking the P_4 pulse.

5.3 MODULATOR/POWER SUPPLY

Use Schematic #9-1100-0101-04 and Component Locator #7050-1129-02 to aid in understanding the following circuit design.

The modulator is comprised of U5, Q15 and Q16. Q6 inverts and amplifies the reply pulses from the digital circuits. U5 is a dual, one-shot multivibrator. One section generates a long reply pulse to drive the reply indicator (T) on the front panel display and the second section provides the 0.45 usec pulses for the Transmitter. R21 is provided to allow precise transmitter pulse length adjustment.

Q5, Q9, Q15 and Q16 amplify the 0.45 usec pulses to drive the emitter of the transmitter oscillator and to drive the collector modulation transistor, Q8.

The Power Supply provides regulated output voltages of +5.00, +8.00, +15.00 and +48.00 VDC. To operate with voltage variations of 11 to 33 VDC, a switching regulator is used. The +15.00 volt supply has the most constant load and is therefore used in the main regulator feedback loop.

5.3 MODULATOR/POWER SUPPLY (Continued)

Diode CR6 sets the reference voltage for the power supply. Q2-Q4 provide a 9.0 VDC supply for the switching voltage regulator circuit. U1 provides a variable duty cycle drive signal for the switching transistor Q1. CR1 and CR2 provide peak to peak rectification of the signal appearing on the 22 turn winding of T1. The feedback loop through U2 compares the +15.0 VDC output with the reference voltage and adjusts the duty cycle of the drive signal generated in U1 to keep the peak to peak voltage on the transformer windings constant. The output applied to C9 therefore is held reasonably constant over the input voltage range. R13 allows adjustment of the +15 VDC supply.

CR3 and CR4 rectify the transformer output and provide approximately +55 VDC. Q10-Q12 in conjunction with R36 provide precise regulation of the transmitter voltage supply.

U3 and U4 are fixed, three terminal regulators used to supply +5.00 and +8.00 VDC.

Q14, CR12 and R38 work together to provide voltage spike protection while L1, C1, C2 and C3 provide filtering both in and out of the transponder. CR8 and R39 prevent reverse voltage damage to the unit.

5.4 TRANSMITTER

Use Schematic #9-1100-0007-02 and Assy Drawing #1900-1707-04 to aid in understanding the following circuit description.

The Transmitter consists of an oscillator stage and a Power Amplifier. The oscillator, Q1, is switched on both the collector and the emitter to eliminate parasitic oscillations. R1 provides a current limit for the transistor and stabilizes the operating point.

The oscillator frequency is determined by the cavity resonator connected to the base. Feedback to the base is adjusted by C3. The output signal is coupled from the oscillator collector to the input of the common base power amplifier Q2. The Transmitter and Receiver are coupled to a common antenna connector by approximately quarter-wave cables on their respective RF ports.

Use Schematic #9-1100-0091-04 and Component Locator #7050-0028-03 to aid in understanding the following circuit description.

5.5 MICROPROCESSOR/CONTROLLER

The microprocessor/controller assembly consists of the microprocessor, tuning encoder, the OFF/ON/ALT switch and the power supply for the display.

The microprocessor (U701) is located on the controller board assembly. The major functions of the microprocessor include the following:

1. Changing the standby code in response to tuning encoder input.
2. Maintaining the display which consists of 8 digits and one indicator letter.

5.5 MICROPROCESSOR/CONTROLLER (Controller)

3. Controlling reply code by setting logic levels on parallel BCD channeling lines.

A logic low on Pin 7 resets the microprocessor. A reset takes place whenever the voltage on Pin 7 goes from high(5V) to low(0V) and back. C703 and its connected pull up resistor in RP701 make up a filter for noise reduction during reset. Y701, C701, and C702 provide 4.19 MHz at Pins 8 and 9 for use as a time base by the microprocessor. Frequencies derived from the 4.19 MHz are used for the internal clock and timers. Whenever the microprocessor is reset (e.g. turned on) the active code is set to "1200" and the standby code to "0000".

By way of pull up resistors in RP701 and depending on knob position, the tuning encoder in SW701 puts either 0 or 5V on each of two lines A and B.

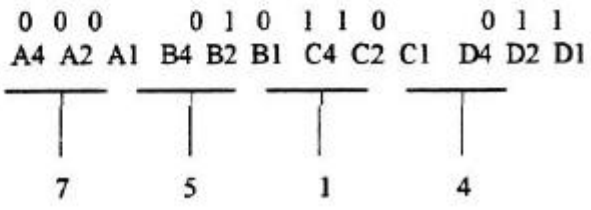
When the knob is turned, the voltage changes on each line at every other detent. When the knob is turned clockwise the voltages sequence such that A is high when B goes low and A is low when B goes high. This also means that B is high when A goes high and B is low when A goes low. The software uses this pattern to increment the standing code at each clockwise detent. Conversely, counterclockwise knob movement produces a pulse pattern exactly opposite of that above. This results in a decrement of the standby code at each counterclockwise detent.

The speed at which the tuning knob is turned determines how much the code is incremented or decremented at each detent. A software configured microprocessor timer measures the time between detents. If this time is greater than 150 mS, tuning is "slow" and standby code is incremented or decremented by 1 octal.

If this time is less than 150 mS, tuning is "fast" and standby code is incremented or decremented by 30 octal.

Incrementing a standby code of 7777 by 1 octal will cause a "rollover" to 0000. Likewise, decrementing a standby code 0000 by 1 octal will cause a rollover to 7777. Rollover also occurs in fast tune (e.g. 7777 to 0027).

Whenever the active code comes up or is changed, the microprocessor sets up a corresponding parallel BCD code (3 bits per digit) on Pins 45 to 56. Pull up resistors in RP702 are used to generate high or low outputs. The BCD code is complementary in that a "1" represents a "0" and vice-versa. For example the code for 7514 would be:



Circuitry on the Power Supply/Modulator board turns on Q701 when the transponder is not replying (not transmitting). This puts a low at Pin 44 of the microprocessor. When the unit istransmitting, Q701 is turned off and Pin 44 is at 5V through its connected pull up resistor in

5.5 MICROPROCESSOR/CONTROLLER (Controller)

RP701. This causes the microprocessor to illuminate the "T" in the display.

Applying a ground to the cathode of CR704 with SW702 applies A/C A+ to Pin 8 of U703 and to the main Power Supply/Modulator Assembly. U702 is powered by 8 VDC from the main power supply. U703 is used to produce a regulated 5V output (Pin 1) for U701 (Pin 58), to the display dimming circuit (R701), and to pull up resistors in RP701 and RP702. C711 is used to maintain voltage to U701 (Pins 7 and 58) when SW702 is between the "on" and "alt" positions to prevent a reset.

U702, a DC to DC converter chip is the heart of the high voltage power supply for the display. C704 is a timing capacitor that governs the frequency of an oscillator internal to the chip. C710, C705 and R705 form a low pass filter that reduces noise generated by the high voltage power supply on the 8V line. Current through R702 creates a sense voltage at Pin 7. When this voltage gets 330mV below Vcc, internal circuitry acts to reduce output current.

The output across the primary of T701 is a rectangular waveform whose duty cycle is controlled by a feedback loop as described below. R707 reduces noise in the system by reducing the Q of the primary. The secondary is coupled to two half-wave rectifiers (CR702/C706 and

CR703/C707) to produce both positive and negative DC voltage. The duty cycle of the transformer determines the magnitude of these voltages. The transformer runs at approximately 40KHz.

Feedback is generated from the positive DC voltage at the cathode of CR702. Because Pin 5 of U702 is the inverting input of an internal comparator with a 1.25V reference voltage, the voltage at the cathode of CR702 tends to fluctuate around 1.25V + V_z, where V_z is the zener voltage of CR701. V_z is nominally 91V. R703 provides a path for current through CR701 while R708 is used to provide an equal load current on the negative side. R704 is used to set the total drop across the +90V/-90V lines to 180V.

The feedback loop works as follows. When voltage at the cathode of CR702 gets above about 1.37V + V_z, the internal comparator in U702 produces a low output. This tends to reduce the duty cycle of the U702 output and thus brings down the magnitude of the +90V/-90V voltages. When the voltage at the cathode of CR702 drops below about 1.13V + V_z the comparator has a positive output which tends to increase the duty cycle and thus bring the voltage up. The total ripple across the -90V/+90V lines is approximately 0.24 Vp-p.

5.6 DISPLAY

Use Schematic #9-1100-0089-03, Component Locators #7050-0024-02, 7050-0025-02 and Display Schematic #9-1100-0107-02 to aid in understanding the following circuit description.

When the transfer (<->) switch is pressed it grounds Pin 25 of the microprocessor, which is normally at 5V through the connected pull up resistor in RP701. A temporary ground in Pin 25 causes two things to happen:

5.6 DISPLAY (continued)

1. Active and standby codes are swapped in the display
2. The microprocessor sets up the appropriate parallel BCD code to program the transponder reply code.

Pin 24 of the microprocessor is normally at 5V through its connected pull up resistor in RP701. Pushing the VFR switch puts a momentary ground on Pin 24.

The display is driven by two different signals, one for the anodes and one for the cathodes. +5V pulsed anode signals from the microprocessor (Pins 1-6 and 62-64) are applied to Pins 1-8 of U901 and the base of Q903. This results in +90V pulsed signals to corresponding anodes of the display by switching action of U901, Q901, and Q903. The software causes the anodes to be swept in the following sequence:
1,3,5,7,9,2,4,6,8,1,3... The period between beginning of each pulse at successive anodes is 1msec. The duration of each pulse is software controlled as discussed below.

Each segment (a,b,c,d, etc.) in the display has a cathode connected to a display pin as shown in Schematic #9-1100-0107-02. The microprocessor (Pins 11-17 and 61) sends +5V cathode pulses to Pins 1-7 of U801 and to the emitter of Q904. Through switching action, this results in -90V pulses at the cathodes.

The software controls the synchronization of anode and cathode pulses. For a segment, at a particular anode location, to be illuminated, it must receive a -90V cathode pulse the same time it receives a +90V anode pulse during an anode sweep. The software uses the tuning input to generate a particular display pattern.

Ambient light on the photo-resistor, LDR901, in the front panel determines display brightness. This photo-resistor varies from approximately 11K Ohm (strong light) to 1M causes the microprocessor to change the standby code to 1200.Ohm (dark) and forms a voltage divider circuit with R701. In strong light, voltage is minimized on Pin 31 of the microprocessor at around 0.8V. The software uses this information to maximize pulse width during an anode sweep and thus maximize display brightness. With decreasing light level, the voltage on Pin 31 increases up to a maximum of about 4.8V. As the voltage on Pin 31 increases, the pulse widths decreases and the display dims.