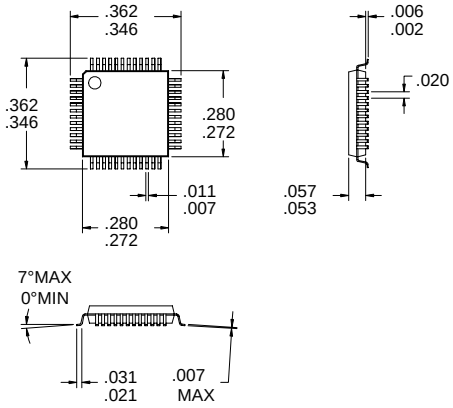
433/868/915MHZ FM/FSK/ASK/OOK TRANSCEIVER

Typical Applications

- Wireless Meter Reading
- Keyless Entry Systems
- 433/868/915MHz ISM Band Systems
- Wireless Data Transceiver
- Wireless Security Systems
- Battery Powered Portable Devices

Product Description

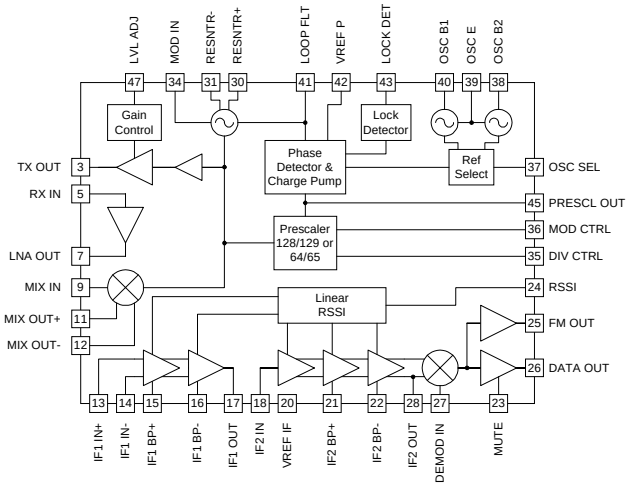
The RF2905 is a monolithic integrated circuit intended for use as a low cost FM transceiver. The device is provided in 48-lead plastic LQFP packaging and is designed to provide a fully functional FM transceiver. The chip is intended for linear (AM, FM) or digital (ASK, FSK, OOK) applications in the North American 915MHz ISM band and European 433MHz and 868MHz ISM bands. The integrated VCO, dual modulus/dual divide (128/129 or 64/65) prescaler, and reference oscillator require only the addition of an external crystal to provide a complete phase-locked oscillator.



Package Style: LQFP-48

Optimum Technology Matching® Applied

- [x] Si BJT
- [ ] GaAs HBT
- [ ] GaAs MESFET
- [ ] Si Bi-CMOS



Functional Block Diagram

Features

- Fully Monolithic Integrated Transceiver
- 2.7V to 5.0V Supply Voltage
- Narrow Band and Wide Band FM/FSK
- 300MHz to 1000MHz Frequency Range
- 10dB Cascaded Noise Figure
- 10mW Output Power at 433MHz

Ordering Information

RF2905	433/868/915MHz FM/FSK/ASK/OOK Transceiver
RF2905 PCBA-L	Fully Assembled Evaluation Board (433MHz)
RF2905 PCBA-M	Fully Assembled Evaluation Board (868MHz)
RF2905 PCBA-H	Fully Assembled Evaluation Board (915MHz)

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http://www.rfmd.com

Absolute Maximum Ratings

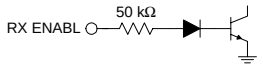
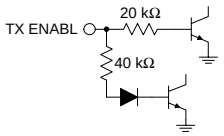
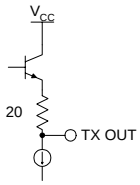
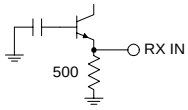
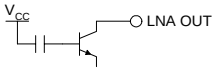
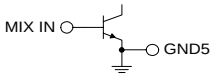
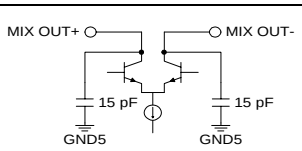
Parameter	Ratings	Unit
Supply Voltage	-0.5 to +5.5	V_{DC}
Control Voltages	-0.5 to +5.0	V_{DC}
Input RF Level	+10	dBm
Output Load VSWR	50:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

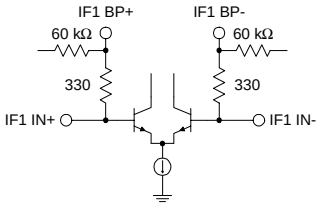
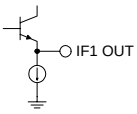
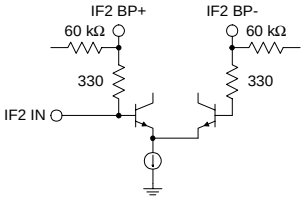
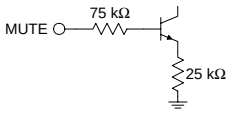
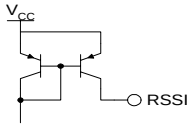
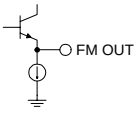
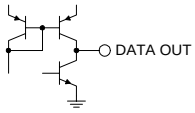
Caution! ESD sensitive device.

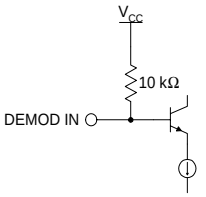
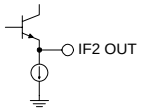
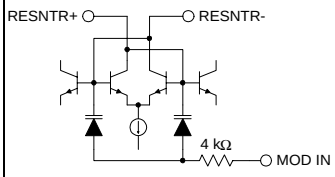
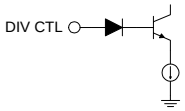
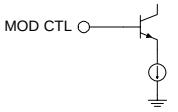
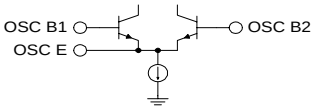
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.6V, Freq=433MHz
RF Frequency Range		300 to 1000		MHz	
VCO and PLL Section					
VCO Frequency Range		300 to 1000		MHz	
Prescaler divide ratio		64/65 or 128/129			
Prescaler Output Impedance		50		Ω	
PLL Lock Time		10		ms	The PLL lock time is set externally by the bandwidth of the loop filter
PLL Phase Noise		-80		dBc/Hz	Freq=915MHz, 10kHz Offset
		-100		dBc/Hz	Freq=915MHz, 100kHz Offset
Reference Frequency	TBD		17	MHz	
Crystal R_S		50	100	Ω	
Charge Pump Current	-40		+40	µA	
Transmit Section					
Max Modulation Frequency	2			MHz	
Min Modulation Frequency	Set by loop filter bandwidth				
Maximum Power Level	+7	+10		dBm	Freq=433MHz
		+3		dBm	Freq=915MHz
Power Control Range	12			dB	
Power Control Sensitivity		10		dB/V	
Max FM Deviation	200			kHz	Instanteneous frequency deviation is inversely proportional with the modulation voltage
Antenna Port Impedance		50		Ω	TX ENABL="1"
Antenna Port Impedance		TBD		Ω	TX ENABL="0"
Antenna Port VSWR			1.5:1		TX Mode
Modulation Input Impedance	4			kΩ	
Harmonics		-23		dBc	
Spurious				dBc	Compliant to Part 15.249 and I-ETS 300 220
Overall Receive Section					
Frequency Range		300 to 1000		MHz	
Cascaded Voltage Gain		35		dB	Freq=433MHz
		23		dB	Freq=915MHz
Cascaded Noise Figure		10		dB	
Cascaded Input IP_3		-31		dBm	Freq=433MHz
		-26		dBm	Freq=915MHz
RX Sensitivity		-101		dBm	IF BW=150kHz, Freq=433MHz, S/N=8dB
LO Leakage			-70	dBm	
RSSI DC Output Range		0.5 to 2.5		V	R_{LOAD}=51kΩ
RSSI Sensitivity		25		mV/dB	
RSSI Dynamic Range	70	80		dB	

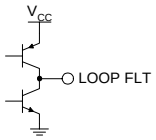
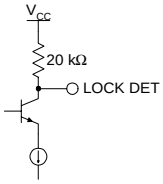
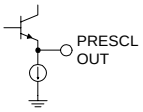
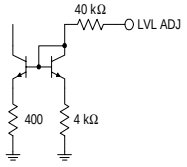
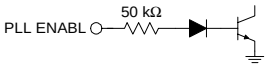
LNA					
Voltage Gain		23		dB	433MHz
		16		dB	915MHz
Noise Figure		4.8		dB	433MHz
		5.5		dB	915MHz
Input IP_3		-27		dBm	433MHz
		-20		dBm	915MHz
Input P_{1dB}		-37		dBm	433MHz
		-30		dBm	915MHz
Antenna Port Impedance		50		Ω	RX ENABL="1"
		TBD		Ω	RX ENABL="0"
Antenna Port VSWR			1.5:1		Freq=433MHz, RX Mode
Output Impedance		Open Collector		Ω	433MHz
		Open Collector		Ω	915MHz
Mixer					Single-ended configuration
Conversion Voltage Gain		8		dB	433MHz
		7		dB	915MHz
Noise Figure (SSB)		TBD		dB	433MHz
		17		dB	915MHz
Input IP_3		-21		dBm	433MHz
		-17		dBm	915MHz
Input P_{1dB}		-31		dBm	433MHz
		-28		dBm	915MHz
Maximum Output Voltage				V_{PP}	Balanced
First IF Section					
IF Frequency Range	0.1	10.7	25	MHz	
Voltage Gain		40		dB	IF=10.7MHz
Noise Figure		13		dB	
Input IP_3		TBD		mV_{PP}	
IF1 Input Impedance		330		Ω	
IF1 Output Impedance		330		Ω	
Second IF Section					
IF Frequency Range	0.1	10.7	25	MHz	
Voltage Gain		60		dB	IF=10.7MHz
IF2 Input Impedance		330		Ω	
IF2 Output Impedance		1		kΩ	At IF2 OUT- pin
Demod Input Impedance		10		kΩ	
FM Output Impedance		500		Ω	
Data Output Impedance		>1		MΩ	
FM Output Bandwidth	2			MHz	
Data Output Bandwidth	2			MHz	
Data Output Level	0.3		V_{CC}-0.3	V	Z_{LOAD}=1MΩ || 3pF; Output voltage is proportional with the instantaneous frequency deviation.
FM Output DC Level		2.6		V	Z_{LOAD}>10kΩ
FM Output AC Level		200		mV_{PP}	Z_{LOAD}>10kΩ

Power Down Control					
Logical Controls “ON”	2.0			V	Voltage supplied to the input
Logical Controls “OFF”			1.0	V	Voltage supplied to the input
Control Input Impedance	25k			Ω	
Turn On Time			4	ms	Reference Crystal=7.075MHz
Turn Off Time			4	ms	Dependent upon reference crystal. Higher
RX to TX and TX to RX Time			4	ms	frequencies reduce turn on/off times
Power Supply					
Voltage		3.6		V	Specifications
		2.7 to 5.0		V	Operating limits
Current Consumption		25		mA	TX Mode, LVL ADJ=3.6V
		10		mA	TX Mode, LVL ADJ=0V
		9		mA	RX Mode
			1	μA	Power Down Mode
		8		mA	PLL Only Mode

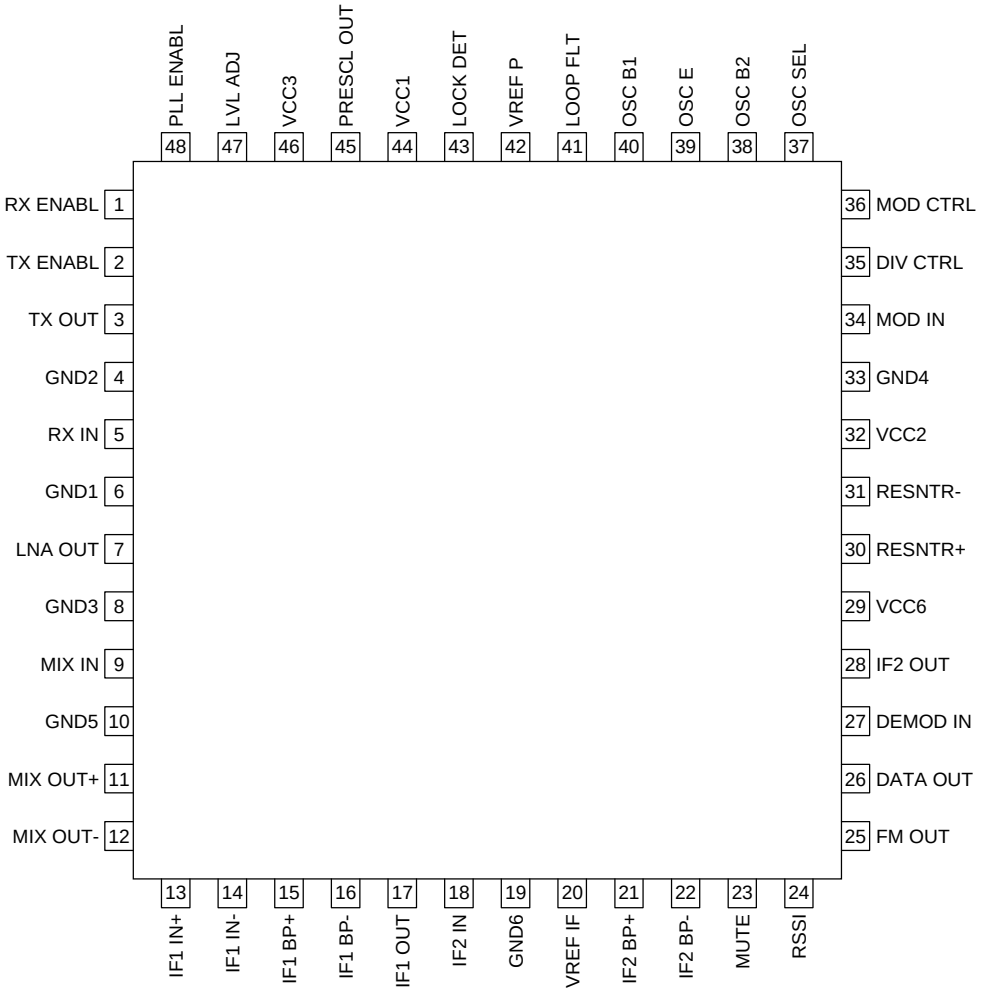
Pin	Function	Description	Interface Schematic
1	**RX ENABL**	Enable pin for the receiver circuits. RX ENABL>2.0V powers up all receiver functions. RX ENABL<1.0V turns off all receiver functions except the PLL functions and the RF mixer.	
2	**TX ENABL**	Enables the transmitter circuits. TX ENABL>2.0V powers up all transmitter functions. TX ENABL<1.0V turns off all transmitter functions except the PLL functions.	
3	**TX OUT**	RF output pin for the transmitter electronics. TX OUT output impedance is a low impedance (see output impedance plot in Figure TBD) when the transmitter is enabled. TX OUT is a high impedance when the transmitter is disabled.	
4	**GND2**	Ground connection for the 40 dB IF limiting amplifier and Tx PA functions. Keep traces physically short and connect immediately to ground plane for best performance.	
5	**RX IN**	RF input pin for the receiver electronics. RX IN input impedance is a low impedance (see input impedance plot in Figure TBD) when the transmitter is enabled. RX IN is a high impedance when the receiver is disabled.	
6	**GND1**	Ground connection for RF receiver functions. Keep traces physically short and connect immediately to ground plane for best performance.	
7	**LNA OUT**	Output pin for the receiver RF low noise amplifier. This pin is an open collector output and requires an external pull up coil to provide bias and tune the LNA output. A capacitor in series with this output can be used to match the LNA to 50Ω impedance image filters.	
8	**GND3**	Same as pin 4.	
9	**MIX IN**	RF input to the RF Mixer. An LC matching network between LNA OUT and MIX IN can be used to connect the LNA output to the RF mixer input in applications where an image filter is not needed or desired.	
10	**GND5**	GND5 is the ground connection shared by the input stage of the transmit power amplifier and the receiver RF mixer.	
11	**MIX OUT+**	Complementary (with respect to pin 12) IF output from the RF mixer. Interfaces directly to 10.7MHz ceramic IF filters as shown in the application schematic. A pull-up inductor and series matching capacitor should be used to present a 330Ω termination impedance to the ceramic filter. Alternately, an IF tank can be used to tailor the IF frequency and bandwidth to meet the needs of a given application.	
12	**MIX OUT-**	IF output from the RF mixer. For a balanced mixer output, pull-up inductors from pin 11 and 12 to V_{CC} and a capacitor between the pins should be used. The sum of the total pull-up inductance should be used to resonate the capacitor between pins 11 and 12. DC blocking capacitors of 10nF can then be used to connect the balanced output to IF1 IN+ (pin 13) and IF1 IN- (pin 14).	See pin 11.

13	IF1 IN+	Balanced IF input to the 40dB limiting amplifier strip. A 10nF DC blocking capacitor is required on this input.	
14	IF1 IN-	Functionally the same as pin 13 except inverting node amplifier input. In single-ended applications, this input should be bypassed directly to ground through a 10nF capacitor.	See pin 13.
15	IF1 BP+	DC feedback node for the 40dB limiting amplifier strip. A 10nF bypass capacitor from this pin to ground is required.	See pin 13.
16	IF1 BP-	Same as pin 15.	See pin 13.
17	IF1 OUT	IF output from the 40dB limiting amplifier. The IF1 OUT output presents a nominal 330 Ω output resistance and interfaces directly to 10.7MHz ceramic filters.	
18	IF2 IN	Balanced IF input to the 60dB limiting amplifier strip. A 10nF DC blocking capacitor is required on this input. The IF2 IN input presents a nominal 330 Ω input resistance and interfaces directly to 10.7MHz ceramic filters.	
19	GND6	Ground connection for 60dB IF limiting amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
20	VREF IF	DC voltage reference for the IF limiting amplifiers. A 10nF capacitor from this pin to ground is required.	
21	IF2 BP+	DC feedback node for the 60dB limiting amplifier strip. A 10nF bypass capacitor from this pin to ground is required.	See pin 18.
22	IF2 BP-	Same as pin 21.	See pin 18.
23	MUTE	This pin is used to mute the data output (DATA OUT). MUTE>2.0V turns the DATA OUT signal on. MUTE<1.0V turns the DATA OUT signal off. The MUTE signal should be logic low in the Sleep Mode.	
24	RSSI	A DC voltage proportional to the received signal strength is output from this pin. The output voltage range is 0.5V to 2.5V and increases with increasing signal strength.	
25	FM OUT	Linear output from the FM demodulator. This pin is used in analog applications when signal fidelity is important.	
26	DATA OUT	Demodulated data output from the demodulator. Output levels on this are TTL/CMOS compatible. The magnitude of the load impedance is intended to be 1MΩ or greater. When using a RF2905 transmitter and receiver back to back a data inversion will occur.	

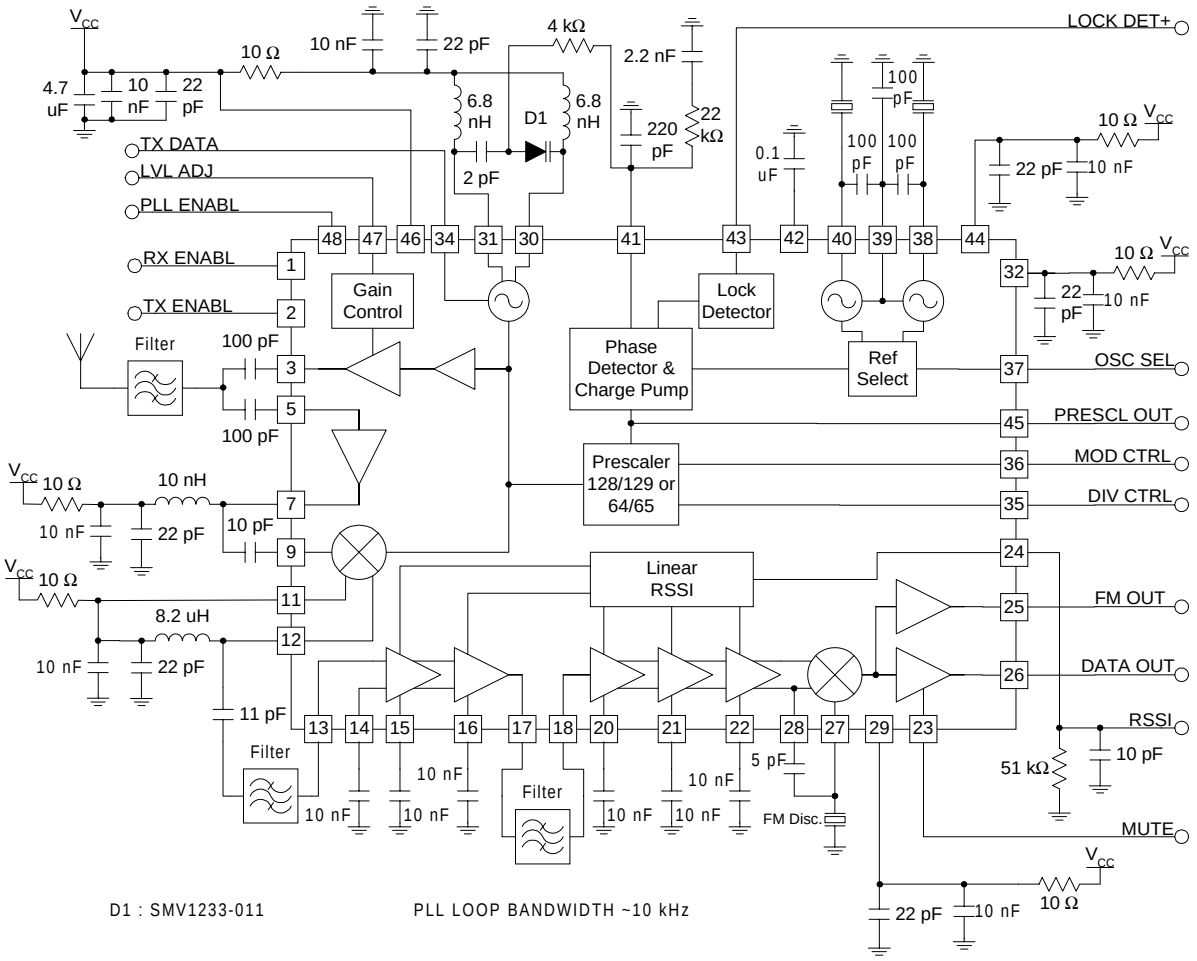
27	**DEMOD IN**	This pin is the input to the FM demodulator. This pin is NOT AC coupled. Therefore, a DC blocking capacitor is required on this pin to avoid shorting the demodulator input with the LC tank. A ceramic discriminator or DC blocked LC tank resonant at the IF should be connected to this pin.	
28	**IF2 OUT**	Balanced IF output from the 60dB limiting amplifier strip. This pin is intended to be connected to pin 27 through a 5pF capacitor and an FM discriminator circuit.	
29	**VCC6**	This pin is used is supply DC bias to the 60dB IF limiting amplifier. An IF bypass capacitor should be connected directly to this pin and returned to ground. A 10nF capacitor is recommended for 10.7MHz IF applications.	
30	**RESNTR+**	This port is used to supply DC voltage to the VCO as well as to tune the center frequency of the VCO. Equal value inductors should be connected to this pin and pin 31 although a small imbalance can be used to tune in the proper frequency range.	
31	**RESNTR-**	See RESNTR+ description.	See pin 30.
32	**VCC2**	This pin is used is supply DC bias to the VCO, prescaler, and PLL. An IF bypass capacitor should be connected directly to this pin and returned to ground. A 10nF capacitor is recommended for 10.7MHz IF applications.	
33	**GND4**	GND4 is the ground shared on chip by the VCO, prescaler, and PLL electronics.	
34	**MOD IN**	FM analog or digital modulation can be imparted to the VCO through this pin. The VCO varies in accordance to the voltage level presented to this pin. To set the deviation to a desired level, a voltage divider referenced to Vcc is the recommended. This deviation is also dependent upon the overall capacitance of the external resonant circuit.	See pin 30.
35	**DIV CTRL**	This pin is used to select the desired prescaler divisor. A logic high (DIV CTRL>2.0V) selects the 64/65 divisor. A logic low (DIV CTRL<1.0V) selects the 128/129 divisor.	
36	**MOD CTRL**	This pin is used to select the prescaler modulus. A logic high (MOD CTRL>2.0V) selects 64 or 128 for the prescaler divisor. A logic low (MOD CTRL<1.0V) selects 65 or 129 for the prescaler divisor.	
37	**OSC SEL**	A logic high (OSC SEL>2.0V) applied to this pin powers on reference oscillator 2 and powers down reference oscillator 1. A logic low (OSC SEL<1.0V) applied to this pin powers on reference oscillator 1 and powers down reference oscillator 2.	
38	**OSC B2**	This pin is connected directly to the reference oscillator 2 transistor base. The intended reference oscillator configuration is a modified Colpitts. A 100pF capacitor should be connected between pin 38 and pin 39.	
39	**OSC E**	This pin is connected directly to the emitter of the reference oscillator transistors. A 100pF capacitor should be connected from this pin to ground.	See pin 38.

40	**OSC B1**	This pin is connected directly to the reference oscillator 1 transistor base. The intended reference oscillator configuration is a modified Colpitts. A 100pF capacitor should be connected between pin 39 and pin 40.	See pin 38.
41	**LOOP FLT**	Output of the charge pump, and input to the VCO control. An RC network from this pin to ground is used to establish the PLL bandwidth.	
42	**VREF P**	Bypass pin for the prescaler reference voltage. A 33nF capacitor to ground is needed to supress reference spurs in the device. This value may be different for different PCB arangements.	
43	**LOCK DET**	This pin provides an analog output indicating the lock status of the PLL. The amplitude of this signal is typically 200mV$_{PP}$ around a DC level of V_{CC}-0.1V.	
44	**VCC1**	This pin is used to supply DC bias to the receiver RF electronics. A RF bypass capacitor should be connected directly to this pin and returned to ground. A 100pF capacitor is recommended for 915MHz applications. A 220pF capacitor is recommended for 433MHz applications.	
45	**PRESCL OUT**	Dual-modulus/Dual-divide prescaler output. The output can be interfaced to an external PLL IC for additional flexibility in frequency programming.	
46	**VCC3**	This pin is used to supply DC bias to the transmitter PA. A RF bypass capacitor should be connected directly to this pin and returned to ground. A 100pF capacitor is recommended for 915MHz applications. A 220pF capacitor is recommended for 433MHz applications.	
47	**LVL ADJ**	This pin is used to vary the transmitter output power. An output level adjustment range greater than 12dB is provided through analog voltage control of this pin. DC current of the transmitter power amp ia also reduced with output power. This pin MUST be low when the transmitter is disabled.	
48	**PLL ENABL**	This pin is used to power up or down the VCO and PLL. A logic high (PLL ENABL>2.0V) powers up the VCO and PLL electronics. A logic low (PLL ENABL<1.0V) powers down the PLL and VCO.	

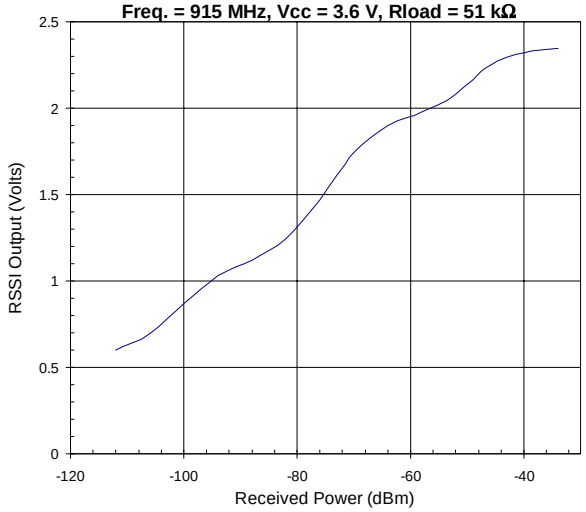
Pin Out


PLL ENABL 48
LVL ADJ 47
VCC3 46
PRESCL OUT 45
VCC1 44
LOCK DET 43
VREF P 42
LOOP FLT 41
OSC B1 40
OSC E 39
OSC B2 38
OSC SEL 37
RX ENABL 1
TX ENABL 2
TX OUT 3
GND2 4
RX IN 5
GND1 6
LNA OUT 7
GND3 8
MIX IN 9
GND5 10
MIX OUT+ 11
MIX OUT- 12
36 MOD CTRL
35 DIV CTRL
34 MOD IN
33 GND4
32 VCC2
31 RESNTR-
30 RESNTR+
29 VCC6
28 IF2 OUT
27 DEMOD IN
26 DATA OUT
25 FM OUT
13 IF1 IN+
14 IF1 IN-
15 IF1 BP+
16 IF1 BP-
17 IF1 OUT
18 IF2 IN
19 GND6
20 VREF IF
21 IF2 BP+
22 IF2 BP-
23 MUTE
24 RSSI

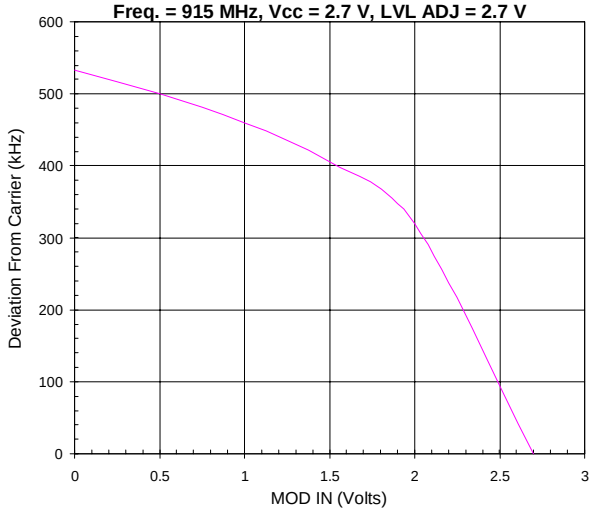
915 MHz Application Schematic



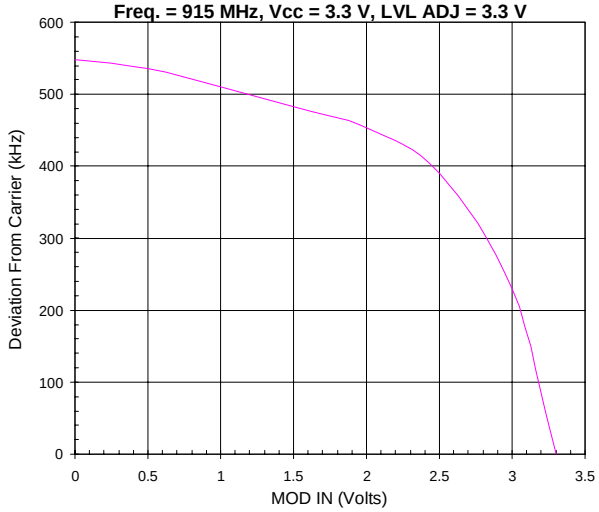
RSSI ,
Freq. = 915 MHz, Vcc = 3.6 V, Rload = 51 kΩ



Modulation Deviation,
Freq. = 915 MHz, Vcc = 2.7 V, LVL ADJ = 2.7 V



Modulation Deviation,
Freq. = 915 MHz, Vcc = 3.3 V, LVL ADJ = 3.3 V



Modulation Deviation,
Freq. = 915 MHz, Vcc = 5.0 V, LVL ADJ = 5.0 V