DB2068C Radio Module

operational description

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1.0 Purpose

The purpose of this document is to provide the necessary information to describe the operational theory.

2.0 Scope

This document will provide a top level description of the DB2068C Radio Module.

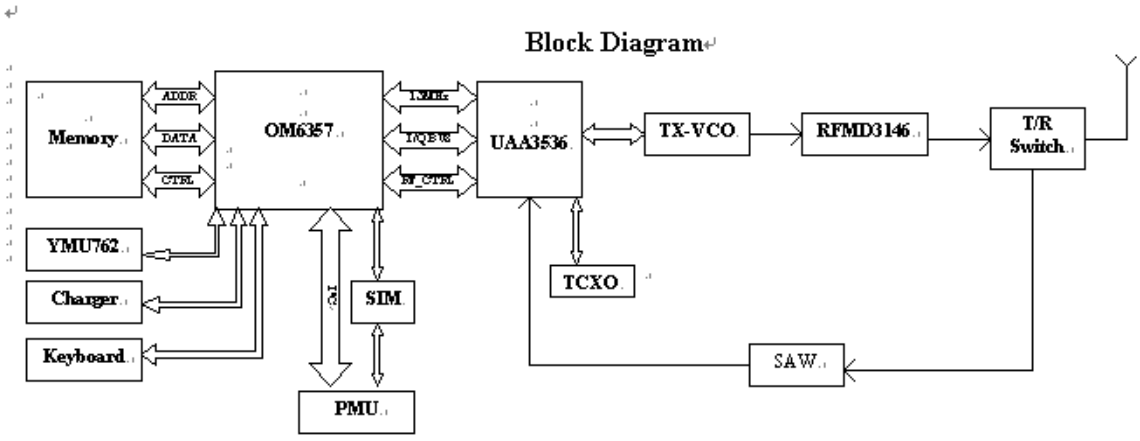
3.0 Related Documents

There are a number of related documents which are helpful when using this manual. They include the following.
a) DB2068C User's Manual
b) DB2068C Transceiver Data Sheet
c) GSM System Specification.
d) DB2068C Radio Circuitry Description

The DB2068C User's Manual provides the necessary information to operate a mobile. DB2068C Traceiver Data Sheet provides some information for the RF part. The DB2068C Radio Circuitry Description .Circuitry Description provides information on the circuits relevant to FCC certification.

4.0 Overview

The attached picture is DB2068C BLOCK diagram.



4.1DB2068C Radio Module Circuit Architecture

The circuit can be powered-up into four different modes, RX, TX, SYN or REF mode, depending on supply voltages applied, the logical level at pins RXON/TXON/SYNON and the 3-wire bus serial programming. In RX (TX) mode, all sections required for receive (transmit) are turned on. The SYN mode is used to power-up the synthesiser and the RF VCO prior to the RX or TX mode. In the SYN mode, some internal LO buffers are also powered-up such that VCO pulling is minimized when switching on the receiver

or the transmitter. The reference oscillator (REF mode) is turned on by applying the supply voltage. Additionally band selection is done using the 3-wire bus serial programming allowing the proper enabling of the LNAs and TX charge-pump current programming.

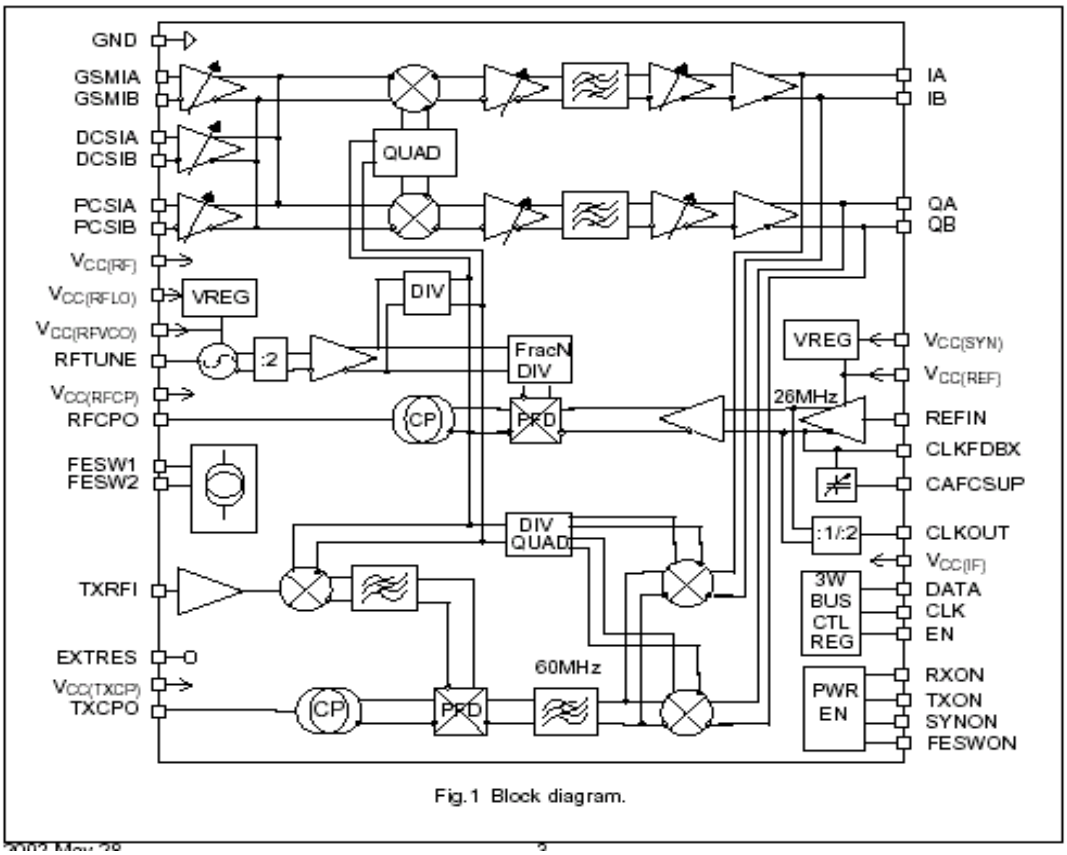


Fig.1 Block diagram.

5.0 FUNCTIONAL DESCRIPTION

RF Receiver

The receiver front-end converts the aerial RF signal from GSM850 (869-894 MHz), GSM900 (925 - 960 MHz), DCS(1805 - 1880 MHz) or PCS (1930 - 1990 MHz) bands down to a low intermediate frequency (IF) of 100 kHz. The first stages are symmetrical low noise amplifiers (LNAs). They are matched to 50 W using external baluns. The DCS inpurs can also be used for PCS operation. The LNAs are followed by an I, Qdown-mixer. It consists of two mixers in parallel but driven by quadrature out of phase LO signals. The In phase (I) and Quadrature phase (Q) IF signals are low pass filtered to provide protection from high frequency offset interferers. The low IF I and Q signals are then fed into the channel filter.

Channel filter and AGC

The front-end low IF I and Q outputs enter the integrated bandpass channel filter with provision for five 8 dB gain steps in front of the filter. The filter is a self-calibrated fifth order band-pass filter centred around 100 kHz and has a bandwidth of 240 kHz for GSM

mode, 300kHz for EDGE mode. Being filtered the low IF I and Q are further amplified with provision for ten 4 dB gain steps and fully integrated DC offset compensation. Realised with an active high pass circuit this compensation either operates continuously or keeps the acquired offset correction during the bursts depending on the programming. The low IF output buffer provides close to rail-to-rail output signals.

IQ modulator
I and Q baseband signals are applied to the IQ modulator that shifts the modulation spectrum up to the transmit IF. It is designed for low harmonic distortion, low carrier leakage and high image rejection to keep the phase error as small as possible. The modulator is loaded at its IF output by an integrated low pass filter that supress unwanted spurs prior to get into the phase detector. The clock drive is generated by division of the RFLO signal provided for the transmit offset mixer.

Transmit modulation loop
The analog transmit modulation loop is composed by an on-chip offset mixer with spur filter and by a phase/frequency detector with charge pump. The loop is closed off-chip by a loop filter and transmit VCO. The analog PLL copies the modulation to the off-chip transmit VCO and acts as a tracking filter. A PLL of at least third order is required to meet noise requirements at 20 MHz offset from carrier. The PLL bandwidth must be greater than 700 kHz in order to keep a low dynamic phase error and to minimize the acquisition time. The IF frequencies used are about 60 MHz.

RF VCO
The RF VCO is fully integrated and self calibrating on manufacturing tolerances. It consists of 64 different frequency ranges that are selected internally depending on the frequency programming. It covers the necessary bandwidth of 3476 to 3980MHz and is tuned via the RF charge pump and the external loop filter. An internal supply voltage regulator using VCC(RFLO) as input supplies the RF VCO and minimises parasitic couplings and pushing. This regulator and the RF VCO are turned on by the SYNON signal. The 64 different frequency ranges are realised by switching of varactors' cathodes between GND and the regulated RFVCO supply.

RF LO section
The RF LO section covering the 3476 to 3980 MHz bandwidth is driven by the internal RF VCO module. It includes the LO buffering for the RF PLL, a divider by two or one for GSM850/GSM900 and DCS/PCS respectively which drives a quadrature generation network to supply the RX IQ down-mixer or it drives the transmit modulation loop offset mixer and the clock divider driving the IQ modulator.Philips Semiconductors Objective specification Low power GSM850/GSM900/DCS/PCS multi-band transceiver UAA3536HN/C2