Collex Communication Corp.

COLLEX COMMUNICATION CORP.

Product Datasheet

CUSTOMER	
DESCRIPTION	**Bluetooth Stereo module**
MODEL	**HSM3.0**

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INTRODUCTION

Bluetooth wireless technology is a 2.4GHz ISM-band open industry standard for short range wireless communication, which is capable of voice and data transfer.

The Collex HSM 3.0-Bluetooth Module is a perfect solution for enhanced audio applications, such as stereo headphones and high performance telephony headsets. It can be connected with any Bluetooth devices in an operating range of ten meters. It is slim and light so the designers can have better flexibilities for the product shapes.

Moreover, HSM 3.0 is an external version Bluetooth module. With our latest software built-in, the Collex HSM 3.0 has the best compatibility with Bluetooth devices in the market and it is fully compliant with the Bluetooth version 2.0 specification.

The detail information of Collex HSM 3.0-Bluetooth Module is presented in this document below. For latest information, please visit our web site Http://www.collex.com.tw.

FEATURE

- Small and easy to integrate.
- Support of enhanced audio applications.
- Range up to ten meters cable free connection with Bluetooth devices.
- No radio signal interference.
- High quality stereo audio (sample rate up to 44.1kHz most)
- Built-in Software DSP (cVc)
- Fully Bluetooth v2.0 Specification Compliant
- Support Handsfree, Headset, A2DP, AVRCP Profiles.
- Fully qualified Bluetooth RF requirement.

FUNCTIONS

- Call accept/Reject/Terminate/audio transfer
- Caller ID, Caller Name
- Retrieve phonebook from Bluetooth mobile phones
- Retrieve SMS from Bluetooth mobile phones
- Real-time phonebook/SMS query
- New SMS notify
- Call waiting/Three-way call
- Control iPOD functions through Bluetooth connection
  i.e. Pause/Play/Next/Previous/Fordward/Backward
- Can customize PIN code and device name
- Can pair up to 8 Bluetooth Devices

SPECIFICATION

- Humidity 10% ~ 90%
- Storage Temperature -40 ~ 150°C
- Operating Temperature -30 ~ 85°C
- Power Consumption 50mA(playing);1mA(standby);40mA(talking)
- Output Power 0 dBm (Class II)
- Frequency Band 2.4GHz~2.4835GHz ISM Band
- Range 10 meters (free space)
- Standard Bluetooth 2.0 specification

Electrical Characteristics

CSR BloeCore3-Multimedia External:

Absolute Maximum Ratings		
Rating	**Minimum**	**Maximum**
Storage Temperature	-40°C	+150°C
Supply Voltage: VDD_RADIO, VDD_LO, VDD_ANA and VDD_CORE	-0.4V	2.2V
Supply Voltage: VDD_MEM, VDD_PADS, VDD_PIO and VDD_USB	-0.4V	3.7V
Supply Voltage: VREG_IN	-0.4V	5.6V
Other Terminal Voltages	VSS-0.4V	VDD+0.4V

Recommended Operating Conditions		
Operating Condition	**Minimum**	**Maximum**
Operating Temperature Range	-40°C	+105°C
Guaranteed RF performance range (1)	-25°C	+85°C
Supply Voltage: VDD_RADIO, VDD_LO, VDD_ANA and VDD_CORE	1.7V	1.9V
Supply Voltage: VDD_MEM, VDD_PADS, VDD_PIO and VDD_USB	1.7V	3.6V
Supply Voltage: VREG_IN	2.2V	4.2V(2)

Notes:

(1) Typical figures are given for RF performance between -40°C and +105°C.

(2) The device will operate without damage with VREG_IN as high as 5.6V, however the RF performance is not guaranteed above 4.2V.

Input/Output Terminal Characteristics				
Linear Regulator	**Minimum**	**Typical**	**Maximum**	**Unit**
Normal Operation				
Output Voltage (Iload = 70 mA)	1.70	1.78	1.85	V
Temperature Coefficient	-250	-	+250	ppm/°C
Output Noise[1][2]	-	-	1	mV rms
Load Regulation (Iload < 100 mA)	-	-	50	mV/A
Settling Time[1][3]	-	-	50	µs
Maximum Output Current	140	-	-	mA
Minimum Load Current	5	-	-	µA
Input Voltage	-	-	4.2[6]	V
Dropout Voltage (Iload = 70 mA)	-	-	350	mV
Quiescent Current (excluding load, Iload < 1mA)	25	35	50	µA
Low Power Mode[4]				
Quiescent Current (excluding load, Iload < 100µA)	4	7	10	µA
Disabled Mode[5]				
Quiescent Current	1.5	2.5	3.5	µA

Notes:

For optimum performance the VDD_ANA ball adjacent to VREG_IN should be used for regulator ouput.

(1) Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors.

(2) Frequency range 100Hz to 100kHz.

(3) 1mA to 70mA pulsed load.

(4) Low power mode is entered and exited automatically when the chip enters/leaves Deep Sleep mode.

(5) Regulator is disabled when VREG_EN is pulled low. It can also be disabled when VREG_IN is either open circuit or driven to the same voltage as VDD_ANA.

(6) Operation up to 5.6V is permissible without damage and without the output voltage rising sufficiently to damage the rest of BlueCore3, but output regulation and other specifications are no longer guaranteed at input voltages in excess of 4.2V.

Input/Output Terminal Characteristics (Continued)					
Digital Terminals		**Minimum**	**Typical**	**Maximum**	**Unit**
Input Voltage Levels					
V_{IL} input logic level low	2.7V ≤ VDD ≤ 3.0V	-0.4	-	+0.8	V
	1.7V ≤ VDD ≤ 1.9V	-0.4	-	+0.4	V
V_{IH} input logic level high		0.7VDD	-	VDD+0.4	V
Output Voltage Levels					
V_{OL} output logic level low, (I_o = 4.0mA), 2.7V ≤ VDD ≤ 3.0V		-	-	0.2	V
V_{OL} output logic level low, (I_o = 4.0mA), 1.7V ≤ VDD ≤ 1.9V		-	-	0.4	V
V_{OH} output logic level high, (I_o = -4.0mA), 2.7V ≤ VDD ≤ 3.0V		VDD-0.2	-	-	V
V_{OH} output logic level high, (I_o = -4.0mA), 1.7V ≤ VDD ≤ 1.9V		VDD-0.4	-	-	V
Input and Tri-state Current with:					
Strong pull-up		-100	-40	-10	µA
Strong pull-down		+10	+40	+100	µA
Weak pull-up		-5.0	-1.0	-0.2	µA
Weak pull-down		+0.2	+1.0	+5.0	µA
I/O pad leakage current		-1	0	+1	µA
C_I Input Capacitance		1.0	-	5.0	pF

Input/Output Terminal Characteristics (Continued)					
Auxiliary ADC		**Minimum**	**Typical**	**Maximum**	**Unit**
Resolution		-	-	8	Bits
Input voltage range (LSB size = VDD_ANA/255)		0	-	VDD_ANA	V
Accuracy	INL	-1	-	1	LSB
(Guaranteed monotonic)	DNL	0	-	1	LSB
Offset		-1	-	1	LSB
Gain Error		-0.8	-	0.8	%
Input Bandwidth		-	100	-	kHz
Conversion time		-	2.5	-	µs
Sample rate[2]		-	-	700	Samples/s

Input/Output Terminal Characteristics (Continued)				
Auxiliary DAC	**Minimum**	**Typical**	**Maximum**	**Unit**
Resolution	-	-	8	Bits
Average output step size[3]	12.5	14.5	17.0	mV
Output Voltage		monotonic[3]		
Voltage range (I_O=0mA)	VSS_PADS	-	VDD_PIO	V
Current range	-10.0	-	+0.1	mA
Minimum output voltage (I_O=100mA)	0.0	-	0.2	V
Maximum output voltage (I_O=10mA)	VDD_PIO-0.3	-	VDD_PIO	V
High Impedance leakage current	-1	-	+1	µA
Offset	-220	-	+120	mV
Integral non-linearity[3]	-2	-	+2	LSB
Settling time (50pF load)	-	-	10	µs

Input/Output Terminal Characteristics (Continued)				
Stereo Audio CODEC	**Minimum**	**Typical**	**Maximum**	**Unit**
Input Stage/Microphone Amplifier				
Input full scale at maximum gain	-	4	-	mV rms
Input full scale at minimum gain	-	400	-	mV rms
Gain resolution	-	3	-	dB
Distortion at 1kHz	-		-74	dB
Input referenced rms noise in 15kHz bandwidth	-	8	-	µV rms
3dB Bandwidth	-	17	-	kHz
Input impedance	-	20	-	kΩ
THD+N (microphone input) @ 30mV rms input	-	-66	-	dB
Analogue to Digital Converter				
Resolution	-	-	16	bits
Input sample rate	8	-	44.1	kHz
Signal / (Noise + Distortion), 0 - F_{sample} /2, with full scale 1kHz tone				
F_{sample} = 8kHz	-	84	-	dB
F_{sample} = 11.025kHz	-	83	-	dB
F_{sample} = 16kHz	-	84	-	dB
F_{sample} = 22.050kHz	-	83	-	dB
F_{sample} = 32kHz	-	80	-	dB
F_{sample} = 44.1kHz	-	74	-	dB
Digital Gain	-24		21.5	dB
Digital to Analogue Converter				
Resolution	-	-	16	bits
Output sample rate	8	-	48	kHz
Gain Resolution	-	3	-	dB
Signal / (Noise + Distortion), 0 – 20 kHz, with full scale 1kHz tone				
F_{sample} = 8kHz	-	79	-	dB
F_{sample} = 11.025kHz	-	78	-	dB
F_{sample} = 16kHz	-	79	-	dB
F_{sample} = 22.050kHz	-	88	-	dB
F_{sample} = 32kHz	-	90	-	dB
F_{sample} = 44.1kHz	-	90	-	dB
F_{sample} = 48kHz	-	89	-	dB
Digital Gain	-24	-	21.5	dB

Input/Output Terminal Characteristics (Continued)				
Output Stage/Loudspeaker Driver	**Minimum**	**Typical**	**Maximum**	**Unit**
Output power into 32Ω	-	30	-	mW pk
Output voltage full scale swing	-	2.0	-	V pk-pk
Output current drive (at full scale swing)[9]	10	20	40	mA
Output full scale current (at reduced swing)[9]	-	75	-	mA
Distortion and noise (relative to full scale), THD	-	-75	-	dBc
Allowed Load: resistive	16	-	O.C.	Ω
Allowed Load: capacitive	-	-	500	pF

Notes:

VDD_CORE, VDD_RADIO, VDD_LO and VDD_ANA are at 1.8V unless shown otherwise.

VDD_PADS, VDD_PIO and VDD_USB are at 3.0V unless shown otherwise.

The same setting of the digital trim is applied to both XTAL_IN and XTAL_OUT.

Current drawn into a pin is defined as positive, current supplied out of a pin is defined as negative.

(1) Internal USB pull-up disabled.

(2) Access of ADC is through VM function and therefore sample rate given is achieved as part of this function.

(3) Specified for an output voltage between 0.2V and VDD_PIO -0.2V.

(4) Integer multiple of 250kHz.

(5) The difference between the internal capacitance at minimum and maximum settings of the internal digital trim.

(6) XTAL frequency = 16MHz; XTAL C0 = 0.75pF; XTAL load capacitance = 8.5pF.

(7) Clock input can be any frequency between 8 and 40MHz in steps of 250kHz plus CDMA/3G TCXO frequencies of 7.68, 14.44, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz.

(8) Clock input can either be sinusoidal or square wave. If the peaks of the signal are below VSS_ANA or above VDD_ANA a DC blocking capacitor is required between the signal and XTAL_IN.

(9) For specified THD. Much greater current can be supplied by the loudspeaker driver with compromised THD.

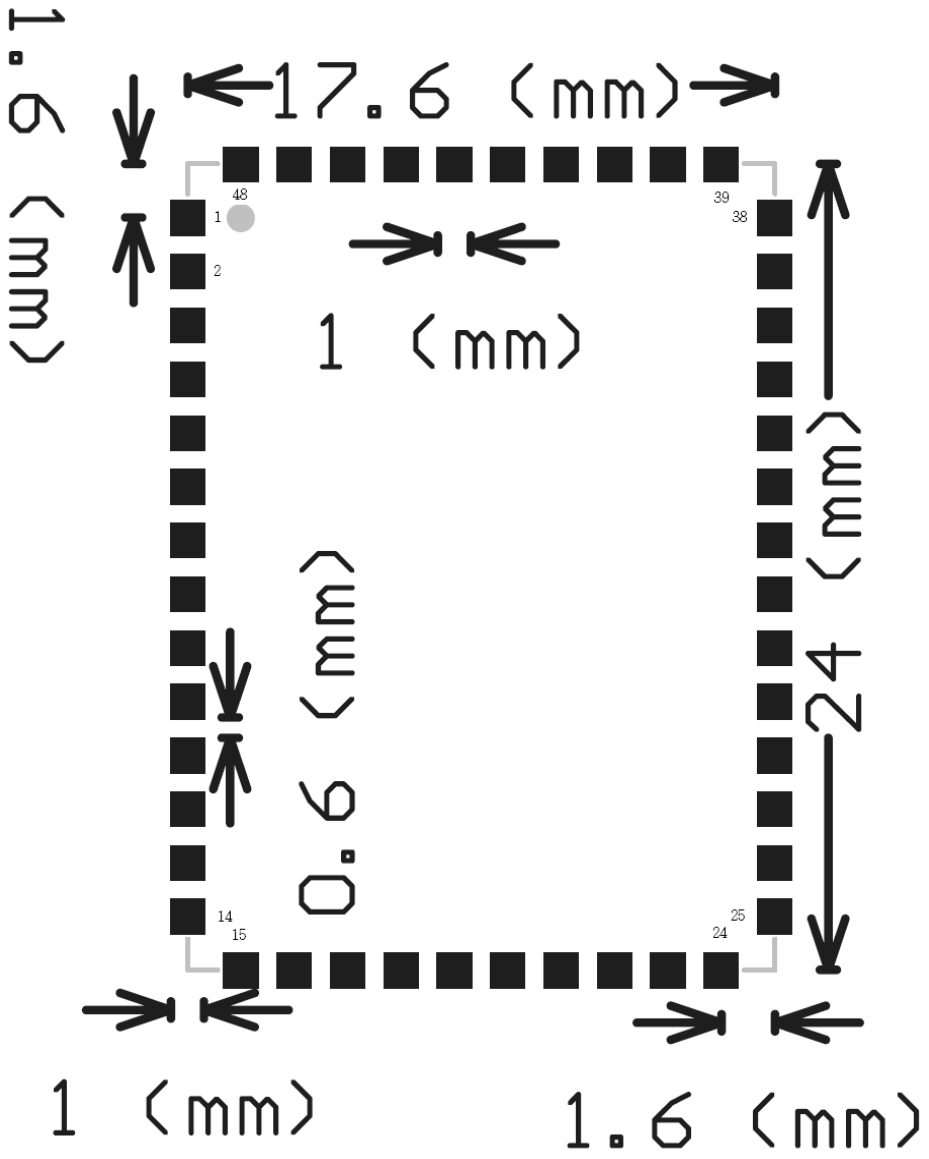
Power Consumption

Typical Average Current Consumption		
VDD=1.8V Temperature = +20°C Output Power = +4dBm		
Mode	**Average**	**Unit**
SCO connection HV3 (30ms interval Sniff Mode) (Slave)	21	mA
SCO connection HV3 (30ms interval Sniff Mode) (Master)	21	mA
SCO connection HV3 (No Sniff Mode) (Slave)	28	mA
SCO connection HV1 (Slave)	42	mA
SCO connection HV1 (Master)	42	mA
ACL data transfer 115.2kbps UART no traffic (Master)	5	mA
ACL data transfer 115.2kbps UART no traffic (Slave)	22	mA
ACL data transfer 720kbps UART (Master or Slave)	45	mA
ACL data transfer 720kbps USB (Master or Slave)	45	mA
ACL connection, Sniff Mode 40ms interval, 38.4kbps UART	3.2	mA
ACL connection, Sniff Mode 1.28s interval, 38.4kbps UART	0.45	mA
Parked Slave, 1.28s beacon interval, 38.4kbps UART	0.55	mA
Standby Mode (Connected to host, no RF activity)	47.0	µA
Reset (RESET high or RESETB low)	15.0	µA
DSP		
DSP core (including PM memory access)		
Minimum (NOP)	0.25	mA/MIPS
Maximum (MAC)	0.65	mA/MIPS
DSP memory access (DM1 or DM2)	0.15	mA/MIPS
CODEC		
Microphone inputs and ADC / channel	0.85	mA
DAC and loudspeaker driver, no signal / channel[1]	1.4	mA
Digital audio processing subsystem	8	mA

Note:

(1) Power consumption increase is >5% for maximum signal.

Recommended land pattern



Pin Definition

PIO #.	Name	Pad type	Description
1	MIC_L_P	analogue	microphone input positive(left side)
2	MIC_L_N	analogue	microphone input negative(left side)
3	MIC_R_P	analogue	microphone input positive(right side)
4	MIC_R_N	analogue	microphone input negative(right side)
5	AIO[0]	bi-directional	programmable input/output line
6	AIO[1]	bi-directional	programmable input/output line
7	AIO[3]	bi-directional	programmable input/output line
8	1V8	VDD	positive supply(1.7V~1.9V)
9	3V3	VDD	positive supply(2.7V~3.6V)
10	UART_RX	CMOS input with weak internal pull-down	UART data input
11	UART_RTS	CMOS output, tri-state, with weak internal pull-up	UART request to send active low
12	UART_TX	CMOS output, tri-state, with weak internal pull-up	UART data output
13	UART_CTS	CMOS input with weak internal pull-down	UART clear to send active low
14	GND	VSS	ground connection
15	USB_DP	bi-directional	USB data plus
16	USB_DN	bi-directional	USB data minus
17	PCM_CLK	bi-directional with weak internal pull-down	synchronous data clock
18	PCM_IN	CMOS input with weak internal pull-down	synchronous data input
19	PCM_SYNC	bi-directional with weak internal pull-down	synchronous data sync

20	PCM_OUT	CMOS output, tri-state, with weak internal pull-down	synchronous data output
21	PIO[4]	bi-directional with programmable strength internal pull-up/down	programmable input/output line
22	PIO[6]	bi-directional with programmable strength internal pull-up/down	programmable input/output line
23	SPI_CLK		
24	SPI_MISO		
25	GND	VSS	ground connection
26	SPI_MOSI		
27	SPI_CSB		
28	RESET	CMOS input with weak internal pull-down	reset if high. Input debounced so must be high for >5ms to cause a reset
29	PIO[11]	bi-directional with programmable strength internal pull-up/down	programmable input/output line
30	PIO[10]	bi-directional with programmable strength internal pull-up/down	programmable input/output line
31	PIO[9]	bi-directional with programmable strength internal pull-up/down	programmable input/output line
32	PIO[3]	bi-directional with programmable strength internal pull-up/down	programmable input/output line
33	PIO[1]	bi-directional with programmable strength internal pull-up/down	programmable input/output line

34	PIO[0]	bi-directional with programmable strength internal pull-up/down	programmable input/output line
35	RF_IN	analogue	single ended receiver input(not used)
36	GND	VSS	ground connection
37	RF I/O	analogue	Bluetooth signal input/output port
38	GND	VSS	ground connection
39	PIO[2]	bi-directional with programmable strength internal pull-up/down	programmable input/output line
40	AUX_DAC	analogue	voltage DAC output
41	PIO[8]	bi-directional with programmable strength internal pull-up/down	programmable input/output line
42	PIO[5]	bi-directional with programmable strength internal pull-up/down	programmable input/output line
43	PIO[7]	bi-directional with programmable strength internal pull-up/down	programmable input/output line
44	SPKR_R_N	analogue	speaker output negative(right side)
45	SPKR_R_P	analogue	speaker output positive(right side)
46	SPKR_L_N	analogue	speaker output negative(left side)
47	SPKR_L_P	analogue	speaker output positive(left side)
48	GND	VSS	ground connection

Bluetooth Firmware update method

We suggest that reserve the SPI PIN connection on PCB when designing your product. The following is the PIN order we recommend.

Order	Name	Description
1	3V3	Power for Bluetooth module
2	GND	ground connection
3	MISO	serial peripheral interface data output
4	CSB	chip select for synchronous serial interface active low
5	CLK	serial peripheral interface clock
6	MOSI	serial peripheral interface data input

Appendix:

Reference circuit:

TBA