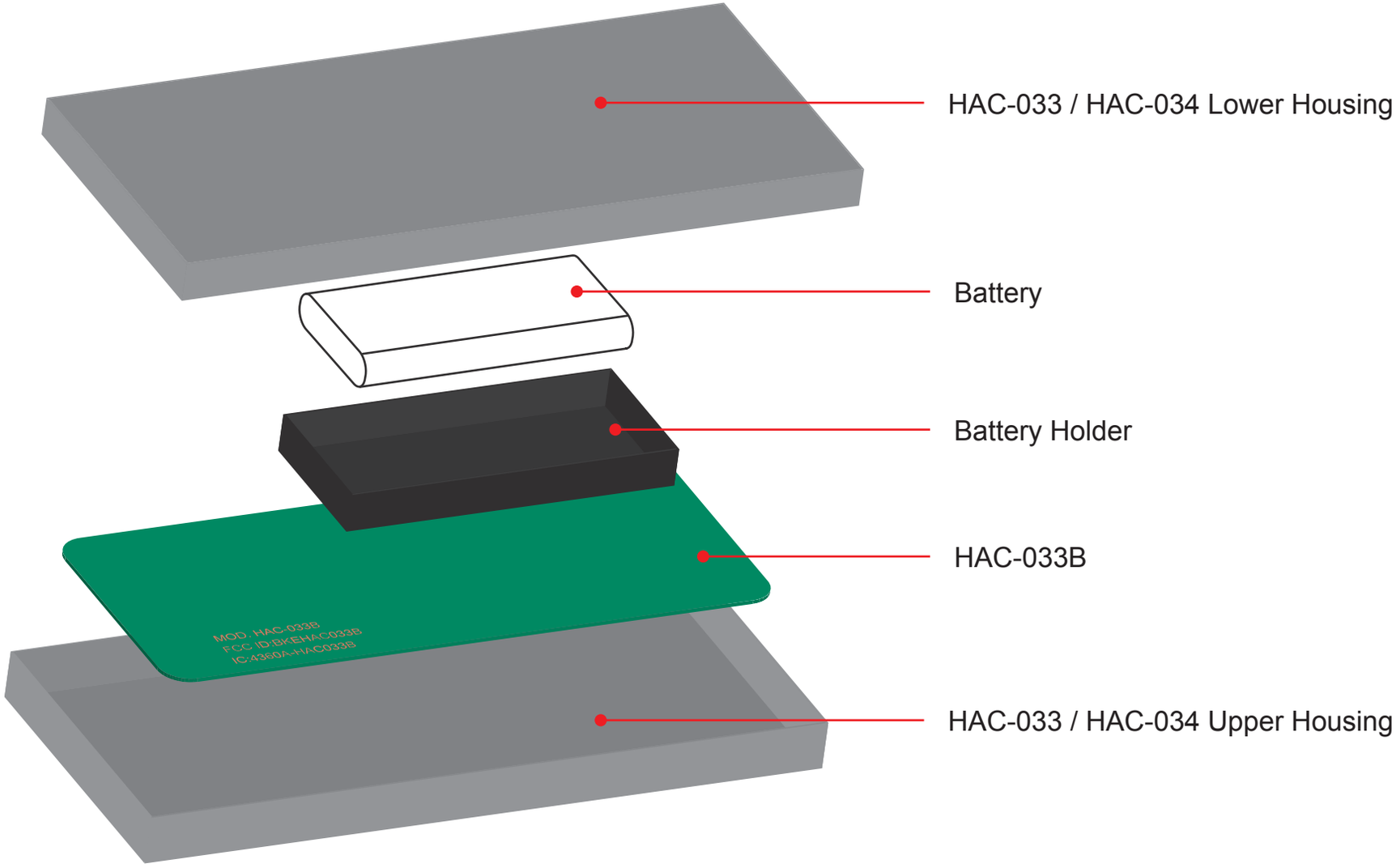
HAC-033B Module Installation Manual

Assembly drawing



Specifications

1.1 Electrical Characteristics

Table1 shows the maximum electrical rating for voltages referenced to VDD pin.

Table 1. Absolute Maximum Voltages

Requirement Parameter	Specification			Unit
	Minimum	Nominal	Maximum	
Ambient Temperature of Operation	–30	25	85	°C
Storage temperature	–40	–	150	°C
ESD Tolerance HBM	–2000	–	2000	V
ESD Tolerance MM	–100	–	100	V
ESD Tolerance CDM	–500	–	500	V
Latch-up	–	200	–	mA
VDD Core	1.14	1.2	1.26	V
VDD IO	1.62	3.3	3.6	V
VDD RF (excluding class 1 PA)	1.14	1.2	1.26	V

Table2 shows the power supply characteristics for the range T_J = 0°C to 125°C.

Table 2. Power Supply Specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
VBAT input	–	1.62	3.3	3.6	V
Operating temperature	Junction temperature	–40	50	125	°C
Total system leakage	Max value is defined at temp = 85°C	–	0.5	1.3	µA
PMU turn-on time	VBAT is ready.	TBD	–	300	µs

Table 3 shows the digital level characteristics for (VSS = 0V).

Table 3. VDDC LDO Electrical Specifications

Parameter	Conditions		Min.	Typical	Max.	Unit
Input Voltage	–		1.62	3.3	3.6	V
Nominal Output Voltage	–		–	1.2		V
DC Accuracy	Accuracy at any step, including bandgap reference.		–5	–	5	%
Output Voltage Programmability	Range		0.89	–	1.34	V
	Step Size		–	30	–	mV
Load Current	–		–	–	40	mA
Dropout Voltage	I_{load} = 40 mA		–	–	200	mV
Line Regulation	Vin from 1.62V to 3.6V, I_{load} = 40 mA		–	–	0.2	%Vo/V
Load Regulation	I_{load} = 1 mA to 40 mA, Vout = 1.2V, Package + PCB R = 0.3Ω		–	0.02	0.05	%Vo/mA
Quiescent Current	No load @Vin = 3.3V		–	18	23	µA
	Max load @Vin = 3.3V		–	–	0.56 0.65	mA
Power down Current	Vin = 3.3V @25C		–	0.2	–	µA
	Vin = 3.6 @80C		–	TBD	–	–
Output Noise	I_{load} = 15 mA, 100 kHz		–		40	nV/sqrtHz
	I_{load} = 15 mA, 2 MHz		–		14	nV/sqrtHz
PSRR	Vin = 3.3, Vout = 1.2V, I_{load} = 40 mA	1 kHz	65	–	–	dB
		10 kHz	60	–	–	dB
		100 kHz	55	–	–	dB
Over Current Limit	–		100	–	–	mA
Turn-on Time	VBAT = 3.3V, BG already on, LDO OFF to ON, Co = 1 µF, 90% of Vout		–	–	100	µs
In-rush current during turn-on	During start-up, Co = 1 µF		–	–	60	mA
Transient Performance	I_{load} = 1 mA to 15 mA and 15 mA to 1 mA in 1 µs		–	–	40	mV
	I_{load} = 15 mA to 40 mA and 40 mA to 15 mA in 1 µs		–	–	25	–
External Output Capacitor	Ceramic cap with ESR ≤0.5Ω		0.8	1	4.7	µF
External Input Capacitor	Ceramic, X5R, 0402, ±20%, 10V.		–	1	–	µF

Table 4. ADC Microphone Specifications (Cont.)

Parameter	Symbol	Conditions/Comments	Min.	Typical	Max.	Unit
MIC bias noise	–	■ PGA input referred. 6 dB attenuation is assumed from MIC bias output to PGA input. ■ 20 Hz to 8 kHz ■ A-weighted	–	–	3	µV
ADC SNR	–	■ A-weighted ■ 0 dB PGA gain	78	–	–	dB
ADC THD + N	–	■ –3 dBFS input ■ 0 dB PGA gain	74	–	–	dB
GPIO input voltage	–	Must be lower than VBAT	–	–	3.6	V
GPIO source impedance[a]	–	Resistance	–	–	1	kΩ
	–	Capacitance	–	–	10	pF

a. Conditional requirement for the measurement time of 10 µs. Relaxed with longer measurement time for each GPIO input channel.

Table 5. Digital I/O Characteristics

Characteristics	Symbol	Minimum	Typical	Maximum	Unit
Input low voltage (VDDO = 3.3V)	V_{IL}	–	–	0.8	V
Input high voltage (VDDO = 3.3V)	V_{IH}	2.0	–	–	V
Input low voltage (VDDO = 1.8V)	V_{IL}	–	–	0.6	V
Input high voltage (VDDO = 1.8V)	V_{IH}	1.1	–	–	V
Output low voltage	V_{OL}	–	–	0.4	V
Output high voltage	V_{OH}	VDDO – 0.4V	–	–	V
Input low current	I_{IL}	–	–	1.0	µA
Input high current	I_{IH}	–	–	1.0	µA
Output low current (VDDO = 3.3V, V_{OL} = 0.4V)	I_{OL}	–	–	8.0	mA
Output high current (VDDO = 3.3V, V_{OH} = 2.9V)	I_{OH}	–	–	8.0	mA
Output high current (VDDO = 1.8V, V_{OH} = 1.4V)	I_{OH}	–	–	4.0	mA
Input capacitance	C_{IN}	–	–	0.4	pF

Note:

In Table 5, current consumption measurements are t aken at VBAT with the assumption that VBAT is connected to VDDIO and LDOIN.

Table 6. Bluetooth Current Consumption, Class1

Operating Mode	Typical	Unit
DM1/DH1	32.15	mA
DM3/DH3	38.14	mA
DM5/DH5	38.46	mA
3DH5/3DH5	37.10	mA
Page scan	486	µA
Sniff slave (495 ms)	254	µA
Sniff slave (22.5 ms)	2.6	mA
Sniff slave (11.25 ms)	4.95	mA
HIDOFF (deep sleep)	2.69	µA

a. No devices present. A 1.28 second interval with a scan window of 11.25 ms.

Table 7. Bluetooth Current Consumption, Class 2(0 dbm)

Operating Mode	Typical	Unit
DM1/DH1	27.5	mA
DM3/DH3	31.34	mA
DM5/DH5	32.36	mA
3DH5/3DH5	31.57	mA
HIDOFF (deep sleep)	2.69	µA

a. No devices present. A 1.28 second interval with a scan window of 11.25 ms.

2 RF Specifications

Note:

- All specifications in Table 8 are for industrial temperatures.
- All specifications in Table 8 are single-ended. Unused inputs are left open.

Table 8. Receiver RF Specifications

Parameter	Conditions	Minimum	Typical [a]	Maximum	Unit
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity [b]	GFSK, 0.1% BER, 1 Mbps	–	–93.5	–	dBm
	LE GFSK, 0.1% BER, 1 Mbps	–	–96.5	–	dBm
	π/4-DQPSK, 0.01% BER, 2 Mbps	–	–95.5	–	dBm
	8-DPSK, 0.01% BER, 3 Mbps	–	–89.5	–	dBm
Maximum input	GFSK, 1 Mbps	–	–	–20	dBm
Maximum input	π/4-DQPSK, 8-DPSK, 2/3 Mbps	–	–	–20	dBm
Interference Performance					
C/I cochannel	GFSK, 0.1% BER	–	9.5	11	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER	–	–5	0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER	–	–40	–30.0	dB
C/I ≥ 3 MHz adjacent channel	GFSK, 0.1% BER	–	–49	–40.0	dB
C/I image channel	GFSK, 0.1% BER	–	–27	–9.0	dB
C/I 1 MHz adjacent to image channel	GFSK, 0.1% BER	–	–37	–20.0	dB
C/I cochannel	π/4-DQPSK, 0.1% BER	–	11	13	dB
C/I 1 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–8	0	dB
C/I 2 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–40	–30.0	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–50	–40.0	dB
C/I image channel	π/4-DQPSK, 0.1% BER	–	–27	–7.0	dB
C/I 1 MHz adjacent to image channel	π/4-DQPSK, 0.1% BER	–	–40	–20.0	dB
C/I cochannel	8-DPSK, 0.1% BER	–	17	21	dB
C/I 1 MHz adjacent channel	8-DPSK, 0.1% BER	–	–5	5	dB
C/I 2 MHz adjacent channel	8-DPSK, 0.1% BER	–	–40	–25.0	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–47	–33.0	dB
C/I Image channel	8-DPSK, 0.1% BER	–	–20	0	dB
C/I 1 MHz adjacent to image channel	8-DPSK, 0.1% BER	–	–35	–13.0	dB
Out-of-Band Blocking Performance (CW)[c]					
30 MHz–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000–2399 MHz	0.1% BER	–	–27	–	dBm
2498–3000 MHz	0.1% BER	–	–27	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	dBm

Table 8. Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical [a]	Maximum	Unit
Out-of-Band Blocking Performance, Modulated Interferer					
776–764 MHz	CDMA	–	–10[d]	–	dBm
824–849 MHz	CDMA	–	–10[d]	–	dBm
1850–1910 MHz	CDMA	–	–23[d]	–	dBm
824–849 MHz	EDGE/GSM	–	–10[d]	–	dBm
880–915 MHz	EDGE/GSM	–	–10[d]	–	dBm
1710–1785 MHz	EDGE/GSM	–	–23[d]	–	dBm
1850–1910 MHz	EDGE/GSM	–	–23[d]	–	dBm
1850–1910 MHz	WCDMA	–	–23[d]	–	dBm
1920–1980 MHz	WCDMA	–	–23[d]	–	dBm
Intermodulation Performance[e]					
BT, Df = 5 MHz	–	–39.0	–	–	dBm
Spurious Emissions[f]					
30 MHz to 1 GHz	–	–	–	–62	dBm
1 GHz to 12.75 GHz	–	–	–	–47	dBm
65 MHz to 108 MHz	FM RX	–	–147	–	dBm/Hz
746 MHz to 764 MHz	CDMA	–	–147	–	dBm/Hz
851–894 MHz	CDMA	–	–147	–	dBm/Hz
925–960 MHz	EDGE/GSM	–	–147	–	dBm/Hz
1805–1880 MHz	EDGE/GSM	–	–147	–	dBm/Hz
1930–1990 MHz	PCS	–	–147	–	dBm/Hz
2110–2170 MHz	WCDMA	–	–147	–	dBm/Hz

a. Typical operating conditions are 1.22V operating voltage and 25°C ambient temperature.
b. The receiver sensitivity is measured at BER of 0.1% on the device interface.
c. Meets this specification using front-end band pass filter.
d. Numbers are referred to the pin output with an external BPF filter.
e. f0 = -64 dBm Bluetooth-modulated signal, f1 = –39 dBm sine wave, f2 = –39 dBm Bluetooth-modulated signal, f0 = 2f1 – f2, and |f2 – f1| = n*1 MHz, where n is 3, 4, or 5. For the typical case, n = 4.
f. Includes baseband radiated emissions.

Note:

- All specifications in Table 9 are for industrial temperatures.
- All specifications in Table 9 are single-ended. Unused inputs are left open.

Table 9. Transmitter RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
General					
Frequency range	–	2402	–	2480	MHz
Class1: GFSK TX power[a]	–	–	12	–	dBm
Class1: EDR TX power[b]	–	–	9	–	dBm
Class 2: GFSK TX power	–	–	2	–	dBm
Power control step	–	2	4	8	dB
Modulation Accuracy					
π/4-DQPSK Frequency Stability	–	–10	–	10	kHz
π/4-DQPSK RMS DEVM	–	–	–	20	%
π/4-QPSK Peak DEVM	–	–	–	35	%
π/4-DQPSK 99% DEVM	–	–	–	30	%
8-DPSK frequency stability	–	–10	–	10	kHz
8-DPSK RMS DEVM	–	–	–	13	%
8-DPSK Peak DEVM	–	–	–	25	%
8-DPSK 99% DEVM	–	–	–	20	%
In-Band Spurious Emissions					
1.0 MHz < |M – N| < 1.5 MHz	–	–	–	–26	dBc
1.5 MHz < |M – N| < 2.5 MHz	–	–	–	–20	dBm
|M – N| ≥ 2.5 MHz	–	–	–	–40	dBm
Out-of-Band Spurious Emissions					
30 MHz to 1 GHz	–	–	–	–36.0[c]	dBm
1 GHz to 12.75 GHz	–	–	–	–30.0[c, d]	dBm
1.8 GHz to 1.9 GHz	–	–	–	–47.0	dBm
5.15 GHz to 5.3 GHz	–	–	–	–47.0	dBm

a. TBD dBm output for GFSK measured with PAVDD = 2.5V.
b. TBD dBm output for EDR measured with PAVDD = 2.5V.
c. Maximum value is the value required for Bluetooth qualification.
d. Meets this spec using a front-end band-pass filter.

3 Timing and AC Characteristics

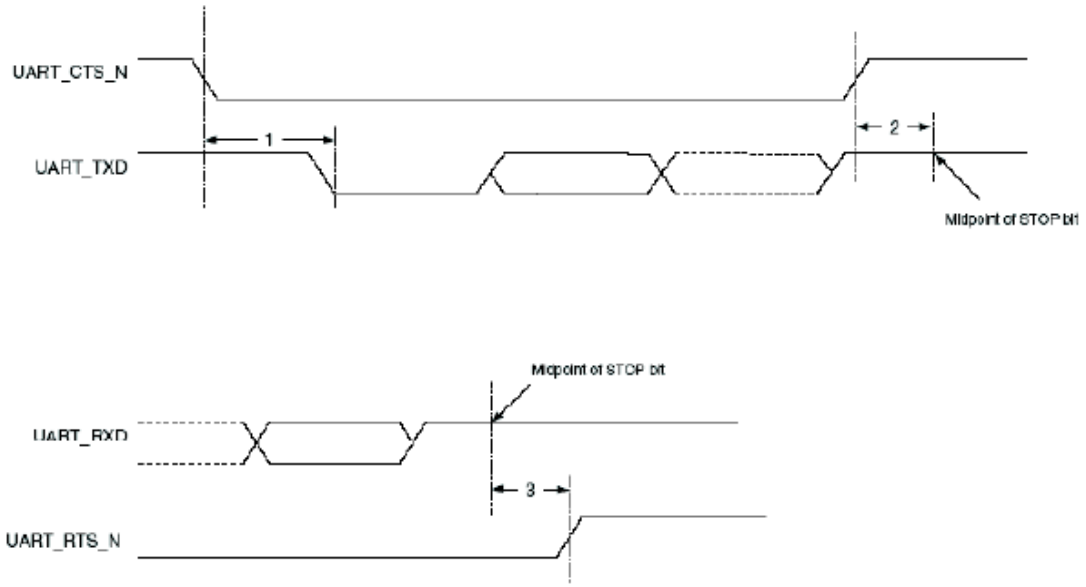
In this section, use the numbers listed in the **Reference** column of each table to interpret the following timing diagrams.

UART Timing

Table 10. UART Timing Specifications

Reference	Characteristics	Min.	Max.	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	–	24	Baud out cycles
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	10	ns
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	2	Baud out cycles

Figure 9. UART Timing



Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	I/O	Power Domain	Description
Radio I/O				
A1	RFOP	I/O	PAVDD	RF antenna port
RF Power Supplies				
D1	IFVDD1P2	I	IFVDD1P2	IFPLL power supply
B1	LNAVDD1P2	I	LNAVDD1P2	RF front-end supply
C1	VCOVDD1P2	I	VCOVDD1P2	VCO supply
B2	PLLVDD1P2	I	PLLVDD1P2	RFPLL and crystal oscillator supply
A3	PAVDD	O	PAVDD	PA supply
Power Supplies				
F1, G3	VDDC	I	VDDC	Baseband core supply
A9, K1	VDDO	I	VDDO	I/O pad and core supply
B6	MIC_AVDD	I	MIC_AVDD	Microphone supply
A5	ADC_AVBAT	I	ADC_AVBAT	ADC supply
A8	ADC_AVDDC	I	ADC_AVDDC	ADC supply
Ground				
A2, A10, B5, C2, C3, D3, F2, J1, K10	VSS	I	VSS	Ground
B8	AVSS	I	AVSS	Analog ground
Clock Generator and Crystal Interface				
B4	XTALI	I	PLLVDD1P2	Crystal oscillator input. See “Crystal Oscillator” on page 10 for options.
A4	XTALO	O	PLLVDD1P2	Crystal oscillator output.
E6	XTALI32K	I	PLLVDD1P2	Low-power oscillator input.
F6	XTALO32K	O	PLLVDD1P2	Low-power oscillator output.
Core				
H3	RESET_N	I/O PU	VDDO	Active-low system reset with open-drain output and internal pull-up resistor.
F5	TM1	I	VDDO	Device test mode control. Connect to GND for all applications.
E5	JTAG_SEL	I	VDDO	ARM JTAG debug mode control. Connect to GND for all applications.
Microphone				
A7	MICP	I	MIC_AVDD	Microphone positive input
B7	MICN	I	MIC_AVDD	Microphone negative input
A6	MIC_BIAS	O	MIC_AVDD	Microphone bias supply
PCM2/I^2S				
J3	PCM_SYNC	I/O, PD	VDDO	Frame synchronization for PCM interface. Alternate function: I^2S word select
K2	PCM_CLK	I/O, PD	VDDO	Clock for PCM interface. Alternate function: I^2S clock

Table 1. Pin Descriptions (Cont.)

Pin Number	Pin Name	I/O	Power Domain	Description
K3	PCM_IN	I, PU	VDDO	Data input for PCM interface. Alternate function: I^2S data input SDA
J2	PCM_OUT	O, PD	VDDO	Data output for PCM interface. Alternate function: I^2S data output SCL
UART				
H5	UART_RXD	I	VDDO	UART serial input – Serial data input for the HCI UART interface.
H4	UART_TXD	O, PU	VDDO	UART serial output – Serial data output for the HCI UART interface.
J4	UART_RTS_N	O, PU	VDDO	Request to send (RTS) for HCI UART interface. Leave unconnected if not used.
J5	UART_CTS_N	I, PU	VDDO	Clear to send (CTS) for HCI UART interface. Leave unconnected if not used.
BSC/SPI				
H1	SPI_MISO_SCL	I/O	VDDO	BSC clock
G1	SPI_MOSI_SDA	I/O	VDDO	BSC data
G2	SPI_CLK	I/O	VDDO	Serial flash SPI clock
H2	SPI_CSN	I/O	VDDO	Serial flash active-low chip select
LDO Regulator Power Supplies				
B3	VBAT	I	VBAT	1.2V LDO input
E1	VDDC_OUT	O	VDDC_OUT	1.2V LDO output
Reserved				
F4	Reserved0	I	VDDO	Reserved. Leave unconnected.
D5	Reserved1	I	VDDO	Reserved. Leave unconnected.
E3	Reserved2	I	VDDO	Reserved. Connect to GND.
E4	Reserved3	I	VDDO	Reserved. Leave unconnected.
D4	Reserved4	I	VDDO	Reserved. Connect to GND.

Table 2. GPIO Pin Descriptions[a]

Pin Number	Pin Name	Default Direction	POR State	Post-Reset State[b]	Power Domain	Alternate Function Description
G7	P0	Input	Floating	Floating	VDDO	■ GPIO: P0 ■ Keyboard scan input (row): KSI0 ■ A/D converter input 29 ■ Peripheral UART: puart_tx ■ SPI_1: MOSI (master and slave) ■ IR_RX ■ 60Hz_main **Note:** Not available during TM1 = 1.
G6	P1	Input	Floating	Floating	VDDO	■ GPIO: P1 ■ Keyboard scan input (row): KSI1 ■ A/D converter input 28 ■ Peripheral UART: puart_rts ■ SPI_1: MISO (master and slave) ■ IR_TX
C9	P2	Input	Floating	Floating	VDDO	■ GPIO: P2 ■ Keyboard scan input (row): KSI2 ■ Quadrature: QDX0 ■ Peripheral UART: puart_rx ■ SPI_1: SPI_CS (slave only) ■ SPI_1: MOSI (master only)
E9	P3	Input	Floating	Floating	VDDO	■ GPIO: P3 ■ Keyboard scan input (row): KSI3 ■ Quadrature: QDX1 ■ Peripheral UART: puart_cts ■ SPI_1: SPI_CLK (master and slave)
G10	P4	Input	Floating	Floating	VDDO	■ GPIO: P4 ■ Keyboard scan input (row): KSI4 ■ Quadrature: QDY0 ■ Peripheral UART: puart_rx ■ SPI_1: MOSI (master and slave) ■ IR_TX
K4	P5	Input	Floating	Floating	VDDO	■ GPIO: P5 ■ Keyboard scan input (row): KSI5 ■ Quadrature: QDY1 ■ Peripheral UART: puart_tx ■ SPI_1: MISO (master and slave) ■ BSC: SDA

Table 2. GPIO Pin Descriptions[a] (Cont.)

Pin Number	Pin Name	Default Direction	POR State	Post-Reset State[b]	Power Domain	Alternate Function Description
G4	P6	Input	Floating	Floating	VDDO	■ GPIO: P6 ■ Keyboard scan input (row): KSI6 ■ Quadrature: QDZ0 ■ Peripheral UART: puart_rts ■ SPI_1: SPI_CS (slave only) ■ 60Hz_main
B10	P7	Input	Floating	Floating	VDDO	■ GPIO: P7 ■ Keyboard scan input (row): KSI7 ■ Quadrature: QDZ1 ■ Peripheral UART: puart_cts ■ SPI_1: SPI_CLK (master and slave) ■ BSC: SCL
D7	P8	Input	Floating	Floating	VDDO	■ GPIO: P8 ■ Keyboard scan output (column): KSO0 ■ A/D converter input 27 ■ External T/R switch control: ~tx_pd
D9	P9	Input	Floating	Floating	VDDO	■ GPIO: P9 ■ Keyboard scan output (column): KSO1 ■ A/D converter input 26 ■ External T/R switch control: tx_pd
G8	P10	Input	Floating	Floating	VDDO	■ GPIO: P10 ■ Keyboard scan output (column): KSO2 ■ A/D converter input 25 ■ External PA ramp control: ~PA_Ramp
G9	P11	Input	Floating	Floating	VDDO	■ GPIO: P11 ■ Keyboard scan output (column): KSO3 ■ A/D converter input 24
C10	P12	Input	Floating	Floating	VDDO	■ GPIO: P12 ■ Keyboard scan output (column): KSO4 ■ A/D converter input 23
E8	P13	Input	Floating	Floating	VDDO	■ GPIO: P13 ■ Keyboard scan output (column): KSO5 ■ A/D converter input 22 ■ PWM3 ■ Triac control 3

Table 2. GPIO Pin Descriptions[a] (Cont.)

Pin Number	Pin Name	Default Direction	POR State	Post-Reset State[b]	Power Domain	Alternate Function Description
J7	P14	Input	Floating	Input enable, pull-down	VDDO	■ GPIO: P14 ■ Keyboard scan output (column): KSO6 ■ A/D converter input 21 ■ PWM2 ■ Triac control 4
J8	P15	Input	Floating	Input enable, pull-up	VDDO	■ GPIO: P15 ■ Keyboard scan output (column): KSO7 ■ A/D converter input 20 ■ IR_RX ■ 60Hz_main
B9	P16	Input	Floating	Floating	VDDO	■ GPIO: P16 ■ Keyboard scan output (column): KSO8 ■ A/D converter input 19
J10	P17	Input	Floating	Floating	VDDO	■ GPIO: P17 ■ Keyboard scan output (column): KSO9 ■ A/D converter input 18
F9	P18	Input	Floating	Floating	VDDO	■ GPIO: P18 ■ Keyboard scan output (column): KSO10 ■ A/D converter input 17
H7	P19	Input	Floating	Floating	VDDO	■ GPIO: P19 ■ Keyboard scan output (column): KSO11 ■ A/D converter input 16
F10	P20	Input	Floating	Floating	VDDO	■ GPIO: P20 ■ Keyboard scan output (column): KSO12
D10	P21	Input	Floating	Floating	VDDO	■ GPIO: P21 ■ Keyboard scan output (column): KSO13 ■ A/D converter input 14 ■ Triac control 3
E6	P22	Input	Floating	Floating	VDDO	■ GPIO: P22 ■ Keyboard scan output (column): KSO14 ■ A/D converter input 13 ■ Triac control 4 ■ XTALO32K
F6	P23	Input	Floating	Floating	VDDO	■ GPIO: P23 ■ Keyboard scan output (column): KSO15 ■ A/D converter input 12 ■ XTALI32K

Table 2. GPIO Pin Descriptions[a] (Cont.)

Pin Number	Pin Name	Default Direction	POR State	Post-Reset State[b]	Power Domain	Alternate Function Description
G5	P24	Input	Floating	Floating	VDDO	■ GPIO: P24 ■ Keyboard scan output (column): KSO16 ■ SPI_1: SPI_CLK (master and slave) ■ Peripheral UART: puart_tx
F7	P25	Input	Floating	Floating	VDDO	■ GPIO: P25 ■ Keyboard scan output (column): KSO17 ■ SPI_1: MISO (master and slave) ■ Peripheral UART: puart_rx
K8	P26 PWM0	Input	Floating	Input enable, pull-down	VDDO	■ GPIO: P26 ■ Keyboard scan output (column): KSO18 ■ SPI_1: SPI_CS (slave only) ■ Optical control output: QOC0 ■ Triac control 1 ■ Current: 16 mA sink
K9	P27 PWM1	Input	Floating	Floating	VDDO	■ GPIO: P27 ■ Keyboard scan output (column): KSO19 ■ SPI_1: MOSI (master and slave) ■ Optical control output: QOC1 ■ Triac control 2 ■ Current: 16 mA sink
K7	P28 PWM2	Input	Floating	Input enable, pull-up	VDDO	■ GPIO: P28 ■ Optical control output: QOC2 ■ A/D converter input 11 ■ LED1 ■ Current: 16 mA sink
K6	P29 PWM3	Input	Floating	Floating	VDDO	■ GPIO: P29 ■ Optical control output: QOC3 ■ A/D converter input 10 ■ LED2 ■ Current: 16 mA sink
J9	P30	Input	Floating	Floating	VDDO	■ GPIO: P30 ■ A/D converter input 9 ■ Peripheral UART: puart_rts
H6	P31	Input	Floating	Floating	VDDO	■ GPIO: P31 ■ A/D converter input 8 ■ Peripheral UART: puart_tx

Table 2. GPIO Pin Descriptions[a] (Cont.)

Pin Number	Pin Name	Default Direction	POR State	Post-Reset State[b]	Power Domain	Alternate Function Description
H9	P32	Input	Floating	Floating	VDDO	■ GPIO: P32 ■ A/D converter input 7 ■ Quadrature: QDX0 ■ SPI_1: SPI_CS (slave only) ■ Auxiliary clock output: ACLK0 ■ Peripheral UART: puart_tx
H10	P33	Input	Floating	Floating	VDDO	■ GPIO: P33 ■ A/D converter input 6 ■ Quadrature: QDX1 ■ SPI_1: MOSI (slave only) ■ Auxiliary clock output: ACLK1 ■ Peripheral UART: puart_rx
H8	P34	Input	Floating	Floating	VDDO	■ GPIO: P34 ■ A/D converter input 5 ■ Quadrature: QDY0 ■ Peripheral UART: puart_rx ■ External T/R switch control: tx_pd
F8	P35	Input	Floating	Floating	VDDO	■ GPIO: P35 ■ A/D converter input 4 ■ Quadrature: QDY1 ■ Peripheral UART: puart_cts ■ BSC: SDA
D8	P36	Input	Floating	Floating	VDDO	■ GPIO: P36 ■ A/D converter input 3 ■ Quadrature: QDZ0 ■ SPI_1: SPI_CLK (master and slave) ■ Auxiliary Clock Output: ACLK0 ■ External T/R switch control: ~tx_pd
E7	P37	Input	Floating	Floating	VDDO	■ GPIO: P37 ■ A/D converter input 2 ■ Quadrature: QDZ1 ■ SPI_1: MISO (slave only) ■ Auxiliary clock output: ACLK1 ■ BSC: SCL

Table 2. GPIO Pin Descriptions[a] (Cont.)

Pin Number	Pin Name	Default Direction	POR State	Post-Reset State[b]	Power Domain	Alternate Function Description
D6	P38	Input	Floating	Floating	VDDO	■ GPIO: P38 ■ A/D converter input 1 ■ SPI_1: MOSI (master and slave) ■ IR_TX
J6	P39	Input	Floating	Floating	VDDO	■ GPIO: P39 ■ SPI_1: SPI_CS (slave only) ■ Infrared control: IR_RX ■ External PA ramp control: PA_Ramp ■ 60Hz_main

a. During power-on reset, all inputs are disabled.
b. The post-reset state is the GPIO state just after a power-on reset before firmware gets loaded.

Note: This content can be viewed on the web.

FCC StatementFCC and ISED Module Information

The module is limited to OEM installation ONLY.

This module is intended for OEM integrators under the following conditions:

1. This module is restricted to installation in products for use only in portable applications.
2. The antenna(s) used for this transmitter must follow the specific operating instructions for satisfying RF exposure compliance.
3. The antenna(s) used for this transmitter must not transmit simultaneously with any other antenna or transmitter.

The OEM integrator is still responsible for

1. ensuring that the end-user has no manual instructions to remove or install module
2. the FCC compliance requirement of the end product, which integrates this module.
3. Appropriate measurements (e.g. 15 B compliance) and if applicable additional equipment authorizations (e.g. Verification, Doc) of the host device to be addressed by the integrator/manufacturer.
4. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations

Guidance to the Host Manufacturer:

1. We hereby acknowledge our responsibility to provide guidance to the host manufacturer in the event that they require assistance for ensuring compliance with the Part 15 Subpart B requirements.

2. The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with the Part 15 Subpart B requirements, the host manufacturer is required to show compliance with the Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions) with the Radio essential requirements. The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in the Part 15 Subpart B or emissions are complaint with the Radio aspects.

The user manual of the end product should include

1. Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.
2. the restriction of operating this device in indoor could void the user's authority to operate the equipment.
3. This device and its antenna(s) must not be co-located or operating in conjunction with any other antenna or transmitter.
4. This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End user must follow the specific operating instructions for satisfying RF exposure compliance.
5. The FCC part 15.19 statement: This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Label of the end product:

The final end product must be labeled in a visible area with the following " Contains FCC ID: **BKEHAC033B** ".

The end product shall bear the following 15.19 statement: This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

If the labelling area is considered too small and therefore it is impractical (smaller than the palm of the hand) to display the compliance statement, then the statement may be placed in the user manual or product packaging.

ISED Statement

OEM integrator is still responsible for testing their end product for any additional compliance requirements required with this module installed.

IMPORTANT NOTE: In the event that these conditions cannot be met, then the IC authorization is no longer considered valid and the IC No. cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate IC authorization.

Modular OEM Integrator Notice

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed must follow the specific operating instructions for

satisfying RF exposure compliance.. The final end product must be labeled in a visible area with the following: “Contains IC: 4360A-HAC033B”.

This device is intended only for OEM integrators under the following conditions:

1) The antenna must follow the specific operating instructions for satisfying RF exposure compliance.

2) The transmitter module may not be co-located with any other transmitter or antenna.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit suivre les instructions d'utilisation spécifiques pour satisfaire la conformité à l'exposition RF.

2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Modular OEM Integrator Notice

IMPORTANT NOTE for OEM integrator:

This module is intended for OEM integrator.

The OEM integrator is still responsible for

1. ensuring that the end-user has no manual instructions to remove or install module
2. the ISED compliance requirement of the end product, which integrates this module.
3. Appropriate measurements and if applicable additional equipment authorizations of the host device to be addressed by the integrator/manufacturer.
4. The separate approval is required for all other operating configurations, including portable configurations and different antenna configurations