SECTION IX

THEORY OF OPERATION

9.1 The EAS Information Super Highway

The Emergency Alert System (EAS) is a nationwide network of radio and television broadcast and cable facilities that can originate or receive and forward (re-transmit) event- and location-specific Emergency Alert messages. Alert messages can originate from the White House, state and local safety agencies, Emergency Operation Centers (EOC), and the National Weather Service (85% of alerts are weather related).
When an agency is sues an Alert, it transmits an EAS header and message to local AM, FM, and TV stations and cable systems which, in turn, broadcast the message to the general public if the message matches the local requirements. The public can receive alert messages in a matter of seconds and can react quickly to impending emergencies.
The EAS message contains digitally encoded event and location information in addition to a normal voice or text announcement. The encoded information permits the network of broadcast and cable stations to decode messages and forward them automatically or manually to a specific area affected by the emergency alert.

9.2 The EAS DECODER: An Overview

The EAS DECODER is similar to a smart telephone answering machine. It receives and screens messages on one or two, records and stores them, and forwards selected messages manually or automatically.

The digital header in the incoming message is decoded and translated, then displayed on the Liquid Crystal Display (LCD) and logged on the printer. The event and location data is compared with the data stored in the Setup memory to determine if it should be forwarded.

If the alert message is to be forwarded, the EAS DECODER inserts a new I.D. code and re-transmits it, along with a two-tone Attention Signal, the recorded voice message and an End Of Message signal. Forwarding can occur automatically or after operator intervention.

Refer to Figure 9.2 for a simplified block diagram of the EAS DECODER.

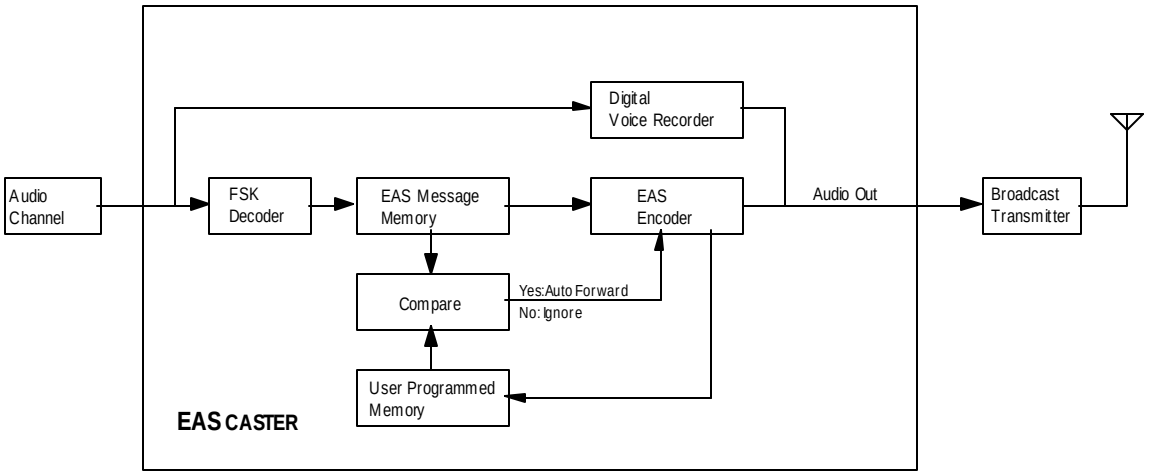

Figure 9.2, EAS DECODER Block Diagram

9.3 A Closer Look: Detailed System Block Diagram

The EAS DECODER system consists of the Main Board, the Encoder and Decoder keyboards, the LCD Display Assembly, the Digital Voice Recorder, the Comm Expander and the Printer. Figure 1 in Appendix A illustrates the EAS DECODER system blocks in detail.

9.4 Main Board (Figure 2, Appendix A)

The EAS DECODER Main Board consists of three major system blocks: Audio Loop-Through and Switching, Digital Signal Processor/CPU, and Input/Output Control.

9.4.1 Audio Loop Through and Switching (Figure 2, Appendix A)

The audio buffering, switching and control section is illustrated on sheet 1 of the Main Board schematic drawing (6601-4060).

U1 and U2 provide two balanced input amplifiers for the Channel 1 and 2 audio inputs. Analog switches U3, U8 and U10 route audio signals to and from the inputs, outputs and voice recorder. U4 and U5 are Coders/Decoders (CODECs) that convert the audio signals to digital data, and vice-versa. U7 provides two buffer amplifiers at the outputs of the CODECs. U11 is the internal speaker amplifier; U12 provides a balanced audio EAS message output.

9.4.2 Digital Signal Processor/CPU (Figure 2, Appendix A)

The Digital Signal Processor (DSP) section and its related logic is illustrated on sheet 2 of the schematic drawing (6601-4060).

U14 is a Texas Instruments TMS320C26 digital signal processor that performs all encoding and decoding functions, and controls all I/O activity. U13 is a Field Programmable Gate Array (FPGA). It generates all internal timing signals and performs all internal digital signal routing. U15 is a real-time clock and provides battery backed-up memory for long term storage of setup information. U16 and U18 are the system random access memory (RAM); U17 and U19 are the system read-only program memory. U21 is a reset circuit and watchdog timer.

9.4.3 Input/Output Control (Figure 2, Appendix A)

Input/Output buffering and control for system peripherals and related equipment, is illustrated on sheet 3 of the schematic drawing (6601-4060).

U25 through U29 are latches that control the printer, liquid crystal display (LCD), four port communication expander, audio multiplexers and relays. U23 controls the On-Air and Alert relays. U22 and U30 provide RS-232 inputs and outputs.

9.5 Left Section Key Pad (Figure 4, Appendix A)

U501, U505. U509, U503, U507 and U511 in series form a 48-bit serial-to-parallel shift register that is used to illuminate the 40 encoder board LEDs. The bits of LED data are shifted in to the keyboard by the I/O control section, above, and then enabled to illuminate or flash the LEDs.

U512, U510, U508, U506, U504 and U502 in series form a 48-bit parallel-to-serial shift register that is used to sense the 41 encoder key switches. The bits of switch data are shifted out of the encoder keyboard by the I/O control section, above, and are then interpreted by the DSP/CPU.

9.6 Right Section Key Pad (Figure 6, Appendix A)

U601 and U603 in series form a 16-bit serial-to-parallel shift register that is used to illuminate the 12 decoder board LEDs. The bits of LED data are shifted in to the keyboard by the I/O control section, and then enabled to illuminate or flash the LEDs.

U604 and U602 in series form a 16-bit parallel-to-serial shift register that is used to sense the ten decoder key switches. The bits of switch data are shifted out of the decoder keyboard by the I/O control section, above, and are then interpreted by the DSP/CPU.

9.7 LCD Display Assembly

The LCD Display Assembly is a 16-character back-lit display with contrast controlled by setup software. The LCD assembly is controlled by the FPGA through an 8-bit parallel data interface at U26 on the main board.

9.8 Digital Voice Recorder (Figure 8, Appendix A)

U3 is a sampling analog-to-digital (A-D) and digital-to-analog (D-A) converter that converts incoming voice messages to digital data and stores the data in memories U5, U6, U7, U8 and U9. U10 and U11 select memory locations for voice storage. To play back a message, U3 retrieves digital data from the memories and converts it back into its original analog form.

U4 and U12 provide audio signal buffering, gain, and Automatic Level Control (ALC).

U2 controls the routing of the audio input and output signals. The FPGA on the main board controls U3 and U2 through an 8-bit parallel data interface at U1.

9.9 Printer

An 24-column ASCII impact printer is controlled by the FPGA through an 8-bit parallel data interface.

9.10 COM Port Expander (Figure 12, Appendix A)

An COM Port Expander provides communication links to external EAS DECODER related equipment such as a character generator or PC controller.

U302 and U303 are Dual Asynchronous Receiver/Transmitters (DUARTs) that convert parallel data to serial data, and vice-versa. They transmit data to and from the main board through an 8-bit parallel interface at U301. They transmit data to COM2 outputs through EIA quad line driver U306. They receive data from COM2 from EIA quad line receiver U305. The DUARTs are controlled by the FPGA on the main board.