Description of GDU325 GSM900/PCS1900 dual band handy cellular phone

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1. Introduction

This document describes the general information of GDU325 GSM900/PCS1900 dual band handy cellular phone (hereafter GDU325), and also describes circuit operation.

1.1 General Specification

- Protocol: GSM Phase 2 compliance
- SIM Application Toolkit: Class 2 compliance
- Frequency Band: GSM 900MHz and PCS 1900MHz
- Speech Codec: Full Rate and Enhanced Full Rate
- Operating Temperature: -10 deg. C to +55 deg. C
- Battery Supply Voltage: (see 1.2)
- RF Power Output Class 4 (2W for GSM900), Class 1(1W for PCS1900)

1.2 Battery

There are four types of batteries can be used for GDU325.

- Starndard Li-ion battery BTL325 (3.8V/700mA)
- Optional Li-ion vibrating battery VTL325 (3.8V/700mA)
- Optional Ni-MH battery BTR325 (3.6V/720mA)
- Optional Ni-MH vibrating battery VTR325 (3.6V/720mA)

1.3 External Interface

GDU325 has there types of external interface

- Earphone Jack

  This is used for connecting hands-free microphone accessory.
- RF Connector

  This is used for measurement purpose only.
- External Interface Connector (including Battery Charger Connector)

  The external interface connector provides user to enable data communication to connect the phone to PC by using optional interface data cable DIC325.

  The battery charger is inserted to the mini-jack part of this connector to charge the battery.

2. Description of Circuit - System Overview

The GDU325 consists of 4 main blocks: RF Interface, Baseband/Audio Interface, GSM Processor and Power Supply System.

3. RF Interface

Figure 1 shows system functional overview of the RF Interface. The transmitter and receiver share local oscillators. The RF and IF Local oscillators are derived by PLLs incorporated in the IC301 from the 13 MHz reference (MX301). The RF Local VCO (MX302) selects the required channels, while all other frequencies required are generated from the IF Local VCO (MX303).

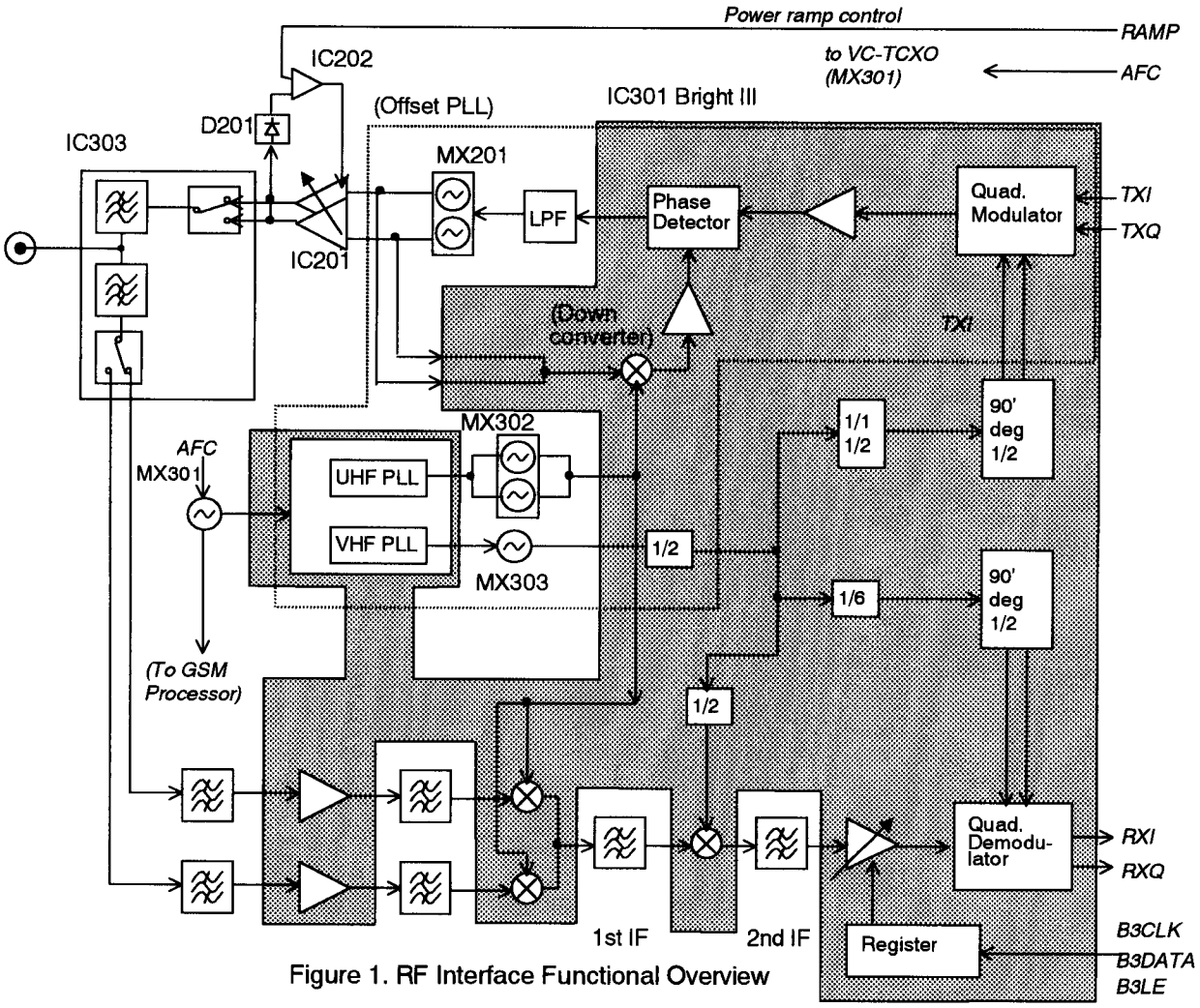

Figure 1. RF Interface Functional Overview

3.1. Bright III (IC301)

The IC301 is a RF transceiver IC designed for GSM900/PCS1900 dual band GSM systems, and integrates most of functions needed for transmitter and receiver.

The Bright III has the following circuit blocks:

- Dual RF LNAs (GSM900 and PCS1900 Band)
- Dual First Mixers, (GSM900 and PCS1900 Band)
- One Second Mixer
- Programmable Gain Amplifier
- IQ Demodulator

- IQ Modulator and Offset PLL
- IF and RF Synthesizer
- Power Mode Controller for each circuit block

3.2. Transmitter

The Baseband/Audio Interface Block generates I and Q baseband signals for the transmit quadrature modulator. This quadrature modulator produces a GMSK modulated 'reference signal' (hereafter IF signal) which passes to the Offset Phase-Locked Loop Block (OPLL). For GSM900 operation, the IF signal frequency is 270 MHz whereas, for PCS1900 operation, the quadrature modulator generates IF signal of 135 MHz.

3.3. Offset Phase-Locked Loop (OPLL)

The OPLL consists of a down-converter, phase detector, loop filter and dual band transmit VCO (MX201) which can operate at either final RF output frequency.

The down converter mixes the RF Local VCO (MX302) with the transmit VCO signal to generate a feedback signal of 270 MHz for GSM900 operation or 135 MHz for PCS1900 operation. The feedback signal passes via a limiter to one port of the phase detector. The GMSK IF signal from the quadrature modulator passes via a second limiter to the other input port of the phase detector.

The phase detector generates an error current proportional to the phase difference between the feedback signal from the down-converter and the IF signal from the quadrature modulator.

The error current is filtered by a second order low-pass filter to generate an output voltage which depends on the GMSK modulation and the desired channel frequency. This voltage controls the transmit VCO (MX201) output frequency which is modulated with the original GMSK data.

The quadrature modulator contains circuitry to maintain the correct sense of the final output modulation with respect to the baseband data. The center frequency of the transmit VCO is offset from the RFLO frequency by 270 MHz for GSM900 operation or 135 MHz for PCS1900 operation. The OPLL acts as a tracking narrowband band pass filter tuned to the desired channel frequency. This reduces the wideband noise floor of the modulation and up-conversion process and provides significant filtering of spurious products.

This OPLL architecture results in a low-noise GMSK modulated signal with very low spurious content.

The RF GMSK outputs from the MX201 are fed directly to the RF Power Amplifier (IC201)

Table 1. RF / IF Local and Tx IF Frequency

Band	Frequency	RF Local	IF Local	Tx IF	Channel
GSM900 transmit	880-915 MHz	1150-1185 MHz	1080 MHz	270 MHz	975-39ch,61-124ch
GSM900 transmit	898-902 MHz	1158-1162 MHz	1040 MHz	260 MHz	40-60ch
PCS1900 transmit	1850-1910 MHz	1715-1775 MHz	1080 MHz	135 MHz	512-668ch,754-810ch
PCS1900 transmit	1882-1898 MHz	1752-1768 MHz	1040 MHz	130 MHz	669-753ch

3.4. Power Amplification : Ramping and Level Control (IC201, IC202, D201)

Dual band Power Amplifier (IC201) is used to amplify the transmit VCO (MX201) output to the final output power. The required output power is +33dBm for GSM900 and +30dBm for PCS1900.

The peak output power level and the profile of the transmitted burst will be controlled via the PA's power control line by means of a closed feedback loop. An AC-coupled RF Detector (D201) is used to sample the RF output from PA.

The output voltage of RF detector is dependent on the incident RF level. This feedback voltage passes to the non-inverting input of the loop integrator (IC202)

A reference voltage "RAMP" is generated from the IC602 of the Baseband/Audio Interface block under control of the Layer 1 software incorporated in the IC601 of the GSM Processor Block. This reference voltage is also summed into the non-inverting input of the loop integrator. The loop maintains zero difference between the sum of the fixed

voltage reference and the temperature compensating voltage on the inverting input, and the sum of the baseband reference signal and feedback voltage on the non-inverting input.

In this way, the amplitude and shape of the transmitted RF burst is controlled by the IC601.

3.5. Antenna Switch (IC303)

The PA output signal is passed to the antenna connector via an integrated dual band Tx/Rx switch module (IC303). The switch module incorporates PIN diode for transmit/receive switches and a passive diplexing network to combine the 900 MHz and 1900 MHz signal paths to a common output. This switch is to be employed to increase the isolation between transmitter circuit and receiver circuit during the PA is not in the active time slot.

3.6. Receiver (F101, F102, F103, F105, F104, IC301)

The IC301 has two first receive mixers, one second receive mixer and two on-chip RF Low-Noise Amplifiers (LNAs) with active bias circuits. The incoming RF signal passes through the antenna switch module to the appropriate receiver front-end amplifier. The two receiver front-end chains comprise a low-loss RF SAW filter (F101 for GSM900, F105 for PCS1900), an on chip LNA and a second RF SAW filter (F102 for GSM900, F103 for PCS1900).

The RF signals from the front-end passes to the first receive mixers within the IC301.

The mixers are implemented as Gilbert cells and the first receive mixer block contains two mixer cells.

The two mixer cells provide high or low conversion gain at 900 MHz, and 1900 MHz. The conversion gain of these mixers are controlled by Layer 1 software incorporated in the IC601 of GSM Processor Block.

The first receive mixer generates a 225 MHz IF signal which passes via a balanced 225 MHz IF SAW filter to the first IF amplifier.

A second internal mixer converts the 225 MHz IF signal down to the 45 MHz second IF signal.

The IF amplifier / second mixer block includes a Gilbert Cell mixer. The gain setting of this mixer is also controlled by Layer 1 software.

The 45 MHz output from the second mixer is filtered and passes to the programmable gain amplifier (PGA).

The gain of PGA is controlled by Layer 1 software incorporated in the IC601 of GSM Processor Block.

The PGA output 45 MHz signal passes to the demodulator and is mixed down to DC signal to generate I and Q baseband signals.

The baseband signals pass via integrated low-pass filters to the baseband A/D converters incorporated in AD6421 Voiceband / Baseband Converter (IC602) in Baseband/Audio Interface Block.

3.7. Automatic Gain Control and Received Signal Strength Measurement

The Layer 1 software controls independently the gain steps in the first receive mixer, second mixer and PGA integrated in the IC301.

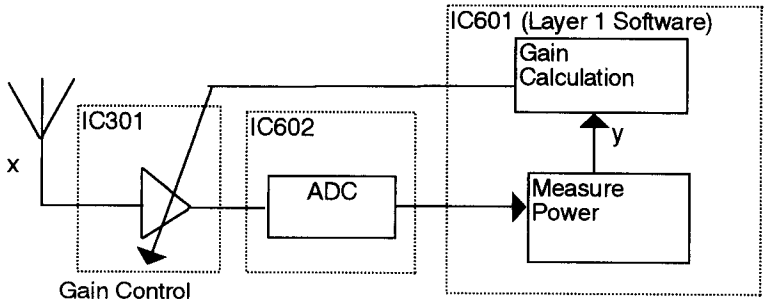

Figure 2 Automatic Gain Control

Figure 2 shows the scheme for Automatic Gain Control (AGC). The IC601 measures the power of the IQ samples passed from the IC602, this power is called "y". The AGC control function of Layer 1 software uses y to calculate

the gains to be set for the IC301, the objective of the control is to set the power of received IQ signal to the IC602 to a fixed level. This calculation is also used for received signal strength indicator (RSSI) measurement.

3.8. RF synthesizer

This is fully integrated part of the IC301 and this is controlled by Layer 1 software incorporated in the IC601 of GSM Processor Block. via serial signal control interface.

It generates the first local oscillator frequency (RF VCO: MX302) for the receiver and the transmitter and is set to the required frequency.

The VCO signal is divided down by a combination of a high-speed dual modulus prescaler and a programmable counters to 200 kHz. This is compared to a 200 kHz reference signal derived from the 13 MHz VCTCXO (MX301).

3.9. IF Synthesizer

This is fully integrated part of the IC301 and this is also controlled by Layer 1 software via serial signal control interface.

It generates the second local oscillator (IF VCO: MX303) frequency for the receiver, and in transmit mode it is divided down to provide the carrier signal for the IQ modulator. The VCO signal is divided down to 1 MHz by a combination of a high-speed dual modulus prescaler and programmable counter. This is compared to a 1 MHz reference signal derived from the 13 MHz VCTCXO. The resulting error signal is filtered by the loop filter and then used to tune the VCO on to the required frequency.

Table 2. RF / IF Local and 1st, 2nd IF for receiver

Band	Frequency	RF Local	IF Local	1st IF	2nd IF
GSM900 receive	925-960 MHz	1150-1185 MHz	1080 MHz	225 MHz	45 MHz
PCS1900 receive	1930-1990 MHz	1705-1765 MHz	1080 MHz	225 MHz	45 MHz

3.10. Reference Oscillator (MX301) & Automatic Frequency Control

The local oscillators share one common 13 MHz frequency reference signal which is provided from an on-board temperature compensated voltage controlled crystal oscillator (MX301 VCTCXO) An AFC control signal is given to the VCTCXO's control input to allow adjustment of the operating frequency. The RF Interface will provide a 13 MHz analogue reference clock output to drive the GSM Processor.

3.11. power mode control

The IC301 includes power mode controller for transmitter path, receiver path, and synthesizers to optimize the power consumption. This functions are controlled by the IC601 via serial interface.

4. Baseband / Audio Interface Block

Figure 3 is a functional block diagram of the Baseband / Audio Interface Block with GSM Processor.

The main parts of the baseband are the chipset which is combination of AD6421 (IC602) and AD6426 (IC601).

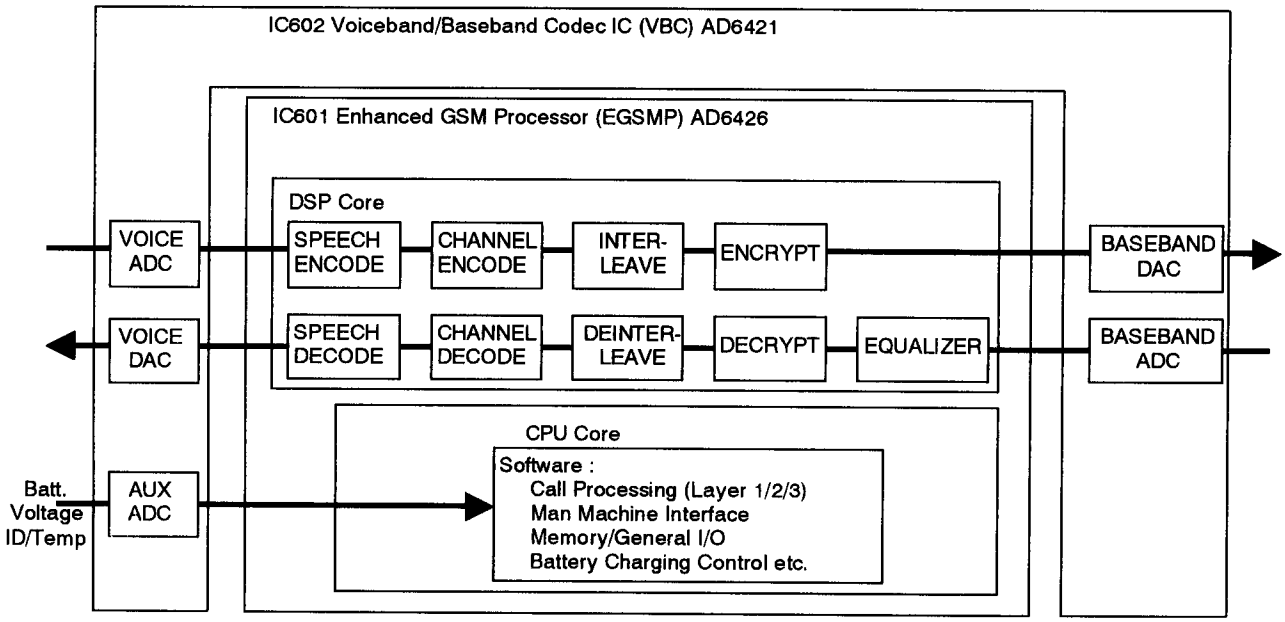

Figure 3. Functional Block Diagram

In this section, the functional interfaces between chipset and other blocks are briefly described as follows;

- Transmit baseband/audio data
- Receive baseband/audio data
- Radio Control System
- Monitoring the battery condition

4.1. Transmit baseband/audio data

4.1.1 Analog-to-Digital Voice Conversion

The microphone (MP401) connected directly to the IC602 provides an analog voice signal input to the multiplexer.

An analog multiplexer selects either the normal (microphone on the phone) or the auxiliary channels (external microphone such as headset) as the input to the sigma-delta ADC circuit.

The ADC samples analog voice signal at 8 kHz rate, producing 13-bit linear values corresponding to the magnitude of the input. The ADC includes all required filtering to meet the GSM specifications. The sampled voice data is passed to IC601 through a Voiceband Serial Port.

The sampled voice data will take the necessary encoding such as Speech CODEC by IC601 and will return to IC602 through a Baseband Serial Port.

4.1.2 GMSK Modulation and D/A Conversion

The IC602 receives baseband data from the IC601 at 270 kb/s. The IC602 uses an on-chip lookup table to perform GMSK modulation. A pair of 10-bit matched differential DACs convert the modulated data and pass I and Q analog data to quadrature modulator integrated on the IC301 which is located on RF Interface Block.

4.2. Receive baseband/audio data

4.2.1 Receive baseband signals - Analog-to-Digital Conversion

The demodulated I and Q signals received from the IC301 are sampled by a pair of ADCs at 270 kHz. The I and Q samples are transferred to the IC601 through a Baseband Serial Port.

The sampled IQ baseband data will take the necessary decoding such as Vitabi-decoding, channel equalization, extracting speech signals by the IC601.

The extracted speech signal - i.e. the receive digital audio signal will return to the IC602 through a Voiceband Serial Port.

4.2.2 Voice Digital-to-Analog Conversion

The Voice DAC function of the IC602 operates at 8 kHz and includes all the needed filtering. The analog signal output level is controlled by PGA and directly drives a earpiece (MP402) as well as a separate auxiliary output.

4.2.3 Auxiliary Audio Signals

[Input Signals]

Auxiliary audio input signals can be input from either a external device or a remote microphone connected to audio jack, or connected to external interface. Input gain can be set to 0 dB or +26 dB.

[Output Signals]

The output signal can be directly connected to an external audio speaker connected to audio jack, or connected to external interface. The output PGA can be programmed for -15 dB or +6 dB.

4.3. Radio Control System Functions

Figure 4 shows the radio control system functions of the IC602.

Following functions are performed by this IC.

- Power Ramp Control
- Automatic Frequency Control (AFC)

4.3.1 Power Ramp Control

To meet the spectrum and time-domain specifications of the transmitted output signal, the transmitted burst signal has to follow a specified power envelope. The envelope for the power profile is originated in IC601 as a set of coefficients, and they are downloaded and stored in the Ramp - RAM configured on IC602.

This envelope profile is fed to the RAMP DAC in the IC602 for each burst signal. The analog output is fed into the Automatic Power Control loop circuit (APC - see section 3.4) as a reference envelope, controlling the power profile and absolute level of the transmitted data.

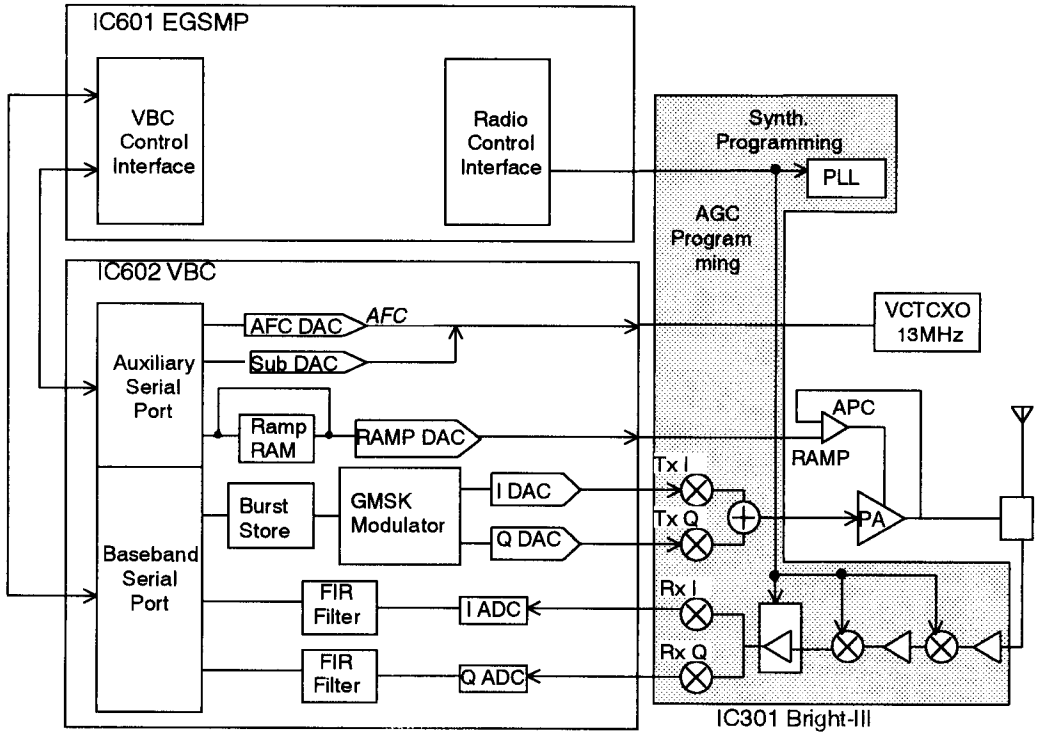

Figure 4. Radio Control System Overview

4.3.2 Automatic Frequency Control (AFC)

The mobile radio tracks the master clock provided form the base station to compensate for temperature/frequency drifts in the crystal oscillator MX301. Drift of the crystal oscillator over time and temperature has to be compensated as well as frequency shifts due to the Doppler effect in case of a mobile radio is moving.

The received signal is analyzed in IC601 and a digital control signal is generated. This signal is sent to the AFC DAC in the IC602 through a Baseband Serial Interface to control the crystal oscillator (MX301 VCTCXO).

4.4. Monitoring the battery condition

GDU325 has battery charging system which is controlled by the software. The auxiliary ADC of IC602 is used to monitor the current status of battery voltage, type of battery attached and temperature of battery.

Figure 5 shows the auxiliary ADC used for monitoring the battery condition.

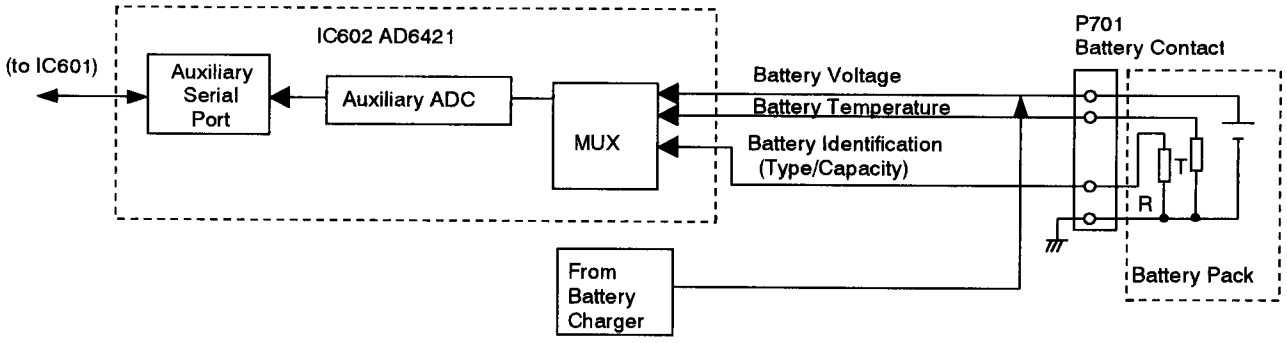

Figure 5. Audio/Auxiliary Section of the IC602 (AD6421 VBC)

5. GSM Processor Block

The main part of this block is IC601 - AD6426 Enhanced GSM Processor (EGSMP).

It combines application specific hardware, an embedded 16-bit DSP and an embedded 16-bit microcontroller (Hitachi H8/300H). It performs channel coding and decoding and executes the protocol stack and Man Machine Interface software. The DSP implements full rate speech transcoding according to GSM specifications. A high performance soft-decision Viterbi equalizer is implemented in the software embedded in the DSP. The embedded microcontroller executes the Layer 1, 2, 3 and user MMI software.

The GSM Processor block has following functional subsystems

- Transmitting voice signal : Speech Coder, Channel Coding
- Receiving baseband signal : Equalizer, Channel Decoding, Speech Decoder
- Generation of Auxiliary Audio Signals
- Digital Audio Interface (DAI)
- Radio Interface to IC602 and RF Interface Block
- SIM Card Interface
- Keypad
- External Memory : FLASH/SRAM, EEPROM
- Display Controller
- Serial Interface to external accessories

5.1. Transmitting voice signal

5.1.1 Speech Codec

IC601 receives the voice data stream from the IC602 through a voiceband serial interface and encodes the data from 104 kb/s to 13 kb/s by this speech codec.

Also IC601 sends the voice data stream which are decoded by this speech codec engine.

The coding algorithm used is Regular Pulse Excitation with Long Term Prediction (RPE-LTP), or Algebric

Code Exitation with Linear Prediction (ACELP) as specified in the 06-series of GSM Recommendations.

5.1.2 Channel Coding

The information received from the speech coder contains parameters that have different levels of priority. These are protected to different levels within the channel coding. The encode protection process incorporates block coding and convolutional encoding. In addition to the normal speech traffic channels, the channel coding function also supports data transmission at full rate and half rate. After the interleave process (if necessary) the data is encrypted using the required A5/1 or A5/2 encryption algorithm. Data is then formatted into bursts, with the required timing and training sequences, and sent to the IC602 through a baseband serial port.

5.2. Receiving baseband signal

5.2.1 Equalizer

The equalizer recovers and demodulates the received signal and establishes local timing and frequency references for the mobile unit as well as RSSI calculation. The equalization algorithm is a version of the Maximum Likelihood Sequence Estimation (MLSE) using the Viterbi algorithm. Two confidence bits per symbol provide additional information about the accuracy of each decision to the channel codec's convolutional decoder. The equalizer outputs a sequence of bits including the confidence bits.

5.2.2 Channel Decoding

Data is decrypted as required, using the A5/1 or A5/2 decryption algorithm prior to the deinterleave process. The deinterleave process is an exact inversion of the interleave process used by the transmit section. The decode function then performs convolutional decoding and parity check. The convolutional decoder uses a Viterbi algorithm, with two soft decision confidence bits supplied by the equalizer. Error control mechanisms are used to ensure adequate bad frame indication.

5.2.3 Speech Codec

Encoded speech data is transferred at 20 ms intervals in blocks of 260 bits plus the Bad Frame Indicator (BFI). The speech decoder supports a Comfort Noise Insertion (CNI) function that inserts a predefined silence descriptor into the decoding process. IC601 also implements control of talker sidetone and short term echo cancellation. The resulting data, at 104 kb/s, is transferred to the IC602 through a voiceband serial interface.

5.3. Generation of Auxiliary Audio Signals

Under the control of Layer 1 software running on IC601, IC601 can generate a variety of fixed and user-programmable tones. This includes all standard DTMF and Call Progress tones as well as user defined tones. The tone structure can consist of up to four frequency components with individual durations. IC601 also generates Talker Sidetone as specified in the GSM recommendations.

5.4. Digital Audio Interface (DAI)

As required by the GSM specifications, a digital audio interface is provided to allow Acoustic Testing of the phone. The voiceband serial interface is used as DAI, and it is activated in one of the test modes. The external DAI Box should be needed for the testing.

5.5. Radio Interface to IC602 and RF Interface

5.5.1 Automatic Gain Control (AGC)

The mobile radio has to cope with a wide range of input signal levels. The major part of the overall gain is provided in the IF amplifier in the RF Interface Block. The incoming signal level is analyzed in IC601. And IC601 send a digital gain control signal to the first downconverting mixer, second IF mixer, and Programmable Gain Amplifier (PGA) embedded in Bright III on the RF Interface Block (IC301 - see section 3.7). The PGA amplifies the appropriate analog IQ Output for the IC602 (Baseand / Audio Interface Block stage).

5.5.2 Synthesizer Control

IC601 and the respective parts of the Layer 1 software control the overall timing and frequency generation of the RF Interface Block. The control signals such as counter values, divide ratio, power consumption bit etc, are provided from IC601.

5.6. SIM Card Interface

IC601 is designed to interface directly to the SIM. However, the subsystem of IC605 is used for voltage level conversion interface to support both 3V and 5V types of SIM.

The SIM Interface subblock implemented in IC605 provides power conversion and level shifting needed for to interface with either 3V or 5V Subscriber Identity Modules (SIMs).

Input voltage for IC605 is 3 V to 7 V, allowing direct connection to the battery.

This subblock contain a charge pump DC/DC converter that delivers a regulated 5 V or 3 V to the 5V / 3V SIM card respectively.

IC601 can control the output voltage needed SIM voltage either 3 V or 5 V, dependent on SIM type.

5.7. Keypad

Eighteen-key Keypad interface logic is provided on IC601.

5.8. External Memory

5.8.1 FLASH/SRAM

The IC603 FLASH/SRAM Stacked Chip Size Package (CSP) memory contains all programs and data for the embedded Control Processor of IC601. The address and data buses are shared by each memory.

The complete GSM protocol software as well as the Man-Machine Interface Software will be loaded onto FLASH ROM. To support FLASH memory, IC601 provides embedded bootstrap program to download the software into the FLASH memory via External Interface Connector (PJ601).

In addition, the Control Processor also uses SRAM to store user-defined variables, typically those used by the Protocol Stack or Application Layer.

5.8.2 EEPROM

IC601 provides separate pins to interface directly to an external serial EEPROM (IC606) via a serial bus. This EEPROM is typically used for the storage of such as calibration data or user definable MMI control parameters.

The total size of the EEPROM is 8Kwords X 8 bits

5.9. Display Controller

IC601 provides separate pins to interface directly to an display controller. (H801 LCD)

This interface consists of 5 signals: DISPD0, DISPA0, DISPEN, DSPCLK, LCDRESET. One backlight pin with PWM control is provided by IC601 to control brightness of backlight LED.

5.10. Serial Interface to external accessories

The External Interface Connector (PJ601) is directly connected to IC601. This interface is not only used for downloading the software into FLASH, but also used for data communication line like RS232 serial interface between host controller and handset.

6. Power Supply/Battery Charger Block

6.1. Power Management System ADP3401

The ADP3401 (IC605) is a multifunction power management system IC. The IC605 contains the following several blocks:

- Four Low Dropout Regulators (LDOs)
- Reset signal Generator

- Power-On/-Off Logic
- Undervoltage Lockout
- SIM Interface Logic Level Translation (3 V/5 V)
- SIM Voltage Supply

6.2. Power Supply for IC605

The input voltage range for IC605 is 3 V to 7 V and regulated by four LDOs to supply powers to sub-blocks of the handset.(i.e. Digital, Analog, TCXO, Backup battery for Real-Time Clock)

6.2.1 Low Dropout Regulators

Four LDOs can be controlled by following state;

- A power key has been pressed: PWRKEYIN is activated
- To hold the power supply, PWRON has been enabled by GSM Processor
- Battery charger has been adopted : CRGPWRON is activated
- To wake the analog circuitry, GSM Processor has activated ANLGON

6.2.2 Digital LDO

The digital LDO (V28D) can regulates 100mA which is sufficient to supply all the digital circuitry in the GDU325 (GSM Processor, Baseband/Audio Interface, FLASH/SRAM/EEPROM, LCD, etc).

6.2.3 Analog LDO

The analog LDO (V28A) has the same features as the digital LDO. V28A is rated to 130 mA load which is sufficient to supply the complete analog section of a Baseband/Audio Interface. The analog LDO and the TCXO LDO can be controlled by ANALOGON.

6.2.4 XTAL OSC LDO

The XTAL OSC LDO (V28-TCXO) is intended as a supply for the temperature-compensated crystal oscillator. The output current is rated to 5 mA for this LDO.

6.2.5 RTC LDO

The RTC LDO (V29-RTC) charges a rechargeable coin cell to drive the real-time clock module. It is also used to charge Manganese Lithium battery (BT701).

Figure 5 shows the use of V29-RTC with IC601 which is a part of the GSM Processor block.

The IC605 supplies current both for charging the coin cell and for the RTC module when the digital supply is off.

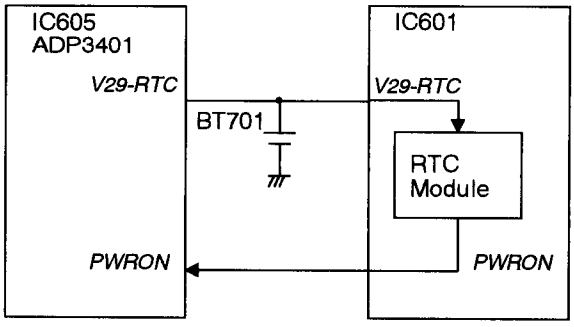

Figure 5.Connection of V29-RTC

The nominal charging voltage for the coin cell is 2.85V.

Since this LDO is running all the time, it features a very low quiescent current (10 uA) even when the handset is switched off.

It also has reverse current protection which is needed when the main battery is removed and the coin cell supplies the RTC module.

6.2.6 Undervoltage Lockout (ULVO)

The UVLO function in the IC605 prevents startup when the initial voltage of the main battery is below the 3.0 V threshold. If the battery is this low with no load, there will be little or no capacity left.

When the battery is greater than 3.0 V, as with the insertion of a fresh battery, the UVLO comparator trips, the RTC LDO is enabled, and the threshold is reduced to 2.9 V. This allows the handset to start normally until the battery voltage decays to 2.9 V open circuit.

Once the 3.0 V threshold is exceeded, the RTC LDO is enabled.

If, however, the backup coin cell is not connected, or is damaged or discharged below 1.5 V, the RTC LDO will not start on its own.

In this situation, the RTC LDO will be started by enabling the Digital LDO. Once the system is started, i.e., the phone is turned on and the Digital LDO is up and running, the UVLO function is entirely disabled.

The IC605 is then allowed to run down to very low battery voltages, typically around 2 V.

The battery voltage is normally monitored by the microprocessor and usually shuts the phone off at around 3.0 V. If the phone is off, i.e., the Digital LDO is off, and the battery voltage drops below 2.9 V, the UVLO circuit disables startup and the RTC LDO.

6.3. RESET

IC605 contains reset circuitry that is active both at power-up and at power-down. RESET is held low at power-up. An internal power-good signal starts the reset delay.

The delay is set by an external capacitor (C707) which produces an appropriate reset time.

At power-off, RESET will be kept low to prevent any spurious microprocessor starts.

6.4. Battery Charger IC Si9731 (IC702)

6.4.1 Battery Charging

IC702 is battery charger IC and it is controlled by the charging software incorporated in IC601.

The "CHRGEEN" of IC601 is connected to charging control circuit incorporated in IC702. The charging will be started when CHRGEEN becomes High.

IC702 is able to charge Li-Ion and Ni-MH type batteries. To identify the type of battery which is attached to the handset, AD converter of IC602 measures ID terminal voltage (BATIDENT) of battery contact (P701), and the measurement value will be identified by the software of IC601.

IC702 can be switched to the following by the type of battery:

- Constant voltage charging in case of Li-Ion battery
- Constant current charging in case of Ni-MH battery

Charging mode switch is made by "CVMODE" of IC601. CVMODE is connected to the charging control circuit incorporated in IC702.

Table 3. Battery Charging Control Line and Switching of Charging Mode

Line	Logic Level	
	Low	High
CHRGEEN	Stop Charge	Start Charge
CVMODE	Constant Current Mode (for Ni-MH)	Constant Voltage Mode (for Li-Ion)

6.4.2 Overcharge Protection

When voltage of 12.8V or greater is applied to "VCHARGE" due to such as damage to Battery Charger, overvoltage protection circuit of IC702 becomes activated and the charging will be stopped.

When the battery become heated due to overcharging, etc., and the battery temperature reaches 50 degrees Centigrade, the battery temperature is detected by converting thermistor resistor value in the battery pack to AD by IC602. And the charging will be stopped.

When charging control becomes impossible due to phone damage, etc. and the battery is heated by overcharging, battery cell will be protected by Thermal fuse in the battery pack and PTC.

Thermal fuse : 98 degrees Centigrade (Operating temp.)
PTC : Ih=2.1A / It=4.7A at 25 degrees Centigrade

7. Appendix: Revision History

Date	Revision	Detail
01/02/27	V1.0	Prepared for Type Approval Test for Hardware Version 1.0