User Manual (LGSRFT1 / LGSRFR1)

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User Manual

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Contents

1 Introduction

This document describes functionality and electrical specification of LGSRFT1 and LGSRFR1. LGSRFT1 together with LGSRFR1 can transmit and receive 16 Gbps data through 60 GHz ISM band wirelessly. With this ultra-high throughput, it can implements 4K wireless video transfer between main SoC and display panel. It is possible to remove every wire attached to TV display and to make customer use living space more freely.

1.1 Overview and Feature of LG2831

LG wireless AV transfer solution (LGSRFT1 + LGSRFR1) consists of 'LG2831 and LG2851' module. It implements wireless data transaction between main SoC and T-Con or FRC instead of Vx1 wired connection. LG2831 is responsible for video/audio data reception from main SoC and regeneration of received data through wireless channel to T-Con or FRC. In case of LG2851, it receives data through 10 GHz wired connection from LG2831 and transmits data through 60GHz wireless channel in box side. In case of display panel, it will do the reverse function of box side.

The main functions of LG2831 are audio/video data reception from main SoC and regeneration to T-Con or FRC, video data compression/decompression with visually lossless quality, making-up wireless transaction protocol and analog-to/from digital conversion to communicate with LG2851.

It supports 4K60p and 4K120p video frame through Vx1 interface. It also supports variable refresh rate of video frame. It supports 32-lane Vx1 interface. It will use 16 lanes of Vx1 for 4K video transaction and use16 or24 lanes of Vx1 for 8K video. In case of 8K application, LG2831 support OSD and PIP stream in addition to main video frame. For this case, another 8 lanes of Vx1 is used. The supported OSD streams are 4K 60p and 2K 60p. In case of PIP, only 2K60p format is allowed. In case of audio, it supports 7.1 channels up to 96 kHz sampling data.

In a view point of data stream, main SoC located at box side processes audio/video data from external input and provide it to LG2831. After receiving video data, LG2831 compresses it with ratio from 4:1 to 30:1. Up to 6:1 compression rate, it can achieve visually lossless image and provide better quality of video to customer. The compressed data is handled by wireless protocol IP, packetized and formatted for wireless transmission through LG2851. To communicate with LG2851, LG2831 has analog interface which can convert digital signal to 10 GHz analog signal.

At the other end, i.e, display side, LG2851 receives 60 GHz radio signal and converts to 10 GHz analog signal to LG2831. After receiving analog signal from LG2851, LG2831 do reverse functions as described above.
For unpredicted radio condition during transmission, the modem protocol IP measures radio quality and control MCS for each packet. In addition, LG2831 will control compression rate of video data for more reliable wireless communication.

LG2831 module provides the following key features:

- **Host Processor**

- Cortex-R5 with 480 MHz core clock frequency
- Icache: 32 KB, Dcache: 32 KB
- I-TCM: 32 KB, D-TCM: 32 KB
- SRAM : 832 KB

- **Flash Memory Interface**

- Support Quad-SPI flash memory
- Max size is 16 MB

- Support up to 60 MHz

- **Peripherals**

- GPIO: Dedicated 10 ports, Shared 49 ports
- UART: Dedicated 1ports, support up to 921.6 Kbps
- I2C: 1 slave, 5master/slave
- SPI: 1 master/slave for interface with F20 or F22

- **Video I/F (Vby1 24-lane)**

- Video Inputs
  · Main Video :
  : Up to 4K 120Hz 10bits, 8K 60Hz 420 10bits or 8K 60Hz DSC compressed with Vby1 16 lanes
  · OSD/PIP :
  : Support 4K OSD/2K PIP with Vby1 8 lanes
  · Control Data Inputs
  : support customized packet data interface using Vby1 control channels
- Video Output
  · Main Video :
  : Up to 4K 120Hz 10bits, 8K 60Hz 420 10bits or 8K 60Hz DSC compressed with Vby1 16 lanes
  : 8K60p 444 10bits with Vby1 24 lanes with 5-byte mode and customized format
  · OSD/PIP :
  : Support 4K OSD/2K PIP with Vby1 8 lanes

- **Video Compression**

- Video
  · Support RGB/YUV444, YUV420 8/10/12 bit format
  · Support up to 4K120Hz or 8K60Hz
  · Compression ratio : 1/4 ~ 1/30 for 4K video, 1/4~ 1/30 for 8K video
- OSD
  · Support ARGB444 32bit format
  · Support up to 4K60Hz or 2K60Hz
  · Compression ratio : 1/4 ~ 1/30

- **HDCP**

- HDCP 2.3 on LG interface

- **Audio I/F**

- Up to 7.1 ch I2S channel transfer (L/R, Sub L/R, Center/LF, Reverse L/R)
- 48/96 kHz, 32 bit

- **Wireless Protocol**

- IEEE 802.11ay based customized format
- Frequency : 57.24 ~ 65.88 GHz
- Bandwidth : 4.32 GHz
- Transmission mode : Control mode, single-carrier mode
- Antenna & MIMO : Single antenna with beamforming
- Data-rate : up to 16.17Gbps

- **RFIC I/F**

- Frequency : 10.56 GHz
- Timely-multiplexed operation : 2 Receiver mode and 2 Transmission mode
- Reference clock output to RF-FE IC (KASI) : 330MHz
- Customized control interface with RF-FE IC (KASI)

- **Package**

- fcBGA: 416 balls
- Ball pitch/size: 0.8/0.45 mm
- Body size: 19x19 mm2

- **Clock**

- Requires external 24 MHz Crystal, 48 MHz TCXO

- **Power**

- 3.3V/1.8V/1.2V/1.0V/0.9V

1.2 Feature of LG2851

LG2851 module is 60GHz mmWave RF front-end module using mmWave RFIC and is supporting the 57.24 – 65.88GHz frequency range and supports 4.32 GHz channel bandwidth. The module includes RX and TX functions needed for signal conversion between the intermediate 10.56GHz frequency and mmWave frequency. Patch, dipole and monopole antennas for the air interface and antenna control functions to form and steer the antenna beam. LG2851 has been designed to be used with LG2831 base-band chip for main application being 4k wireless TVs.

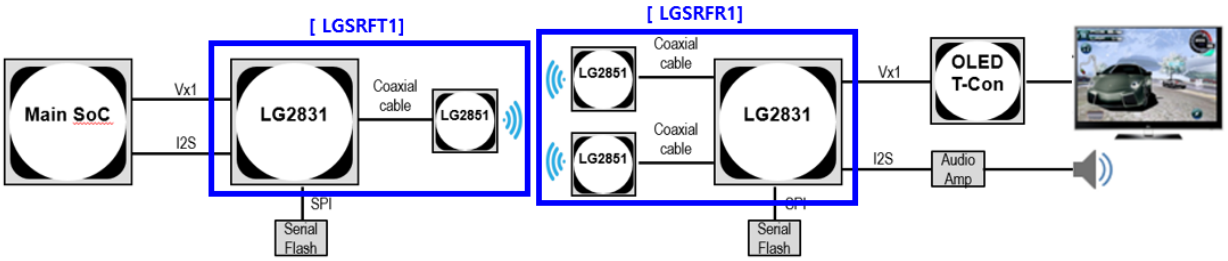
Main features for the LG2851 module are:

- RF frequency range from 57.24 to 65.88 GHz
- Support for 4.32 GHz bandwidth
- Support of BPSK, QPSK, 16-QAM and 64QAM modulations
- COAX-interface between LG2851 and LG2831 combining
    - 330 MHz reference clock
    - 2.64 GHz KIF-control interface for 220 Mbps control data rate
    - 10.56 GHz IF data frequency
- 32 RF inputs and outputs with configurable phase and on-chip combining network to operate beam-forming in RX and TX direction.
- Independent power up/down and bias control for each line-up to support multiple difference module configurations with different antenna arrangements.
- On-chip power detectors and configurable biasing to sense and accurately control the output power of the device
- Simple and fast chip control through programmable trigger commands, both for mode changes and beam steering.

Module is operated from single 5V supply and contains two DCDC converters and two linear regulators to generate power supplies for the LG2851 RFIC.

1.3 Application Example

The figure below shows an example of 4K 120Hz wireless TV application of LGSRFT1 and LGSRFR1.



[Figure 1-1] 'LGSRFT1' and 'LGSRFR1' Use Case for 4K 120Hz Wireless TV System

It shows that 4K 120Hz wireless TV System with LG2831and LG2851. Main SoC receives all external inputs and send video/osd to LG2831. LG2831 sends manuplated data to LG2851. LG2851 transmits data through wireless channel and receives it at LGSRFR1. At the other end, i.e., LGSRFR1, LG2831 processes and regenerates video and audio data, sending them to FRC.

2 Electrical Specifications

This chapter describes the electrical specifications of LG2831 and LG2851 module, including recommended operating power conditions, recommended operating power ripple conditions, and system power-up sequence.

2.1 Absolute Maximum Ratings for LG2851

The absolute maximum ratings describe the maximum conditions in which the device can be operated without risk of temporary or unrecoverable failure of the device. Compliancy with the electrical specifications or reliability requirements is not guaranteed if any of these conditions are violated.

[Table 2-1] Absolute maximum ratings for supply pins

Parameter	Description	Min	Typ	Max	Unit
	Maximum voltage VDD pins (5.0V)			5.5	V
	Maximum Junction temperature	0		100	deg
	Maximum current draw (32TX)			1.5	A

[Table 2-2] Absolute maximum ratings for signal pins

Parameter	Description	Min	Typ	Max	Unit
	Maximum RF input power without breaking device			+10	dBm

[Table 2-3] ESD maximum ratings

Parameter	Description	Min	Typ	Max	Unit
	All pins except RF pins (HBM)	2000			V
	RF pins (HBM)	1000			V

[Table 2-4] Storage conditions maximum ratings

Parameter	Description	Min	Typ	Max	Unit
	Storage Temperature	-55		125	°C
	Humidity	5		95	%

2.2 Operating Conditions for LG2831

Followings are recommended operating power conditions and temperature conditions for LG2831.

[Table 2-5] Recommended Operating Power Conditions

Parameters			Min.	Typ.	Max.	Units
DVDD33_XTAL		3.3V Xtal Power Supply	3.0	3.3	3.6	V
DVDD33 AVDD33_USB20		3.3V Digital Power Supply	3.14	3.3	3.47	V
AVDD18_C4TX AVDD18_VRX AVDD18_PLL VQPS		1.8V Vx1 Power Supply	1.71	1.8	1.89	V
AVDDT_C4TX		C4TX Termination Supply	1.71	1.8	1.89	V
AVDD18_RF_COM AVDD18_RF0_RX AVDD18_RF1_RX AVDD18_RF0_TX AVDD18_RF1_TX AVDD18_RF_PLL		1.8V RF Power Supply	1.75	1.8	1.90	V
AVDD12_RF_COM AVDD12_RF_TXDAC AVDD12_RF0_RXADC AVDD12_RF1_RXADC AVDD12_RF_VCLK24M		1.2V RF Power Supply	1.15	1.2	1.26	V
DVDD10_RF_DFE	V3	1.0V RF Power Supply (AVS initial, TBU)	0.99	1.02	1.05	V
	V2		0.94	0.97	1.00	
	V1		0.89	0.92	0.95	
DVDD09	V3	0.9V Core Power Supply (AVS initial, TBU)	0.91	0.94	0.97	V
	V2		0.87	0.90	0.93	
	V1		0.83	0.86	0.89	
ADVDD09_PLL ADVDD09_VRX		0.9 V Power for C4TX PLL 0.9 V Power for Equalizer	0.85	0.90	0.95	V

[Table 2-6] Recommended Operating Temperature Conditions

	Parameters	Min.	Typ.	Max.	Units
	Ambient Temperature	-10		+50	°C

2.3 Operating Conditions for LG2851

When the device is operated within these conditions the full functionality is guaranteed and electrical specifications and reliability targets are met. Unless otherwise noted in subsequent sections.

[Table 2-7] Supply voltages

Parameter	Description	Min	Typ	Max	Unit
	VDD supply (5.0V)	5		5.5	V

[Table 2-8] Normal Operating Temperature Conditions

Parameter	Description	Min	Typ	Max	Unit
	Ambient Temperature	-10		+50	°C

3 Pin Descriptions

LG2831 and LG2851 module includes many digital / mixed IPs. This chapter describes ball map, power supply pins, and functional pins of the chip

3.1 Pin Description for LG2831

3.1.1 Power Supply Pins

Power types can be categorized as follows.

• Normal Power for Active mode operation

- DVDD33 → 3.3V Power Supply for I/O
- DVDD33_XTAL → 3.3V Power Supply for Crystal Oscillator
- AVDD33_USB20 → 3.3V Power Supply for USB 2.0
- AVDD18_* → 1.8V Power Supply for Mixed-IP
- AVDDT_C4TX → 1.8V Power Supply for Vx1-Tx(C4TX) Termination
- VQPS → 1.8V Power Supply for eFuse
- AVDD12_* → 1.2V Power Supply for RF-IP
- DVDD10_* → 1.0V Power Supply for RF-IP
- DVDD09 → 0.9V Power Supply for Digital Core
- AVDD09_* → 0.9V Power Supply for Mixed IP
- DVDD09_XTAL → 0.9V Power Supply for Crystal Oscillator
- GND → Ground

The following tables provide detailed pin descriptions.

1. Digital Power Supply (3.3V)

Type	Counts	Ball No.	Description
DVDD33	4	F13,F14,V13,V14	Digital 3.3V Power Supply for I/O
DVDD33_AON_XTAL	1	F17	Digital 3.3V Power Supply for Always On Domain and Crystal Oscillator

2. Analog Power Supply (3.3V)

Type	Counts	Ball No.	Description
AVDD33_USB20	1	F12	3.3V Power Supply for USB 2.0

3. Digital Power Supply (1.8V)

Type	Counts	Ball No.	Description
VQPS	1	F18	1.8V Power for eFuse OTP Programming (secure boot)

4. Analog Power Supply (1.8V)

Type	Counts	Ball No.	Description
AVDD18_C4TX	3	H8,J8,K8	Analog 1.8V Power for C4TX
AVDDT_C4TX	3	H9,J9,K9	1.8V Power Supply for Vx1-Tx(C4TX) Termination
AVDD18_RF0_RX	1	T8	Analog 1.8V Power for RF-IP
AVDD18_RF1_RX	1	M8	Analog 1.8V Power for RF-IP
AVDD18_RF0_TX	1	R8	Analog 1.8V Power for RF-IP
AVDD18_RF1_TX	1	N8	Analog 1.8V Power for RF-IP

AVDD18_RF_COM	1	P8	Analog 1.8V Power for RF-IP
AVDD18_VRX	4	M18,N18,P18,R18	Analog 1.8V Power for Vx1-RX
AVDD18_PLL	1	F10	Analog 1.8V Power for PLL
AVDD18_RF_PLL	1	R9	Analog 1.8V Power for RF-IP

5. Analog Power Supply (1.2V)

Type	Counts	Ball No.	Description
AVDD12_RF0_RXADC	1	T10	Analog 1.2V Power for RF-IP
AVDD12_RF1_RXADC	1	M10	Analog 1.2V Power for RF-IP
AVDD12_RF_TXDAC	1	N10	Analog 1.2V Power for RF-IP
AVDD12_RF_COM	1	P10	Analog 1.2V Power for RF-IP
AVDD12_RF_VCLK24M	1	L10	Analog 1.2V Power for RF-IP

6. Digital Power Supply (1.0V)

Type	Counts	Ball No.	Description
DVDD10_RF_DFE	5	M11,N11,P11,R11,T11	Digital 1.0V Power for RF-IP

7. Digital Power Supply (0.9V)

Type	Counts	Ball No.	Description
DVDD09	17	H11,H13,J11,J13,K11,K13,K15,L13,L15, M13,M15,N13,N14,P13,R13,T13,T14	Digital 0.9V Power for CORE
DVDD09_XTAL	1	F16	Digital 0.9V Power for Crystal Oscillator
DVDD09_AON	2	H16,J16	Digital 0.9V Power for Always On Domain

8. Analog Power Supply (0.9V)

Type	Counts	Ball No.	Description
AVDD09_PLL	1	F9	Analog 0.9V Power for PLL
AVDD09_VRX	4	M16,N16,P16,R16	Analog 0.9V Power for Vx1-RX

9. Ground (0V)

Type	Counts	Ball No.	Description
GND	119	B23,C11,D11,D12,D17,D20,D21,E5,E7,E8 ,E9,E10,E12,E19,F5,F6,F7,F15,F19,G5,G1 8,G19,H5,H12,H14,H15,H18,H19,J5,J6,J1 0,J12,J15,J18,J19,K6,K10,K12,K18,K19,L5 ,L6,L8,L9,L11,L12,L14,L16,L18,L19,M5,M 6,M12,M14,M19,N5,N6,N12,N15,N19,P 5,P6,P12,P15,P19,R5,R6,R10,R12,R15,R1 9,T2,T3,T4,T5,T6,T9,T12,T15,T16,T18,T19 ,U2,U3,U4,U5,U19,V2,V3,V5,V6,V7,V8,V 9,V10,V11,V12,V15,V16,V19,W1,W2,W3, W5,W16,W17,W18,W19,Y3,Y17,AA2,AA 3,AA17,AB2,AB3,AB4,AB17,AC4,AC17, E20, E21, E22, E23, F20, F21, F22, F23…	Analog / Digital Ground for All Power Domain.

3.1.2 Functional Pins

Pin types can be categorized as follows.

- I → Input. Must be applied as required.
- I,0 → Input. If not used, needs to be pulled-down.
- I,1 → Input. If not used, needs to be pulled-up.
- IS → Input with Schmitt triggered.
- IU → Input with internal pull-up resistor. Do not need external pull-up or down.
- ID → Input with internal pull-down resistor. Do not need external pull-up or down.
- IDS → Input with internal pull-down resistor and Schmitt triggered. Do not need external pull-up or down.
- O → Output
- OZ → Tri-state Output
- IO → Bidirectional. Must be applied as required.
- IO(I) → Bidirectional. The default value is input.
- IO(O) → Bidirectional. The default value is output.
- IOU → Bidirectional, input with internal pull-up resistor.
- IO,0 → Bidirectional. If not used, pull-down may be required.
- IO,1 → Bidirectional. If not used, pull-up may be required.
- OZD → Tri-state Output with input and internal pull-down resistor.
- OD → Open Drain.
- AI → Analog Input.
- AO → Analog Output.
- AIO → Analog Input/Output.

Note

When you do not use any pins in your applications, the input and bi-directional pins which do not have an internal pull-up or down resistor should be implemented by external pull-up or down resistor.

- Here are some information for designing test / evaluation boards.
- Pull-up and pull-down resistors are used to retain unused or un-driven inputs in an appropriate state. The recommended pull-up value of 4.7 kΩ to VDD33 (+3.3V) or VDD18 (+1.8V) and pull-down value of same value, applies only to individually terminated signals.
- To prevent possible damage to the device, I/Os capable of becoming outputs must never be tied together and terminated through a common resistor.
- The GPIO shared pins are all 'Bidirectional pin' and possible to control Input / Output polarities.

Pin lists are described by classifying into categories. Those are digital interface pins, analog interface pins. Following sections provide detailed pin descriptions.

3.1.2.1 Digital Interface Pins

Digital pins include categories as below (Total 91 pins):

- System Clock (2 balls)
- IC Operational Mode Signal (7 balls)

- Power-ON Reset (1 ball)
- SPI (Serial Peripheral Interface) – 3 ports (14 balls) / GPIO shared (8 balls)
- UART Interface -- 1 ports (2 balls)
- JTAG Interface -- 2 ports (10 balls) / GPIO shared (8 balls)
- I2C Interface -- 8 ports (16 balls) / GPIO shared (8 balls)
- PWM Interface for LCD Backlight Control (2 balls) / GPIO (2 balls)
- Local Dimming Control (12 balls) / GPIO shared (12 balls)
- Digital Audio Input/Output Interface (7 balls) / GPIO shared (2 balls)
- HDCP Interface (8 balls) / GPIO shared (8 balls)
- GPIO Interface -- Dedicated (10 balls)

The following tables provide detailed pin descriptions.

System Clock (2 balls)

Name	Pin(s)	Type	Description
Xin	A22	I	Input (24MHz) This should comprise the RC network externally. It provides the clock source for internal System PLL and Core.
Xout	B22	O	

* **Crystal Specification**

Parameter	Value	Unit
Nominal Frequency	24	MHz
Oscillation Mode	Fundamental	
Load Capacitance (CL)	8	pF
LG2831 Frequency Tolerance (25°C)	±30	ppm
Effective Series Resistance	40Ω Max	ohm
Operation Temperature Range	-20~+95	°C
Crystal input swing	> 800	mV

IC Operational Mode Signal (7 balls) / GPIO shared (1 ball)

Name	Pin(s)	Type	Description
opm	C23	I	This signal is for selecting operation mode of the device. This pin should be tied to GND in operation mode.
wakeup_reset_n	C22	I	Wake Up Reset for Non Always On Block (Active Low)
tvon_out	E18	O	TV On Mode Operation Indication
tvon_in	D19	I	TV On Mode or TV OFF Mode Selection
tx0rx1	E17	I	TX Mode or RX Mode Selection
tx_start_tick	AA7	IO	TX Operation Start
hdcp_statvector_sel	Y16	I	Setting the boot mode
			0 : Serial Flash Boot (Rom Boot) 1 : IRMA/DRMA Boot

Power-ON Reset (1 ball)

Name	Pin(s)	Type	Description
pores_n	D18	I	Power-On Reset (Active Low)

SPI (Serial Peripheral Interface) – 3 ports (14 balls) / GPIO shared (8 balls)

Name	Pin(s)	Type	Description
spi_clk_ms	A19	IO	SPI Slave Interface (Clock)
spi_cs_ms	B19	IO	SPI Slave Interface (Chip Select)
spi_di_ms	C19	IO	SPI Slave Interface (Data Input)
spi_do_ms	C20	IO	SPI Slave Interface (Data Output)
spi_clk_mf	C18	O	SPI Master Flash Memory Interface (Clock)
spi_cs_mf	A21	O	SPI Master Flash Memory Interface (Chip Select)
spi_d0_mf	B21	IO	SPI Master Flash Memory Interface (Data Input/Output)
spi_d1_mf	C21	IO	SPI Master Flash Memory Interface (Data Input/Output)
spi_d2_mf	A18	IO	SPI Master Flash Memory Interface (Data Input/Output)
spi_d3_mf	B20	IO	SPI Master Flash Memory Interface (Data Input/Output)
spi_clk_mf_hdcp	C13	IO	SPI Master HDCP Interface (Clock)
spi_cs_mf_hdcp	B14	IO	SPI Master HDCP Interface (Chip Select)
spi_di_mf_hdcp	B15	IO	SPI Master HDCP Interface (Data Input)
spi_do_mf_hdcp	C14	IO	SPI Master HDCP Interface (Data Output)

UART Interface -- 1 ports (2 balls)

Name	Pin(s)	Type	Description
uart0_rxd	AC8	I	UART0 Interface Receive Data
uart0_txd	AB8	O	UART0 Interface Transmit Data

JTAG Interface -- 2 ports (10 balls) / GPIO shared (8 balls)

Name	Pin(s)	Type	Description
jtag_tck_hdcp	W6	I	JTAG Interface Test Clock for HDCP
jtag_tms_hdcp	W7	IO	JTAG Interface Test MODE Select for HDCP
jtag_trst_hdcp	Y5	IO	JTAG Interface Test Reset for HDCP
jtag_tdi_hdcp	Y6	IO	JTAG Interface Test Data In for HDCP
jtag_tdo_hdcp	Y7	IO	JTAG Interface Test Data Out for HDCP
jtag_tck_cpu	Y13	I	JTAG Interface Test Clock for CPU
jtag_tms_cpu	Y14	IO	JTAG Interface Test MODE Select for CPU
jtag_trst_cpu	W14	IO	JTAG Interface Test Reset for CPU
jtag_tdi_cpu	Y15	IO	JTAG Interface Test Data In for CPU
jtag_tdo_cpu	W13	IO	JTAG Interface Test Data Out for CPU

I2C Interface -- 8 ports (16 balls) / GPIO shared (8 balls)

Name	Pin(s)	Type	Description
sda0_ms	D16	IO	I2C Interface Data must be Pull-Up
scl0_ms	E16	IO	I2C Interface Clock must be Pull-Up
sda1_ms	AB14	IO	I2C Interface Data must be Pull-Up
scl1_ms	AC14	IO	I2C Interface Clock must be Pull-Up
sda2_ms	AB15	IO	I2C Interface Data must be Pull-Up
scl2_ms	AA14	IO	I2C Interface Clock must be Pull-Up
sda3_ms	AB16	IO	I2C Interface Data must be Pull-Up
scl3_ms	AA15	IO	I2C Interface Clock must be Pull-Up
sda4_ms	AA16	IO	I2C Interface Data must be Pull-Up
scl4_ms	AC16	IO	I2C Interface Clock must be Pull-Up
sda_s	E15	IO	I2C Interface Data must be Pull-Up
scl_s	D15	IO	I2C Interface Clock must be Pull-Up
sda_ms_hdcp	D14	IO	I2C Interface Data must be Pull-Up
scl_ms_hdcp	D13	IO	I2C Interface Clock must be Pull-Up
sda_s_hdcp	E14	IO	I2C Interface Data must be Pull-Up
scl_s_hdcp	E13	IO	I2C Interface Clock must be Pull-Up

PWM Interface for LCD Backlight Control (2 balls) / GPIO (2 balls)

Name	Pin(s)	Type	Description
pwm0	AA8	IO	PWM0 (Pulse Width Modulation) Output for LED Backlight Control
pwm1	AB9	IO	PWM1 (Pulse Width Modulation) Output for LED Backlight Control

Local Dimming Control (12 balls) / GPIO shared (12 balls)

Name	Pin(s)	Type	Description
m0_sclk	AC11	IO	Clock for Local Dimming Control 0 (SPI Interface)
m0_mosi	AA12	IO	Data for Local Dimming Control 0 (SPI Interface)
m1_sclk	AB11	IO	Clock for Local Dimming Control 1(SPI Interface)
m1_mosi	AB13	IO	Data for Local Dimming Control 1 (SPI Interface)
m2_sclk	AA11	IO	Clock for Local Dimming Control 2 (SPI Interface)
m2_mosi	AC13	IO	Data for Local Dimming Control 2 (SPI Interface)
m3_sclk	AB12	IO	Clock for Local Dimming Control 3 (SPI Interface)
m3_mosi	AA13	IO	Data for Local Dimming Control 3 (SPI Interface)
ld_vs_out0	AA9	IO	Vsync Output for Local Dimming Control 0
ld_vs_out1	AB10	IO	Vsync Output for Local Dimming Control 1
ld_vs_out2	AC10	IO	Vsync Output for Local Dimming Control 2
ld_vs_out3	AA10	IO	Vsync Output for Local Dimming Control 3

Digital Audio Input/Output Interface (7 balls) / GPIO shared (2 balls)

Name	Pin(s)	Type	Description
audclk	AC5	IO	Clock Input/Output for Digital Audio AMP
daclrch	AA5	IO	L/R Output (Front)
dacslrch	AA6	IO	Surround L/R Output
dacclfch	AB7	IO	Center and Low Frequency Output
dacsck	AC7	IO	PCM Bit Clock Output (Input) to (from) External Audio DAC
daclrck	AB5	IO	Sampling Clock Output (Input) to (from) External Audio DAC
dacrlrch	AB6	IO	Rear L/R Output

GPIO Interface for HDCP (8 balls) / GPIO shared (8 balls)

Name	Pin(s)	Type	Description
hdcp_gpio0	B18	IO	General Purpose IO for HDCP
hdcp_gpio1	C17	IO	General Purpose IO for HDCP
hdcp_gpio2	B17	IO	General Purpose IO for HDCP
hdcp_gpio3	C16	IO	General Purpose IO for HDCP
hdcp_gpio4	B16	IO	General Purpose IO for HDCP
hdcp_gpio5	A16	IO	General Purpose IO for HDCP
hdcp_gpio6	C15	IO	General Purpose IO for HDCP
hdcp_gpio7	A15	IO	General Purpose IO for HDCP

GPIO Interface -- Dedicated (10 balls)

Name	Pin(s)	Type	Description
gpio0	W8	IO	General Purpose IO
gpio1	Y8	IO	General Purpose IO
gpio2	W9	IO	General Purpose IO
gpio3	Y9	IO	General Purpose IO
gpio4	W10	IO	General Purpose IO
gpio5	Y10	IO	General Purpose IO
gpio6	W11	IO	General Purpose IO
gpio7	Y11	IO	General Purpose IO
gpio8	W12	IO	General Purpose IO
gpio9	Y12	IO	General Purpose IO

3.1.2.2 Analog Interface Pins

LG2831 has analog interfaces. Those are:

- Vx1-Rx Interface (65 balls)
- Vx1-Tx Interface (66 balls)
- RFIP(KONE) Interface (13 balls)
- USB 2.0 Host Interface -- 1 port (3 balls)

The following tables provide detailed pin descriptions.

Vx1-Rx Interface (65 balls)

Name	Pin(s)	Type	Description
VRX0P	AA18	AI	Vx1 Serial Data Input
VRX0N	Y18	AI	Vx1 Serial Data Input
VRX1N	Y19	AI	Vx1 Serial Data Input
VRX1P	AA19	AI	Vx1 Serial Data Input
VRX2P	AC19	AI	Vx1 Serial Data Input
VRX2N	AB19	AI	Vx1 Serial Data Input
VRX3N	AC20	AI	Vx1 Serial Data Input
VRX3P	AC21	AI	Vx1 Serial Data Input
VRX4P	AB21	AI	Vx1 Serial Data Input
VRX4N	AB20	AI	Vx1 Serial Data Input
VRX5N	AB22	AI	Vx1 Serial Data Input
VRX5P	AB23	AI	Vx1 Serial Data Input
VRX6P	AA21	AI	Vx1 Serial Data Input
VRX6N	AA20	AI	Vx1 Serial Data Input
VRX7N	Y20	AI	Vx1 Serial Data Input
VRX7P	Y21	AI	Vx1 Serial Data Input
VRX8P	Y23	AI	Vx1 Serial Data Input
VRX8N	Y22	AI	Vx1 Serial Data Input
VRX9N	W20	AI	Vx1 Serial Data Input
VRX9P	W21	AI	Vx1 Serial Data Input
VRX10P	V21	AI	Vx1 Serial Data Input
VRX10N	V20	AI	Vx1 Serial Data Input
VRX11N	V22	AI	Vx1 Serial Data Input
VRX11P	V23	AI	Vx1 Serial Data Input
VRX12P	U21	AI	Vx1 Serial Data Input
VRX12N	U20	AI	Vx1 Serial Data Input
VRX13N	T20	AI	Vx1 Serial Data Input
VRX13P	T21	AI	Vx1 Serial Data Input
VRX14P	T23	AI	Vx1 Serial Data Input
VRX14N	T22	AI	Vx1 Serial Data Input
VRX15N	R20	AI	Vx1 Serial Data Input
VRX15P	R21	AI	Vx1 Serial Data Input
VRX16P	P21	AI	Vx1 Serial Data Input
VRX16N	P20	AI	Vx1 Serial Data Input
VRX17N	P22	AI	Vx1 Serial Data Input

VRX17P	P23	AI	Vx1 Serial Data Input
VRX18P	N21	AI	Vx1 Serial Data Input
VRX18N	N20	AI	Vx1 Serial Data Input
VRX19N	M20	AI	Vx1 Serial Data Input
VRX19P	M21	AI	Vx1 Serial Data Input
VRX20P	M23	AI	Vx1 Serial Data Input
VRX20N	M22	AI	Vx1 Serial Data Input
VRX21N	L20	AI	Vx1 Serial Data Input
VRX21P	L21	AI	Vx1 Serial Data Input
VRX22P	K21	AI	Vx1 Serial Data Input
VRX22N	K20	AI	Vx1 Serial Data Input
VRX23N	K22	AI	Vx1 Serial Data Input
VRX23P	K23	AI	Vx1 Serial Data Input
VRX24P	J21	AI	Vx1 Serial Data Input
VRX24N	J20	AI	Vx1 Serial Data Input
VRX25N	H20	AI	Vx1 Serial Data Input
VRX25P	H21	AI	Vx1 Serial Data Input
VRX26P	H23	AI	Vx1 Serial Data Input
VRX26N	H22	AI	Vx1 Serial Data Input
VRX27N	G20	AI	Vx1 Serial Data Input
VRX27P	G21	AI	Vx1 Serial Data Input
VRX28P	F21	AI	Vx1 Serial Data Input
VRX28N	F20	AI	Vx1 Serial Data Input
VRX29N	F22	AI	Vx1 Serial Data Input
VRX29P	F23	AI	Vx1 Serial Data Input
VRX30P	E22	AI	Vx1 Serial Data Input
VRX30N	E23	AI	Vx1 Serial Data Input
VRX31N	E21	AI	Vx1 Serial Data Input
VRX31P	E20	AI	Vx1 Serial Data Input
vrx_lock_n	W15	OD	Vx1 Lock (Active Low). Must be external Pull-Up.

Vx1-Tx Interface (66 balls)

Name	Pin(s)	Type	Description
C4TX_0N	R3	AO	Vx1 Serial Data Output
C4TX_0P	R4	AO	Vx1 Serial Data Output
C4TX_1N	P1	AO	Vx1 Serial Data Output
C4TX_1P	P2	AO	Vx1 Serial Data Output
C4TX_2N	P3	AO	Vx1 Serial Data Output
C4TX_2P	P4	AO	Vx1 Serial Data Output
C4TX_3N	N3	AO	Vx1 Serial Data Output
C4TX_3P	N4	AO	Vx1 Serial Data Output
C4TX_4N	M1	AO	Vx1 Serial Data Output
C4TX_4P	M2	AO	Vx1 Serial Data Output
C4TX_5N	M3	AO	Vx1 Serial Data Output
C4TX_5P	M4	AO	Vx1 Serial Data Output
C4TX_6N	L3	AO	Vx1 Serial Data Output
C4TX_6P	L4	AO	Vx1 Serial Data Output

C4TX_7N	K1	AO	Vx1 Serial Data Output
C4TX_7P	K2	AO	Vx1 Serial Data Output
TX_LOCKN_0	K5	AI	Vx1 Locking Check Pin
C4TX_8N	K3	AO	Vx1 Serial Data Output
C4TX_8P	K4	AO	Vx1 Serial Data Output
C4TX_9N	J3	AO	Vx1 Serial Data Output
C4TX_9P	J4	AO	Vx1 Serial Data Output
C4TX_10N	H1	AO	Vx1 Serial Data Output
C4TX_10P	H2	AO	Vx1 Serial Data Output
C4TX_11N	H3	AO	Vx1 Serial Data Output
C4TX_11P	H4	AO	Vx1 Locking Check Pin 0
C4TX_12N	G3	AO	Vx1 Serial Data Output
C4TX_12P	G4	AO	Vx1 Serial Data Output
C4TX_13N	F1	AO	Vx1 Serial Data Output
C4TX_13P	F2	AO	Vx1 Serial Data Output
C4TX_14N	F3	AO	Vx1 Serial Data Output
C4TX_14P	F4	AO	Vx1 Serial Data Output
C4TX_15N	E3	AO	Vx1 Serial Data Output
C4TX_15P	E4	AO	Vx1 Serial Data Output
C4TX_16N	D1	AO	Vx1 Serial Data Output
C4TX_16P	D2	AO	Vx1 Serial Data Output
C4TX_17N	D3	AO	Vx1 Serial Data Output
C4TX_17P	D4	AO	Vx1 Serial Data Output
C4TX_18N	C3	AO	Vx1 Serial Data Output
C4TX_18P	C4	AO	Vx1 Serial Data Output
C4TX_19N	B1	AO	Vx1 Serial Data Output
C4TX_19P	B2	AO	Vx1 Serial Data Output
C4TX_20N	B3	AO	Vx1 Serial Data Output
C4TX_20P	B4	AO	Vx1 Serial Data Output
C4TX_21N	A3	AO	Vx1 Serial Data Output
C4TX_21P	A4	AO	Vx1 Serial Data Output
C4TX_22N	D5	AO	Vx1 Serial Data Output
C4TX_22P	C5	AO	Vx1 Serial Data Output
C4TX_23N	D6	AO	Vx1 Serial Data Output
C4TX_23P	C6	AO	Vx1 Serial Data Output
TX_LOCKN_1	E6	AI	Vx1 Locking Check Pin
C4TX_24N	B6	AO	Vx1 Serial Data Output
C4TX_24P	A6	AO	Vx1 Serial Data Output
C4TX_25N	D7	AO	Vx1 Serial Data Output
C4TX_25P	C7	AO	Vx1 Serial Data Output
C4TX_26N	D8	AO	Vx1 Serial Data Output
C4TX_26P	C8	AO	Vx1 Serial Data Output
C4TX_27N	B8	AO	Vx1 Serial Data Output
C4TX_27P	A8	AO	Vx1 Serial Data Output
C4TX_28N	D9	AO	Vx1 Serial Data Output
C4TX_28P	C9	AO	Vx1 Serial Data Output

C4TX_29N	D10	AO	Vx1 Serial Data Output
C4TX_29P	C10	AO	Vx1 Serial Data Output
C4TX_30N	B10	AO	Vx1 Serial Data Output
C4TX_30P	A10	AO	Vx1 Serial Data Output
C4TX_31N	B11	AO	Vx1 Serial Data Output
C4TX_31P	A11	AO	Vx1 Serial Data Output

RFIP(KONE) Interface (13 balls)

Name	Pin(s)	Type	Description
RF0_10G	AC3	AIO	10 GHz RF0-port
RF0_REFCLK_OUT	AC2	AO	330MHz RF0 reference clock for KASI
RF0_CTRL	AB1	AIO	RF0 control signal interface for KASI
RF1_10G	T1	AIO	10 GHz RF1-port
RF1_REFCLK_OUT	U1	AO	330MHz RF1 reference clock for KASI
RF1_CTRL	V1	AIO	RF1 control signal interface for KASI
RF_REFCLK_IN	AA1	AI	48 MHz reference clock input
RF_AFCDAC	Y2	AO	AFCDAC output for VCTCXO control
RF_VREF_CAP	Y1	AO	External filtering capacitor pin for the reference voltage
RF_TP_P	V4	AIO	Testpoint (Positive)
RF_TP_N	W4	AIOO	Testpoint (Negative)
KASI_SCLK	Y4	DO	RFFE clock for KASI debug
KASI_SDATA	AA4	DIO	RFFE input and output data for KASI debug

USB 2.0 Host Interface -- 1 port (3 balls)

Name	Pin(s)	Type	Description
USB2_0_TXRTUNE	C12	AIO	USB 2.0 Transmitter Resistor Tune & voltage probe. External Resistor value is (200 ohm±1%) to GND.
USB2_0_DM	A13	AIO	USB port 2 D-. If not used, must be floated.
USB2_0_DP	B13	AIO	USB port 2 D+. If not used, must be floated.

3.2 Pin Description for LG2851

LG2851 Module connections and testpoints are listed in the table below.

Module Interface (8 pins and testpoints)

Name	Pin(s)	Type	Description
COAX			Triplexer connector
+5.0V			5V external supply DC connector
TP100			Testpoint for VQPS
TP103			Testpoint for GPIO0
TP107			Testpoint for VREF_CAP
TP108			Testpoint for +5.0V
TP109			Testpoint for GND
TP110			Testpoint for +1.8V

4 RF Specifications

RF specifications are defined in typical conditions and room temperature only (ambient). Performance may vary due to variations in IC manufacturing process.

4.1 Receiver and Transmitter for LG2831

Receiver and transmitter specifications are defined below.

[Table 4-1] Transceiver specifications

Parameter	Description	Min	Typ	Max	Unit
IF*_10G	Frequency range	8.4	10.56	12.72	GHz
	Impedance		50		Ohm
	S11			-10	dB
IF*_10G Transmitter	Pout	-17	-14		dBm
	OIP3-Linearity (Ptot-IM3/2)	11			dBm
	Calibrated Image LO leakage			 -40 -45	 dBc dBc
	Band flattness DMG EDMG		 < +/1 < +/2		 dB dB
	EVM DMG EDMG			 -33 -33	 dB dB
	Pin DC-level		0		V
IF*_10G Receiver	Noise figure (ADC included, max gain)			18	dB
	Analog gain range 0 … 24dB				
	Analog gain max	24			dB
	Analog gain step		3		dB
	Calibrated Image			 -40	 dBc
	IM3-Linearity Pin=-10dBm (freq1 Freq2, Pin=-13dBm per tone)			-40	dBc
	EVM DMG EDMG			 -32 -32	 dB dB
	Pin DC-level		0		V
IF*_CTRL KIF-interface	Frequency channel		2640		MHz
	Impedance		50		Ohm
	S11			-10	dB
	TX Signal amplitude tune range	25		150	mV
	RX Signal amplitude min detection	30			mV
	Signal DC-level		500		mV
IF*_REFCLKOUT	Frequency		330		MHz
	Impedance		50		Ohm
	S11			-10	dB
	Signal amplitude		150		mV
	Signal DC-level		600		mV

IF_REFCLK_IN	Frequency		48		MHz
	Frequency accuracy			20	ppm
	Clock input level requirement (from VCTCXO)		0.8		Vpp
	Port DC-level (internal)		450		mV

*=0 or 1 depending on the path

4.2 Receiver and Transmitter for LG2851

Receiver and transmitter specifications are defined for 32 or 16 line-up unless otherwise stated. RX and TX can also be operated with fewer line-ups enabled.

[Table 4-2] Receiver specifications for LG2851 Box Module

Parameter	Description	Min	Typ	Max	Unit
	Operating frequency	57.24		65.88	GHz
	Gain (with 32RX)	36	42		dB
	Gain (with 16RX)	32	38		dB
	Sensitivity (1.76GHz band width, 15db SNR)		-70		dBm EIRS
	Sensitivity (3.52GHz band width, 15db SNR)		-67		dBm EIRS
	Maximum input power		-52		dBm EIRS
	IIP3 (with 32RX)	-38	-30		dBm EIRS
	IIP3 (with 16RX)	-34	-26		dBm EIRS
	RX EVM (with phase tracking)		-30		dB
	RX phase control step size		45		deg
	COAX-port frequency range			12.32	GHz
	Maximum COAX-port output power		-13		dBm
	COAX-port output impedance		50		Ω
	COAX-port return loss (S11)		-10		dB

Conditions: T_A= 25°C, supply VDD= 5V

[Table 4-3] Transmitter specifications for LG2851 Box Module

Parameter	Description	Min	Typ	Max	Unit
	Operating frequency	57.24		65.88	GHz
	Maximum output power		37		dBm EIRP
	OIP3	44	48		dBm EIRP
	Gain (nominal input power -20dBm)	44	52		dB
	TX EVM (with phase tracking)		-30		dB
	TX phase control step size		45		deg
	COAX port frequency range			12.32	GHz
	COAX-port input power		-20		dBm
	COAX-port input impedance		50		Ω
	COAX-port return loss (S11)			-10	dB

Conditions: T_A= 25°C, supply VDD= 5V

[Table 4-4] Receiver specifications for LG2851 Display Module

Parameter	Description	Min	Typ	Max	Unit
	Operating frequency	57.24		65.88	GHz
	Gain (with 16RX)	32	38		dB
	Sensitivity (1.76GHz band width, 15db SNR)		-68		dBm EIRS
	Sensitivity (3.52GHz band width, 15db SNR)		-65		dBm EIRS
	Maximum input power		-48		dBm EIRS
	IIP3 (with 16RX)	-34	-26		dBm EIRS
	RX EVM (with phase tracking)		-30		dB
	RX phase control step size		45		deg
	COAX-port frequency range			12.32	GHz
	Maximum COAX-port output power		-13		dBm
	COAX-port output impedance		50		Ω
	COAX-port return loss (S11)		-10		dB

Conditions: T_A= 25°C, supply VDD= 5V

[Table 4-5] Transmitter specifications for LG2851 Display Module

Parameter	Description	Min	Typ	Max	Unit
	Operating frequency	57.24		65.88	GHz
	Maximum output power		35		dBm EIRP
	OIP3	38	42		dBm EIRP
	Gain (nominal input power -20dBm)	38	46		dB
	TX EVM (with phase tracking)		-30		dB
	TX phase control step size		45		deg
	COAX port frequency range			12.32	GHz
	COAX-port input power		-20		dBm
	COAX-port input impedance		50		Ω
	COAX-port return loss (S11)			-10	dB

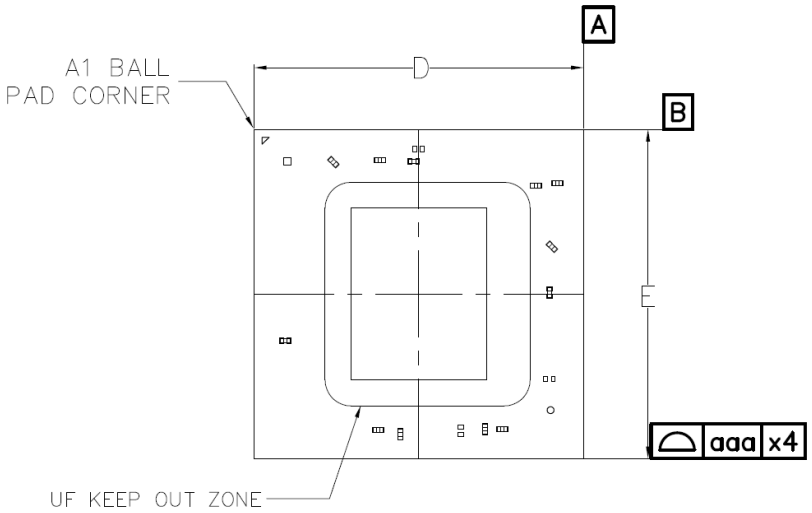
Conditions: T_A= 25°C, supply VDD= 5V

5 Package

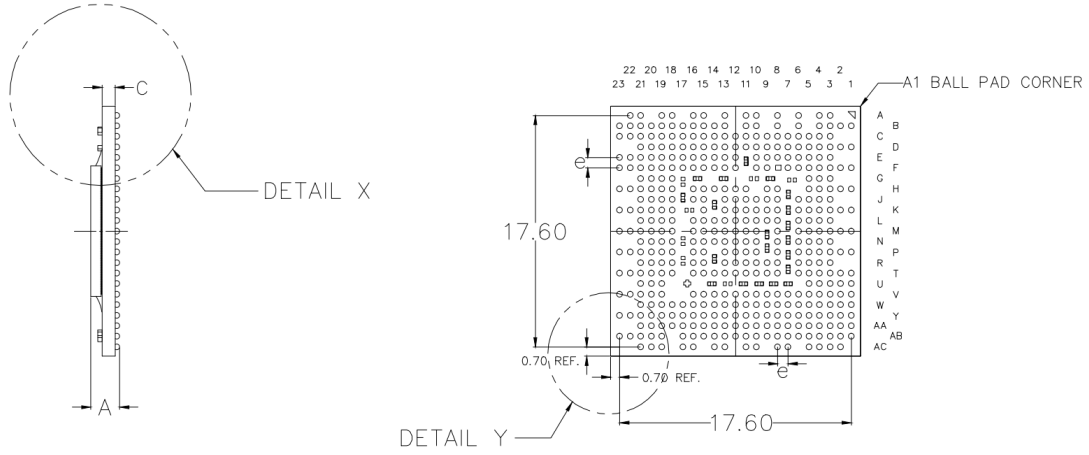
This chapter describes the package information of LG2831 and LG2851 module.

5.1 Package Information for LG2831

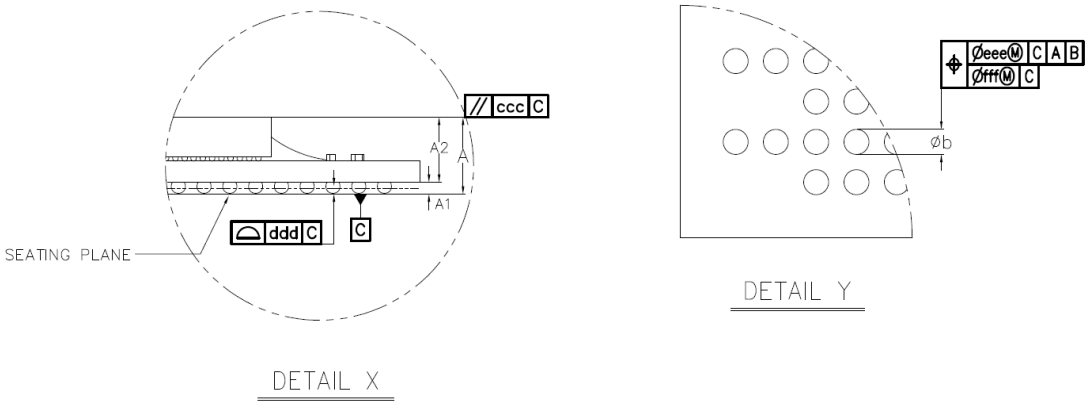
The following figures outline the package information of LG2831.



[Figure 5-1] LG2831 Package Outline Diagram – Top View



[Figure 5-2] LG2831 Package Outline Diagram – Side View / Bottom View



[Figure 5-3] LG2831 Package Outline Diagram – DETAL X/Y

SYMBOL	MIN.	NOM.	MAX.
A	2.00	2.20	2.40
A1	0.24	0.34	0.44
A2	1.76	1.86	1.96
D	18.90	19.00	19.10
E	18.90	19.00	19.10
M	23x23 <DEPOPULATED>		
aaa			0.10
ccc			0.20
ddd			0.20
eee			0.15
fff			0.08
øb	0.35	0.45	0.55
e	0.80 REF.		
C	1.002 REF.		
Raw ball size	ø0.45		

NOTES:

1. All DIMENSIONS AND TOLERANCE CONFORM TO ASME Y14.5M–1994
2. TERMINAL POSITIONS DESIGNATION PER JESD 95–1, SPP–010.
3. COMPLIANT TO JEDEC REGISTERED OUTLINE DR–4.5N, NO EXACT VARIATION AND WITH EXCEPTION TO DIM 'A'.

*A value is increased by 0.02

[Figure 5-4] LG2831 Package Outline Diagram – Symbol Description

REV.	DESCRIPTION	DATE	ENG
–	GENERATE	07/30/'20	TS KIM
A	CHANGE THE BALL MAP 419B TO 416B	02/04/'21	TS KIM
B	ADD THE LSC CAPACITOL 1EA AND MODIFY THE DESIGN	06/21/'22	HS KIM

5.2 Dimension for LG2831 Board

[Figure 5-5] LG2831 Box Board Dimensions (Height : 7.45 mm)

[Figure 5-6] LG2831 Display Board dimensions (Height : 6.85 mm)

5.3 Dimension for LG2851 Module

[Figure 5-7] LG2851 Box Module Dimensions (Height : 2.5 mm)

[Figure 5-8] LG2851 Display Module dimensions (Height : 2.99 mm)

6 Specific Installation Guidelines for Host Product Manufacturer

This module has certified as limited modular approval without power supply regulation. When this module is installed into the host product, the host product must be designed to provide the rated voltages into this module as described in this installation manual.

The PCB board that is providing the rated voltage to the module should be designed to get 12 Vdc rated voltage from the power source in host device and but also the PCB board has such regulator such as, dc-dc converter, should have the capabilities to offer the each rated voltage to the each components in this module as described in power supply pins information of section 3.1.1 and section 3.2.

If it cannot be achieved in host device design, additional testing to prove the host device with this transmitter module is still being compliance with applicable requirements is needed.

7 Regulatory Statement

This chapter describes the regulatory statement for FCC, ISED, CE and UKCA.

7.1 FCC

FCC Part 15.19 Statements:

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC Part 15.21 statement

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

Regulatory notice to host manufacturer according to KDB 996369 D03 OEM Manual v01

This module has been granted modular approval as below listed FCC rule parts.
-FCC Rule parts **15C(15.255)**

Summarize the specific operational use conditions
-The OEM integrator should use equivalent antennas which is the same type and equal or less gain then an antenna listed below this instruction manual.

RF exposure considerations

-The module has been certified for integration into products only by OEM integrators under the following condition:

-The antenna(s) must be installed such that a minimum separation distance of at least 20 cm is maintained between the radiator (antenna) and all persons at all times.

-The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

-Mobile use

As long as the three conditions above are met, further transmitter testing will not be required.
OEM integrators should provide the minimum separation distance to end users in their end-product manuals.

Antennas list

This module is certified with the following integrated antenna.

1. LGSRFT1: Patch Array Antenna, (peak antenna gain: 20 dBi)
2. LGSRFR1:

Antenna No.	Antenna type	Peak Antenna gain (dBi)
ANT0	Patch Array Antenna	19.5
ANT1	Dipole(Left) / Monopole(Right) Array Antenna	13.7(Left),12.5(Right)
ANT2	Monopole Array Antenna	7.7

Any new antenna type, higher gain than listed antenna should be met the requirements of FCC rule 15.203 and 2.1043 as permissive change procedure.

Label and compliance information

End Product Labeling

The module is labeled with its own FCC ID and IC Certification Number. If the FCC ID and IC Certification Number are not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final end product must be labeled in a visible area with the following:

"Contains FCC ID: **BEJLGSRFR1 / BEJLGSRFT1**
"Contains IC**: 2703H-LGSRFR1 / 2703H-LGSRFT1**

Information on test modes and additional testing requirements

-OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, additional transmitter in the host, etc.).

Additional testing, Part 15 Subpart B disclaimer
-The final host product also requires Part 15 subpart B compliance testing with the modular transmitter installed to be properly authorized for operation as a Part 15 digital device.

6.2 ISED

RSS-GEN, Sec. 7.1.3–(licence-exempt radio apparatus)
This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions:

(1) this device may not cause interference, and
(2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

RF Exposure
The antenna (or antennas) must be installed so as to maintain at all times a distance minimum of at least 20 cm between the radiation source (antenna) and any individual. This device may not be installed or used in conjunction with any other antenna or transmitter.

l'exposition aux RF L'antenne (ou les antennes) doit être installée de façon à maintenir à tout instant une distance minimum de au moins 20 cm entre la source de radiation (l'antenne) et toute personne physique.

Caution: Any changes or modifications to this device not explicitly approved by manufacturer could void your authority to operate this equipment. Attention:

Les changements ou modifications de cet appareil non expressément approuvé par le fabricant peuvent annuler votre droit à utiliser cet équipement.

É tiquetage du produit final (IC)

Le module est étiqueté avec sa propre identification FCC et son propre numéro de certification IC. Si l'identification FCC et le numéro de certification IC ne sont pas visibles lorsque le module est installé à l'intérieur d'un autre dispositif, la partie externe du dispositif dans lequel le module est installé devra également présenter une étiquette faisant référence au module inclus. Dans ce cas, le produit final devra être étiqueté sur une zone visible avec les informations suivantes :

« Contient module émetteur IC : 2703H-LGSRFR1 / 2703H-LGSRFT1

6.3 CE

Simplified EU Declaration of Conformity
Hereby, **LG Electronics Inc.** declares that the radio equipment type **[LGSRFR1, LGSRFT1**] is in compliance with Directive 2014/53/EU. The full text of the EU declaration of conformity is available at the following internet address: **http://www.lg.com/global/support/cedoc/cedoc#**

RF Exposure
The antenna (or antennas) must be installed so as to maintain at all times a distance minimum of at least **20**cm between the radiation source (antenna) and any individual. This device may not be installed or used in conjunction with any other antenna or transmitter

EU Importer : LG Electronics European Shared Service Center B.V.
Address : Krijgsman 1, 1186 DM Amstelveen, The Netherlands

The host manufacturer has the responsibility that the host device should be compliance with all essential requirement of RED.

6.4 UKCA

Simplified UKCA Declaration of Conformity
Hereby, LG Electronics Inc. declares that the radio equipment type [**LGSRFR1, LGSRFT1**] is in compliance with the Radio Equipment Regulations 2017(SI 2017 No.1206). The full text of the UKdeclaration of conformity is available at the following internet address: http://www.lg.com/global/support/cedoc/cedoc#

UK Importer : LG Electronics U.K. Ltd
Address : Velocity 2, Brooklands Drive, Weybridge, KT13 0SL

The host manufacturer has the responsibility that the host device should be compliance with all essential requirement of the Radio Equipment Regulations 2017.