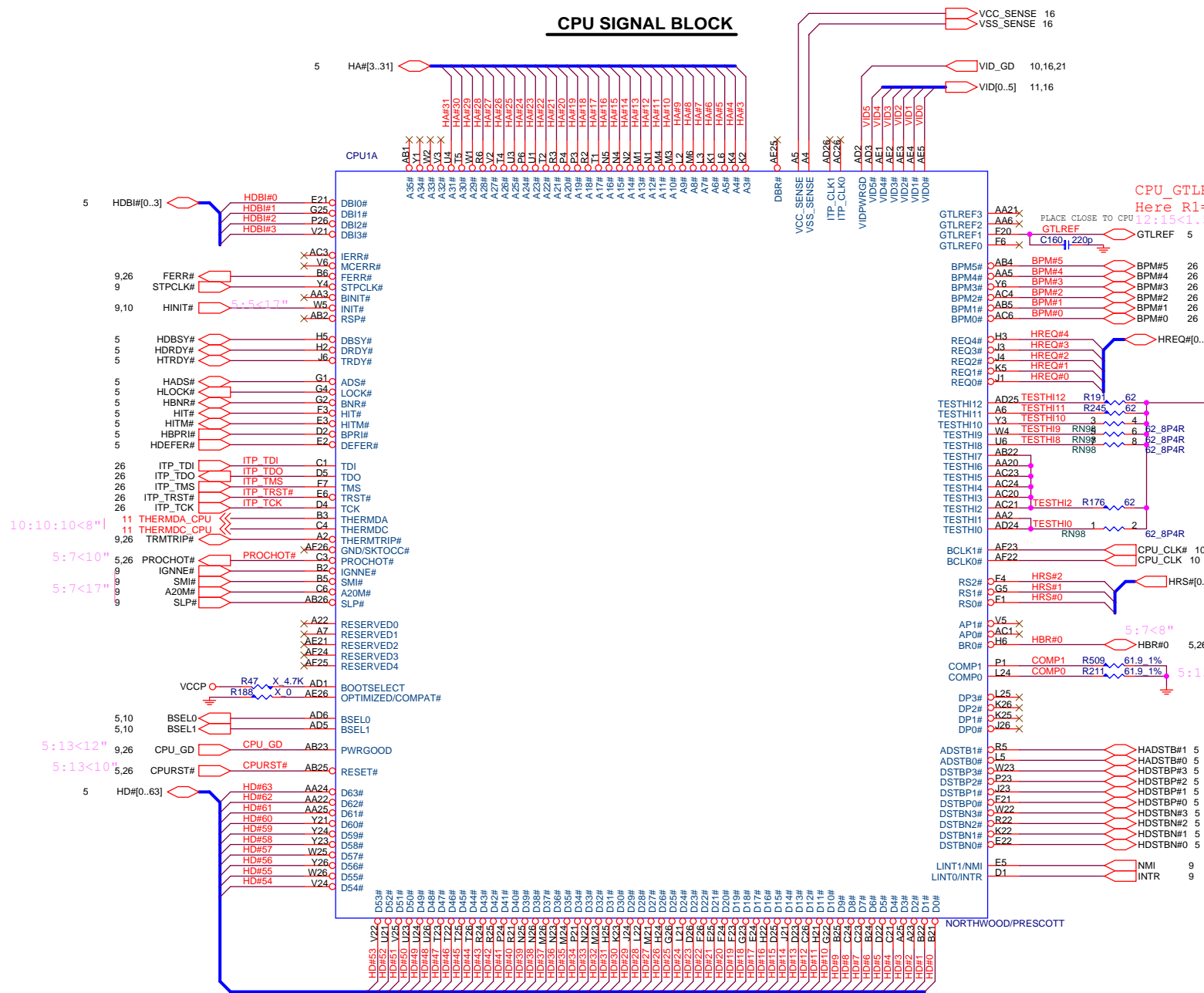
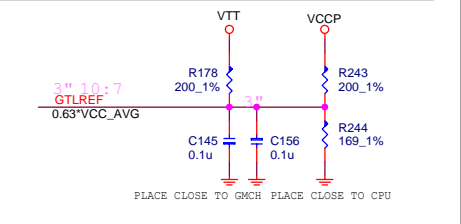


CPU SIGNAL BLOCK

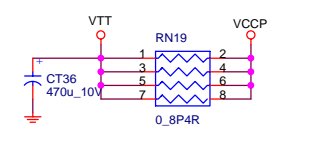


CPU GTL REFERENCE VOLTAGE BLOCK

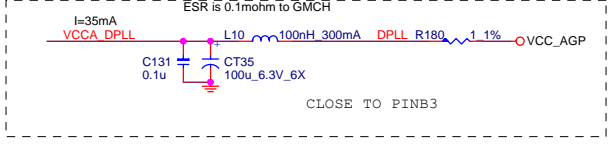
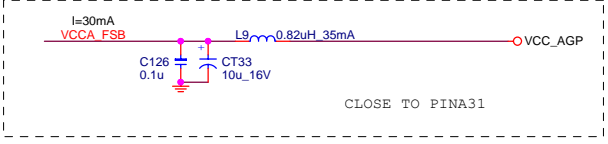
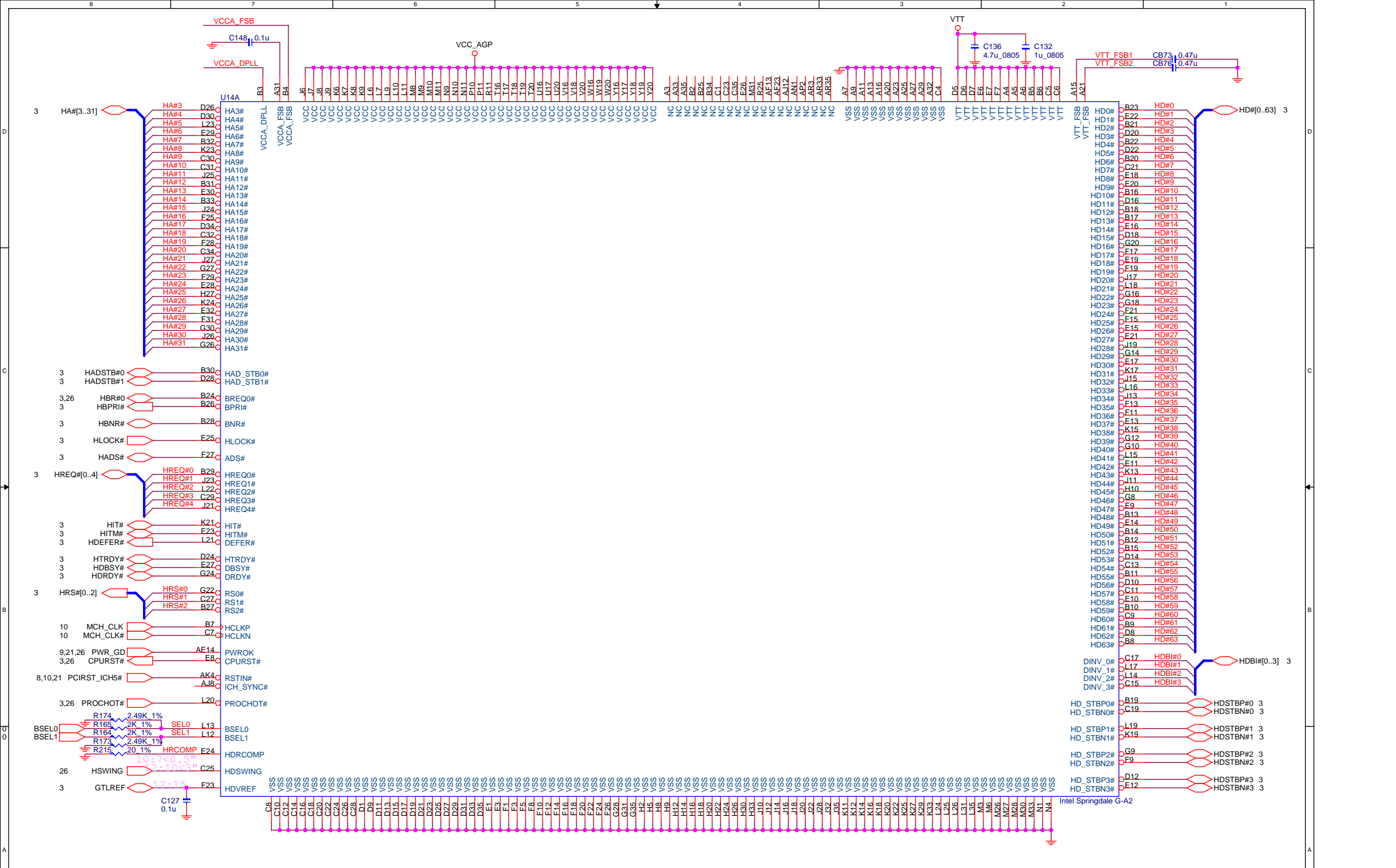


$$CPU_GTLREF = (R3 / (2R3 + R1)) * (Vccp + Vtt);$$

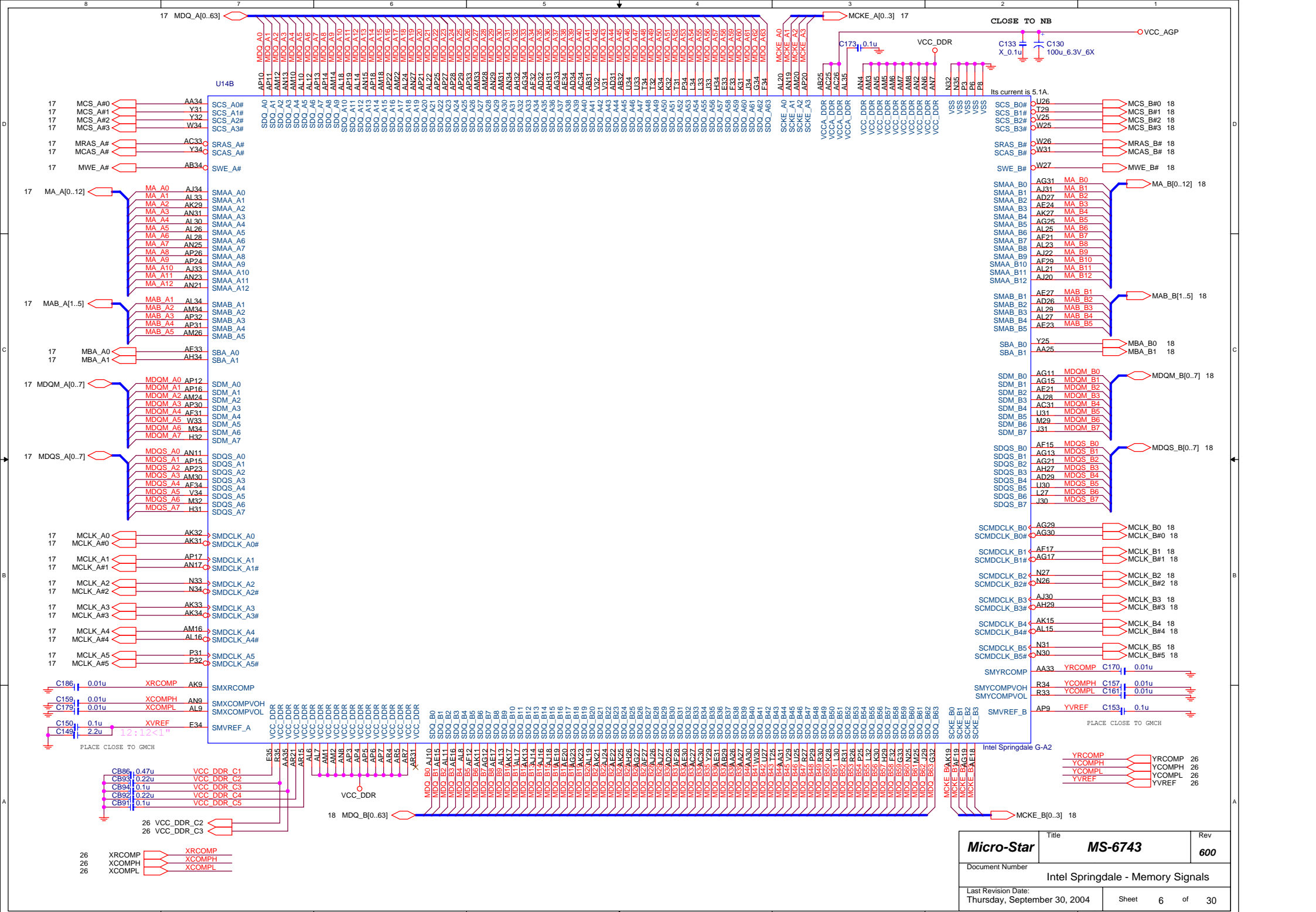
Here $R1 = R2$.

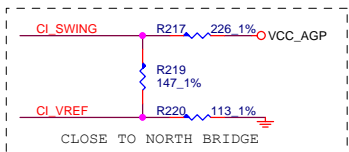
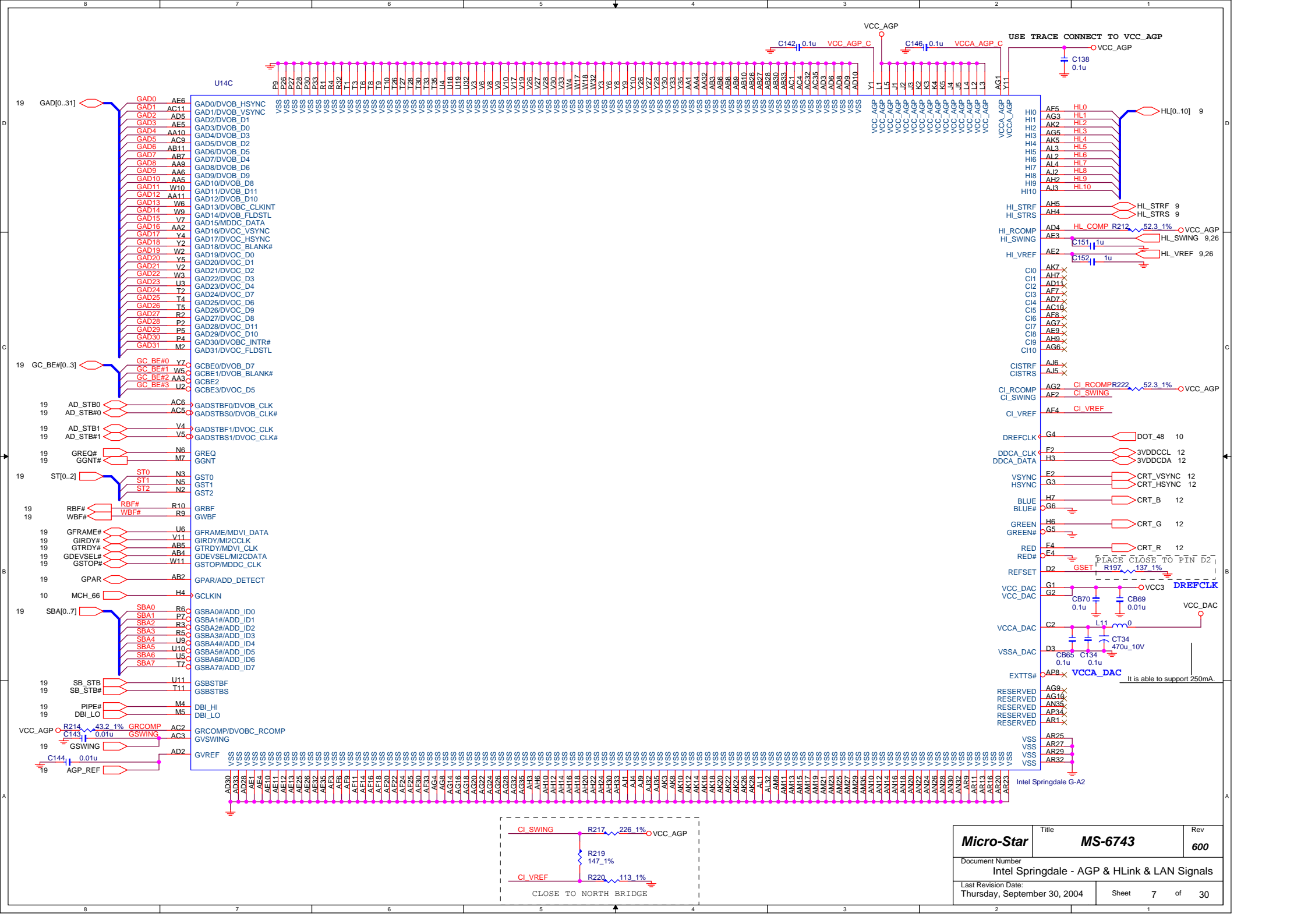


Micro-Star	Title	MS-6743	Rev	600
Document Number		Intel mPGA478B - Signals		
Last Revision Date:		Thursday, September 30, 2004		
		Sheet	3	of 30

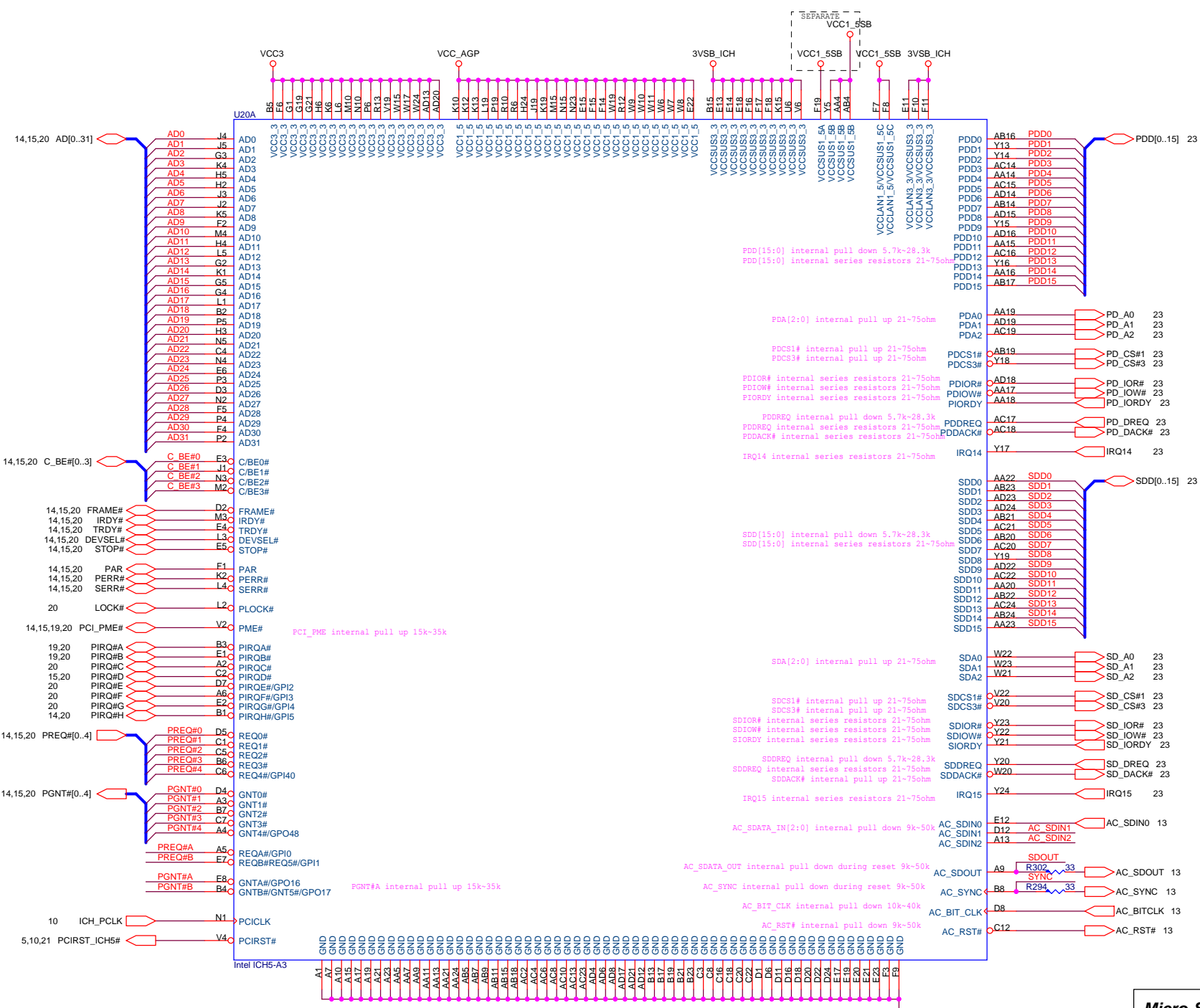


Micro-Star	Title	Rev
	MS-6743	600
Document Number	Intel Springdale - CPU Signals	
Last Revision Date:	Thursday, September 30, 2004	
	Sheet	5 of 30

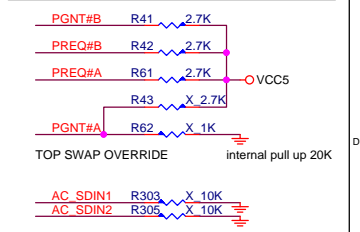




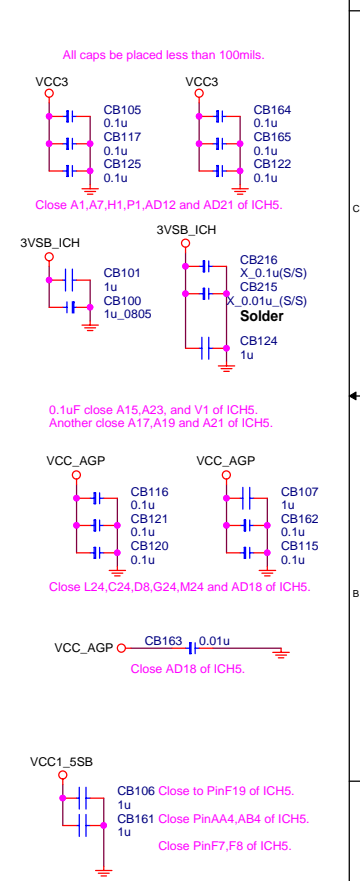
Micro-Star	Title	Rev
	MS-6743	600
Document Number		
Intel Springdale - AGP & HLink & LAN Signals		
Last Revision Date:		
Thursday, September 30, 2004	Sheet	7 of 30



ICH5 Pull-Up / Down Resistors

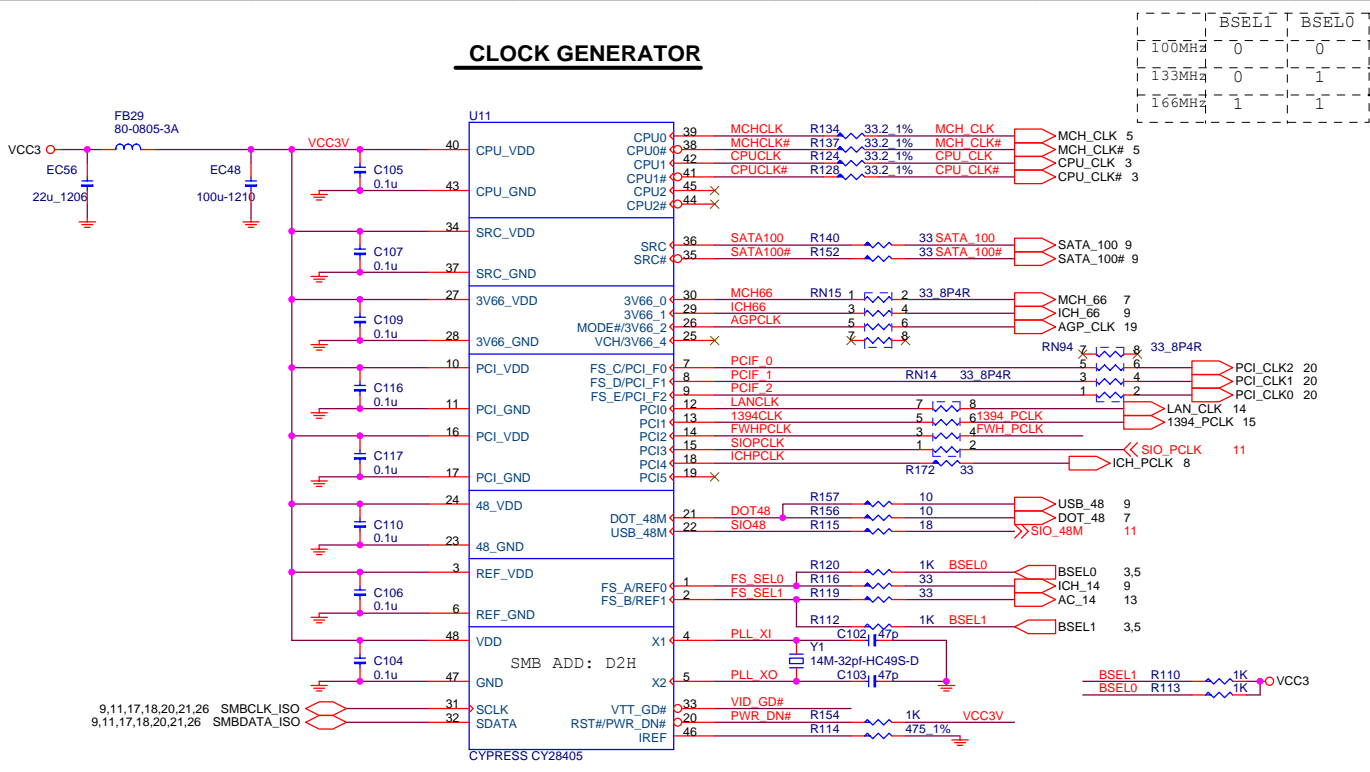


ICH5 Decoupling Capacitors

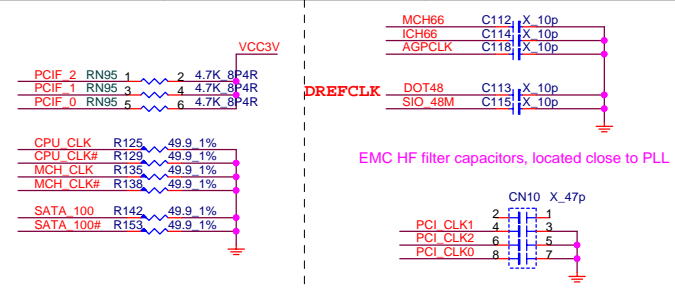


Micro-Star	Title	MS-6743	Rev
Document Number	600		
Intel ICH5 - PCI & IDE & AC97 Signals			
Last Revision Date:	Thursday, September 30, 2004	Sheet	8 of 30

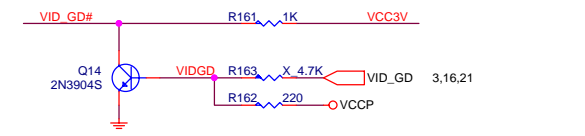
CLOCK GENERATOR



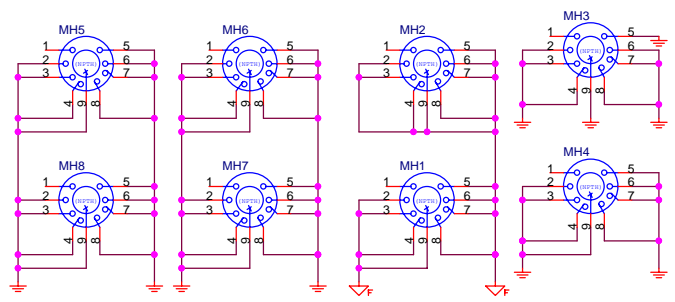
BSEL1	0	BSEL0	0
100MHz	0	1	
133MHz	0	1	
166MHz	1	1	



CLOCK GENERATOR VTT POWER DOWN BLOCK

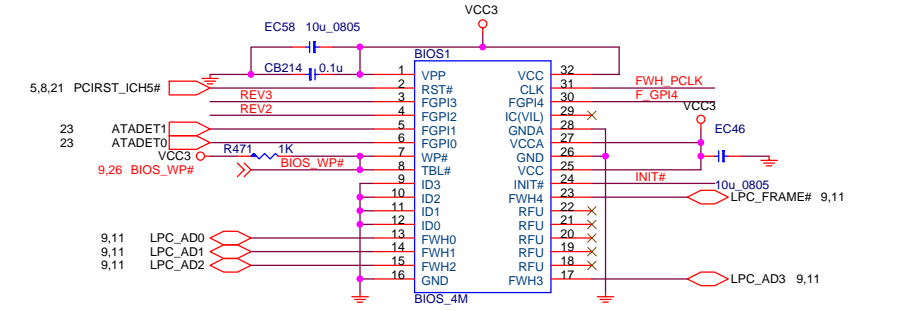


Mounting Holes

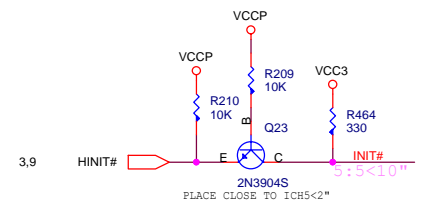


Optics Orientation Holes

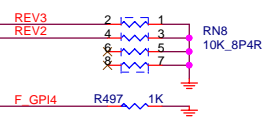
FIRMWARE HUB (FWH)



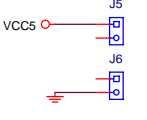
FWH INIT Signal Voltage Translation



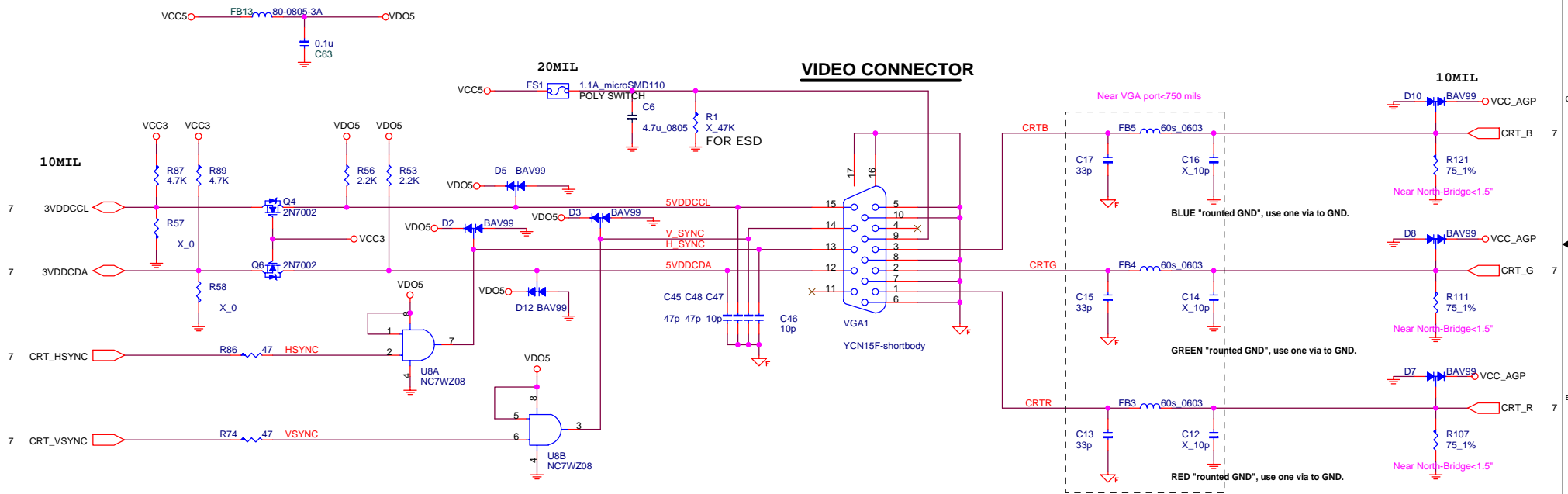
FWH RESISTORS



Simulation



Micro-Star	Title	MS-6743	Rev
			600
Document Number		CY28405 & FWH	
Last Revision Date:		Thursday, September 30, 2004	
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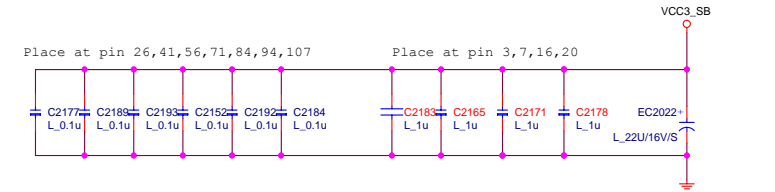
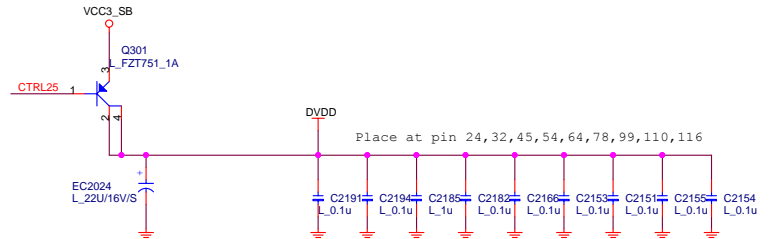
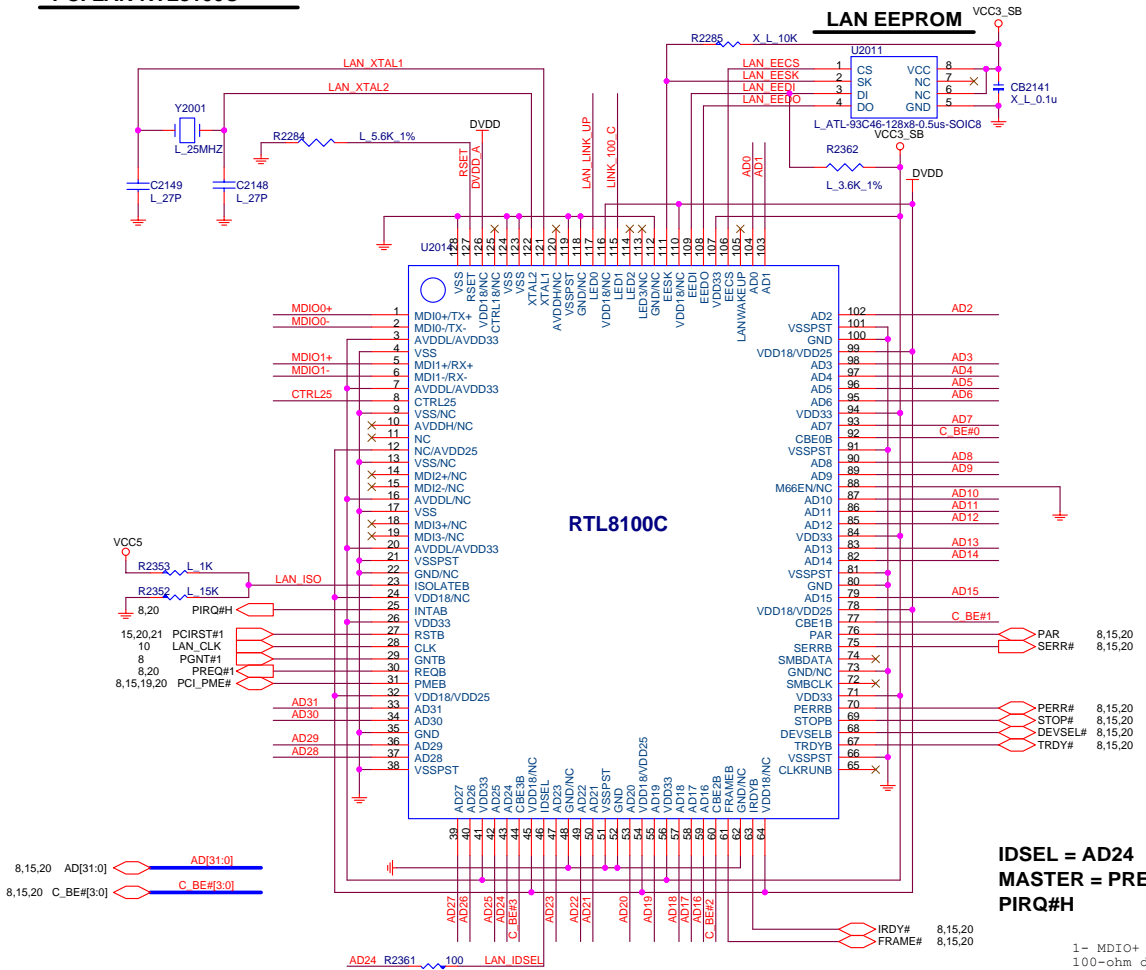


Micro-Star	Title MS-6743	Rev 600
Document Number Floppy & VGA CONNECTORS		
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PCI LAN RTL8100C

LAN EEPROM

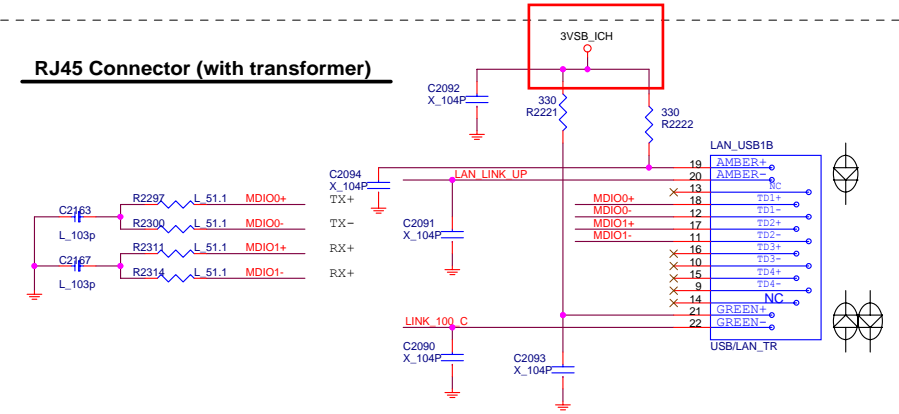
10/100 - 1A
D02-BCP6909-P03
D02-BCP6909-O05



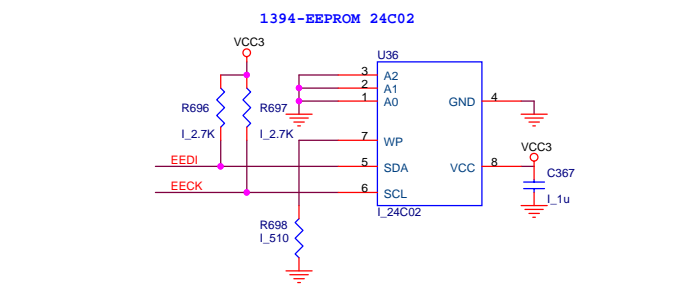
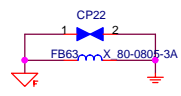
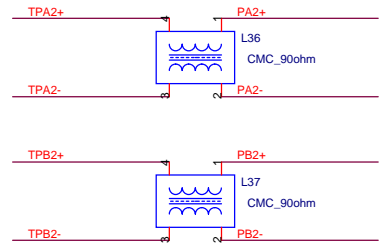
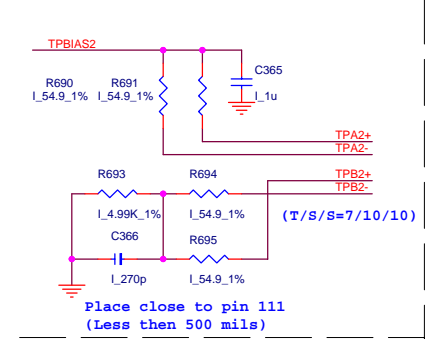
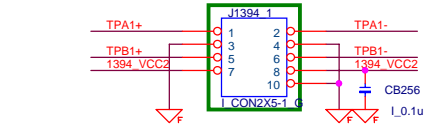
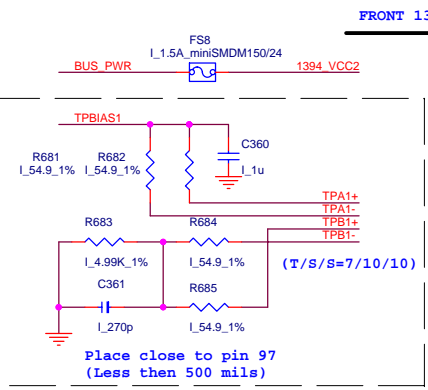
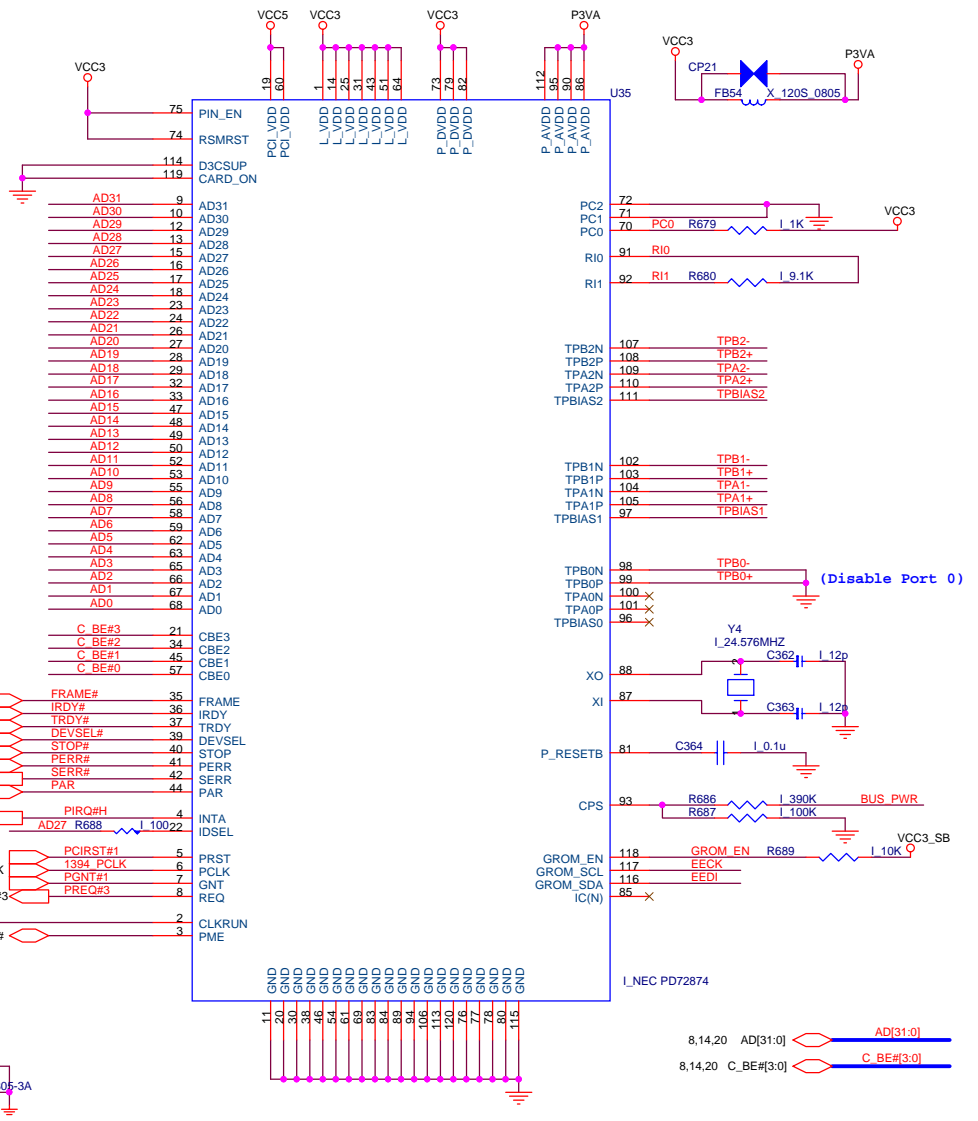
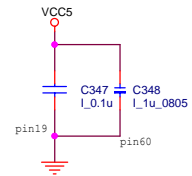
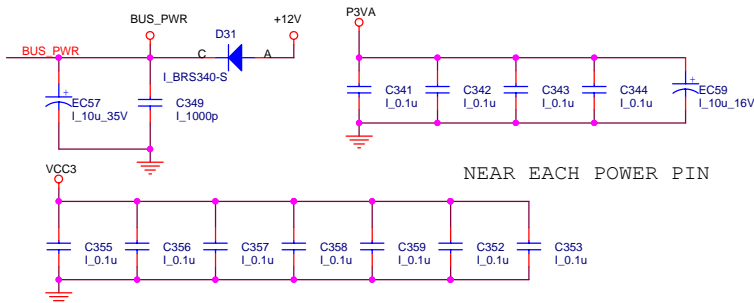
IDSEL = AD24
MASTER = PREQ#1
PIRQ#H

1- MDIO+ & MDIO- pairs should be 100-ohm differential impedance. Route equal length and symmetrically. Separate every pairs.

RJ45 Connector (with transformer)



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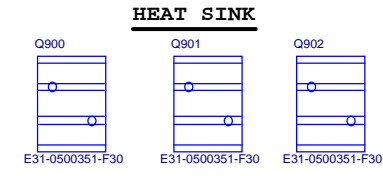
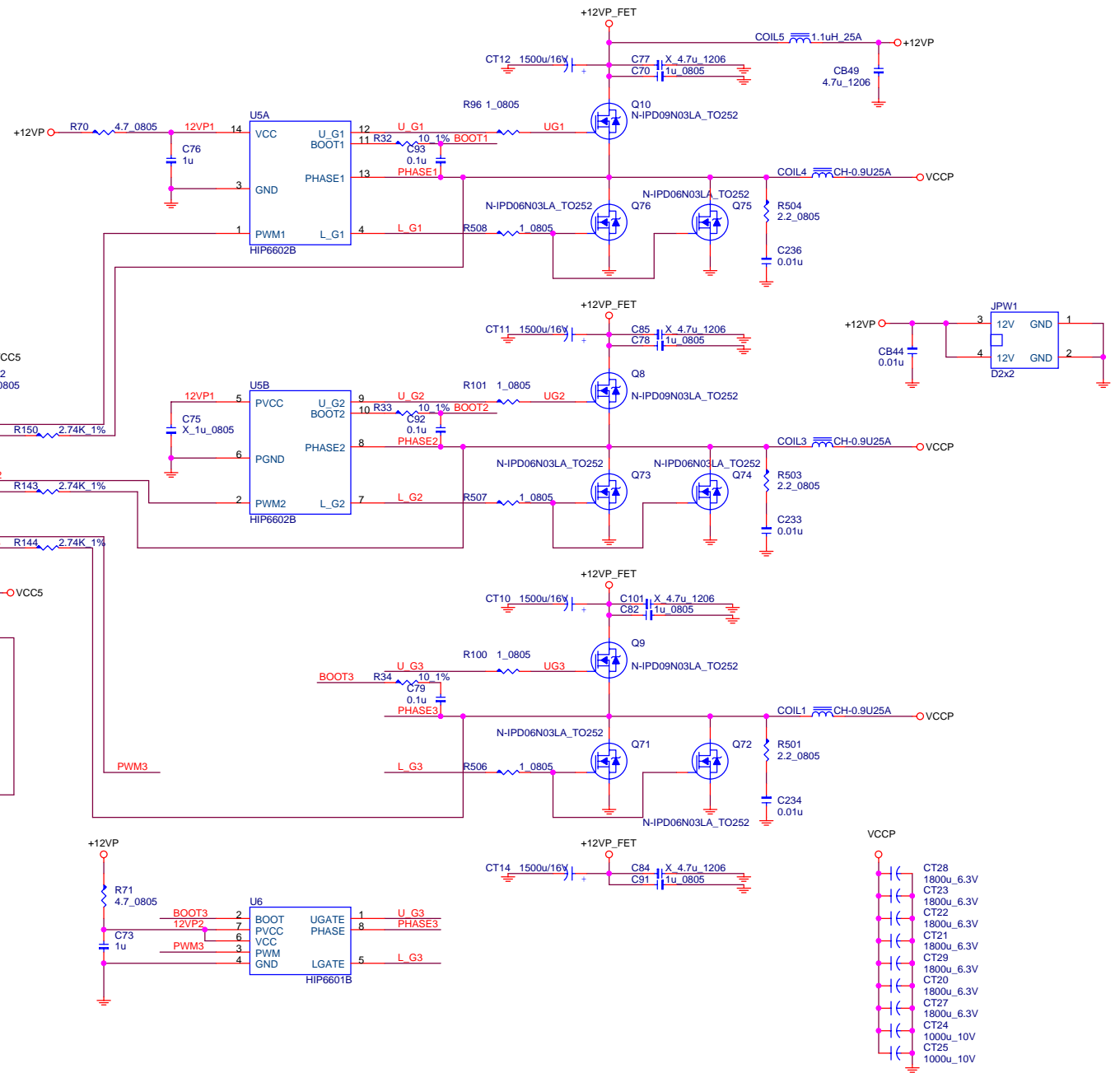
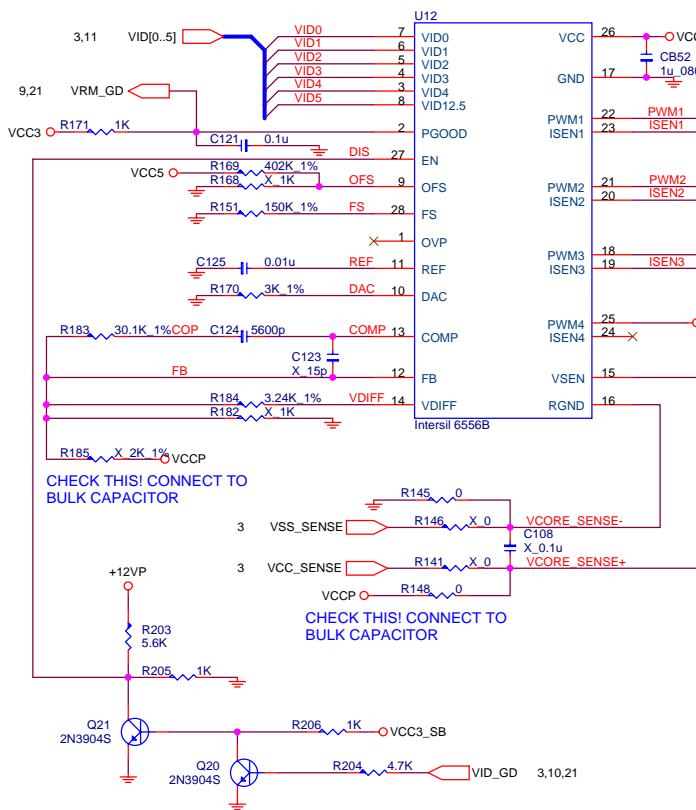
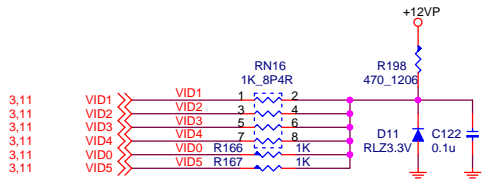
**IDSEL = AD27
MASTER = PREQ#3
PIRQ#D**

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NOTE:

- 1.ASIC TO PHY MAX Length is less than 13.0 mm.
- 2.TPA0+ & TPA0- TWISTED LENGTH IS SAME.(Tolerance±4%)
- 3.TPB0+ & TPB0- TWISTED LENGTH IS SAME.(Tolerance±4%)
- 4.TRACE WIDTH= 7MIL
- 5.TPA0 & TPB0 impedance is 56Ω±1%.
- 6.TRACE SHALL AS SOME LAYER AND BETWEEN CROSS WITH GND.
- 7.TPA0+, TPA0- & TPB0+, TPB0-, trace must be on surface

VID Pull-Up Resistor



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			600
Document Number			
VRM 10 - Intersil 6556A			
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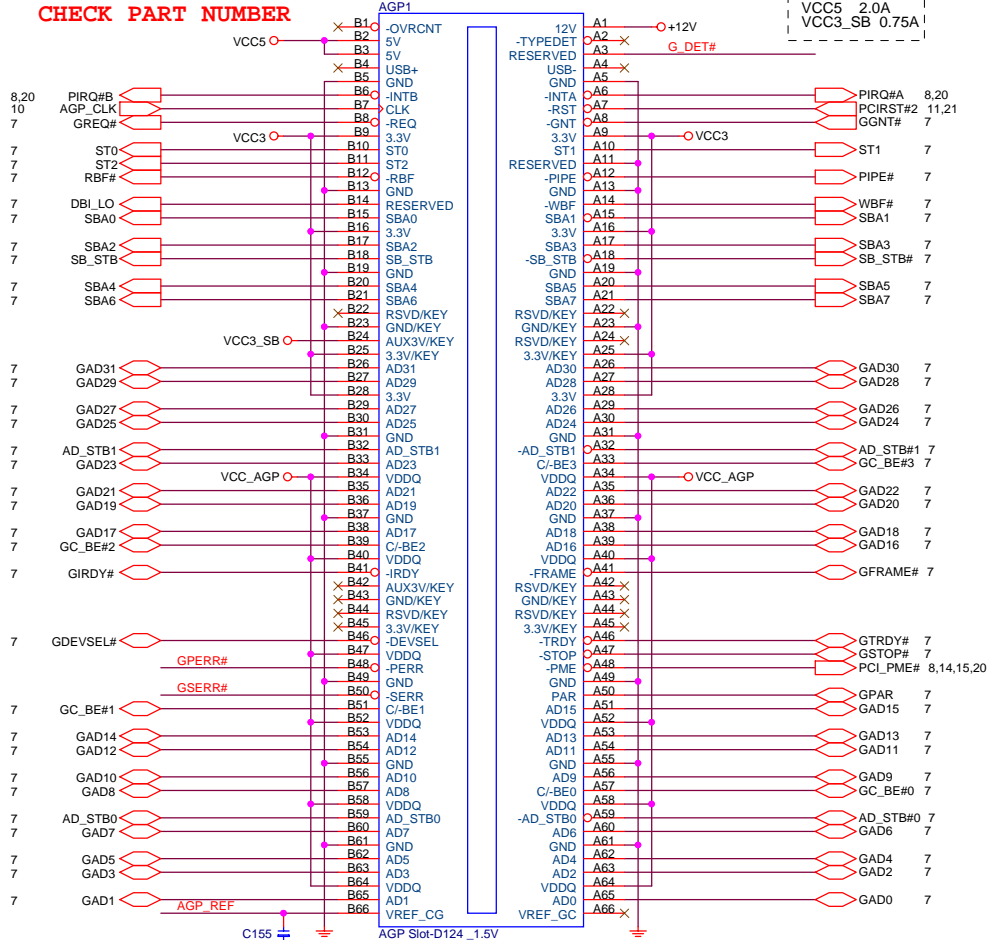
AGP 1.5V 1X/2X/4X/8X SLOT(AGP VER:3.0)

VCC5 = 60mils trace / 15 mils space

AGP Slot I_{max}

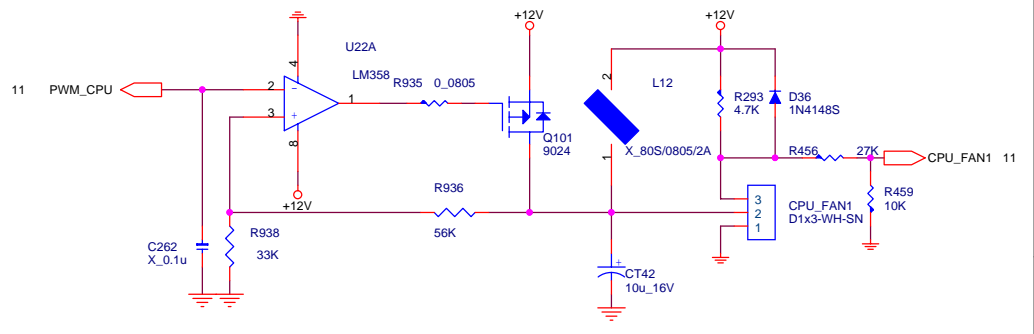
- VCCq 8.0A
- VCC3 6.0A
- VCC12 1.0A
- VCC5 2.0A
- VCC3_SB 0.75A

CHECK PART NUMBER

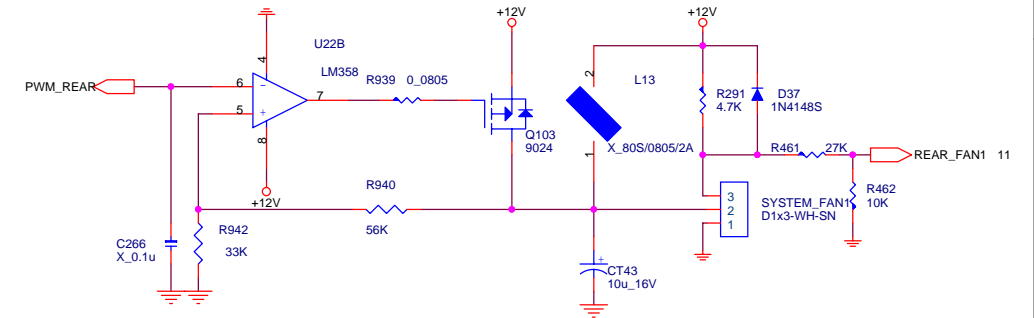


PIRQ#A / PIRQ#B

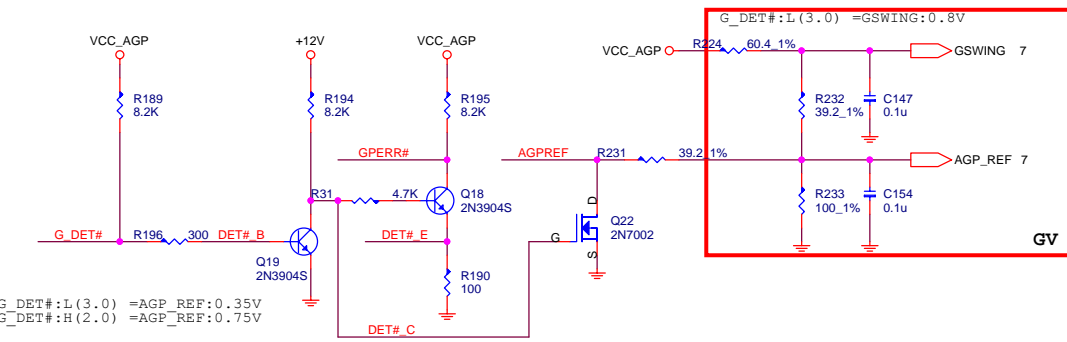
CPU FAN



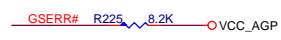
REAR FAN



Springdale Reference & Swing Voltage Circuit

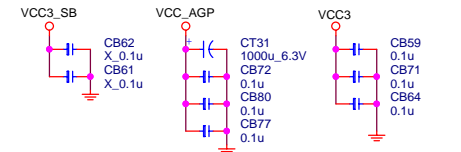


AGP TERMINATION RESISTORS



LESS 10MILS STUB TRACE LENGTH MUST BE FOLLOWING.
Place these resistors between PCI and AGP slot

AGP SLOT DECOUPLING CAPACITORS

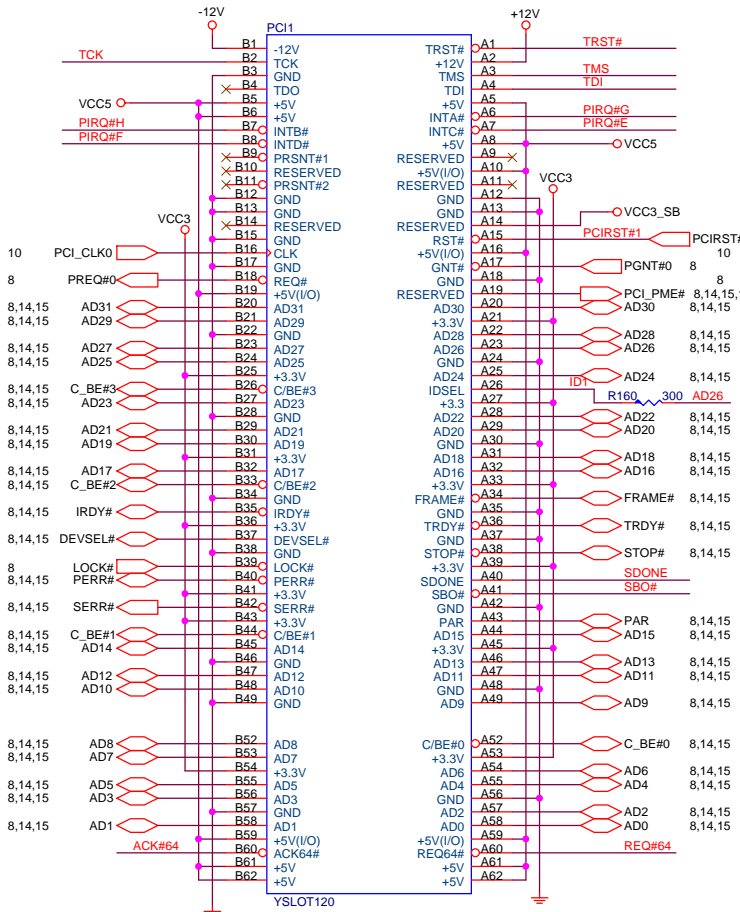


Micro-Star	Title	MS-6743	Rev
Document Number	AGP 1.5V SLOT & FAN CONNECTOR		600
Last Revision Date: Thursday, September 30, 2004			
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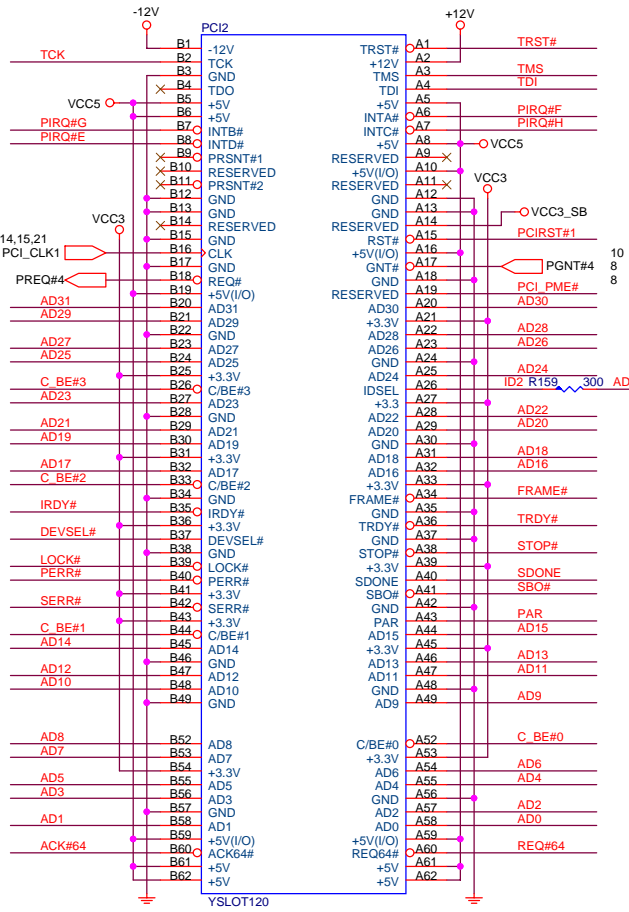
PCI SLOT 1 (PCI VER: 2.2 COMPLY)

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

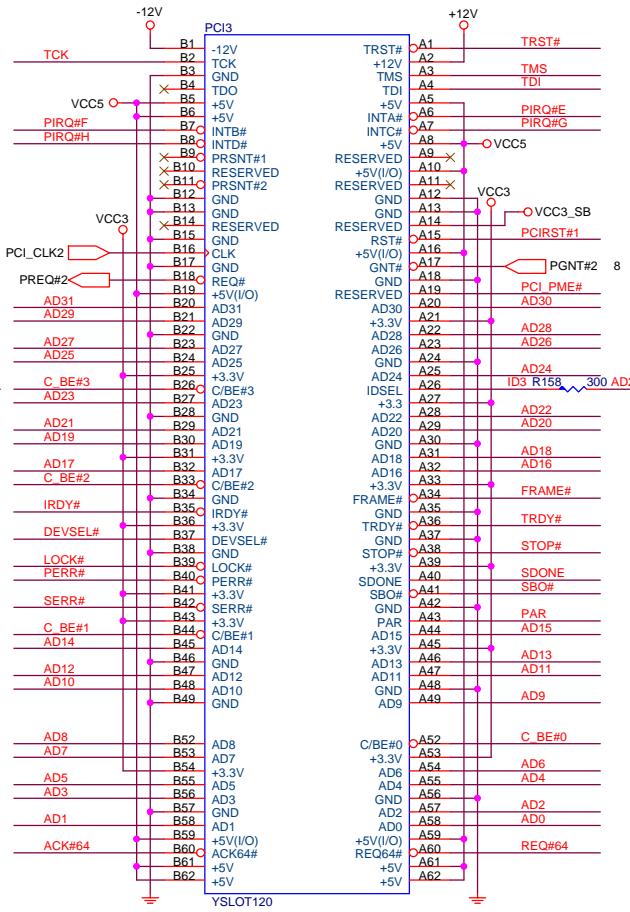
PCI SLOT 3 (PCI VER: 2.2 COMPLY)



IDSEL = AD26
MASTER = PREQ#0
PIRQ#G

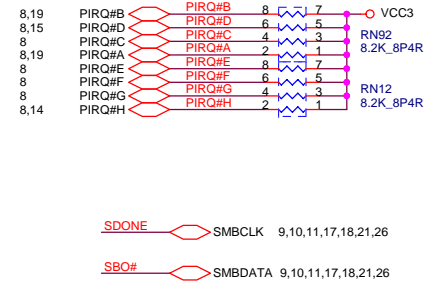
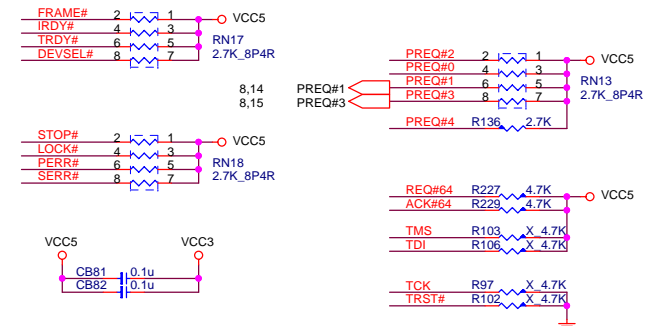


IDSEL = AD25
MASTER = PREQ#4
PIRQ#F

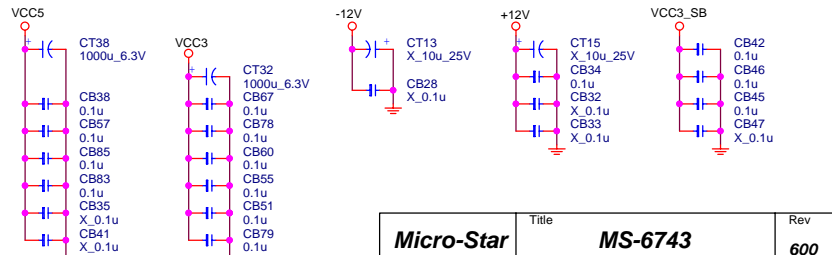


IDSEL = AD28
MASTER = PREQ#2
PIRQ#E

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



Micro-Star	Title	MS-6743	Rev	600
Document Number				
PCI 1 & 2 & 3 Slots				
Last Revision Date:				
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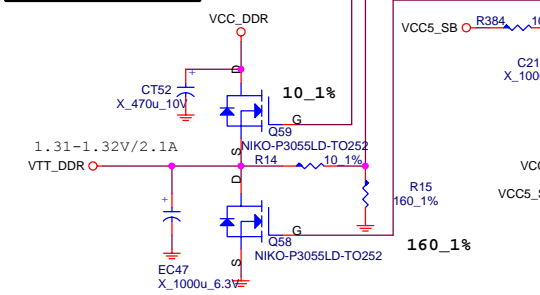
Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	0V
MEM_STR	Main	Standby	0V

SEL0	5VUSB
H	2 MOSFET
L	1 MOSFET

**S50# pin function (Hi level = 5V)
same as 5VUSB (Hi level = 12V)
5VUSB USE 2 MOSFET

**INPUT 2 AND 3 MUST BE HI LEVEL WHEN USE OUTPUT 1 AND 2 FOR GPIO FUNCTION

DDR VTT Power

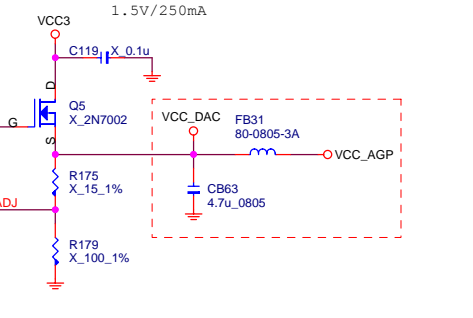
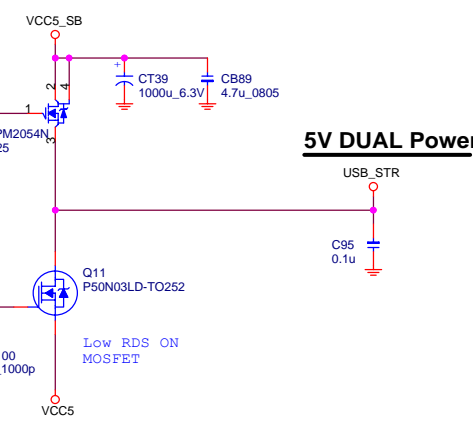
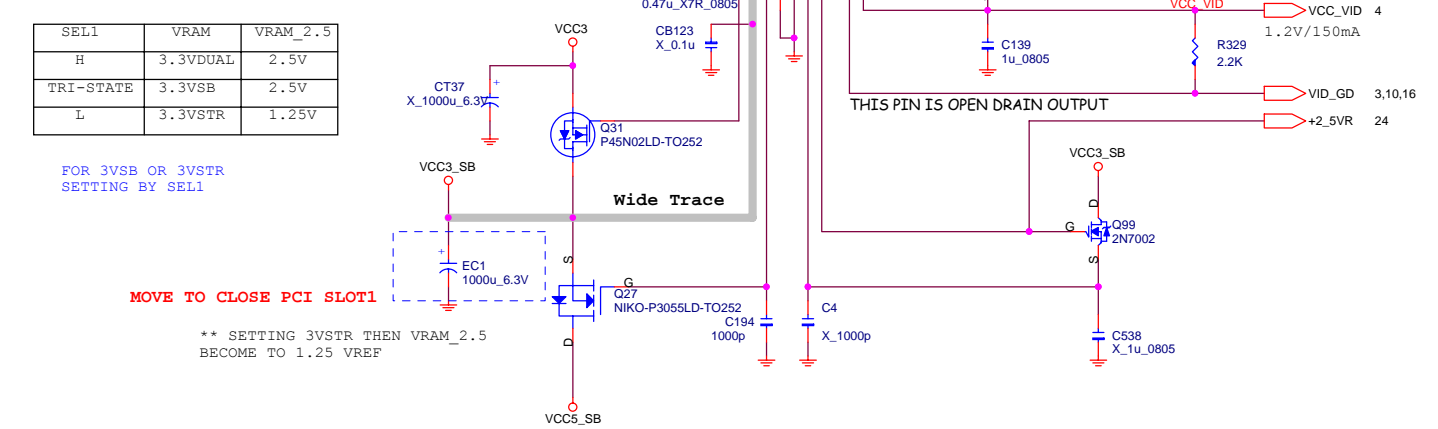


SEL1	VRAM	VRAM_2.5
H	3.3VDUAL	2.5V
TRI-STATE	3.3VSB	2.5V
L	3.3VSTR	1.25V

FOR 3VSB OR 3VSTR SETTING BY SEL1

MOVE TO CLOSE PCI SLOT1

** SETTING 3VSTR THEN VRAM_2.5 BECOME TO 1.25 VREF



GMCH VCC_DAC Voltage Supplier

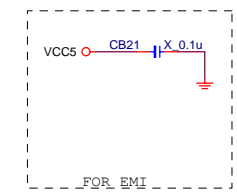
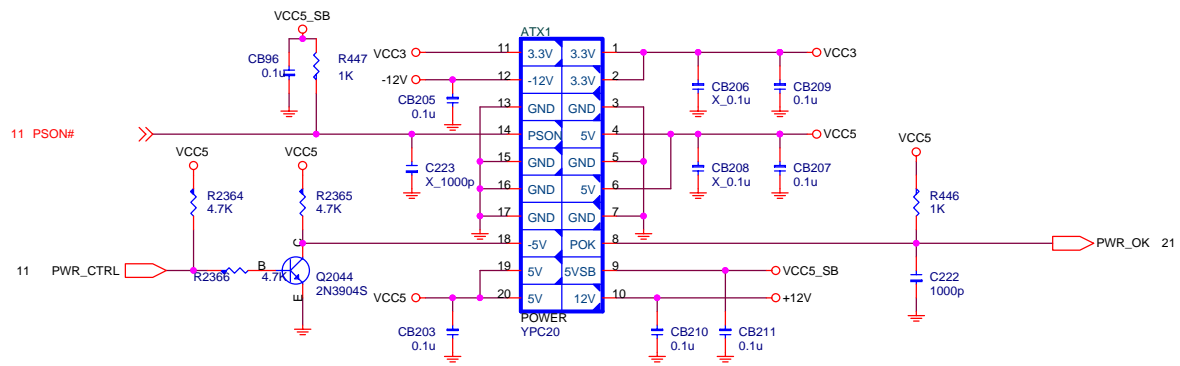
Place MOSFET near CPU

THIS PIN IS OPEN DRAIN OUTPUT

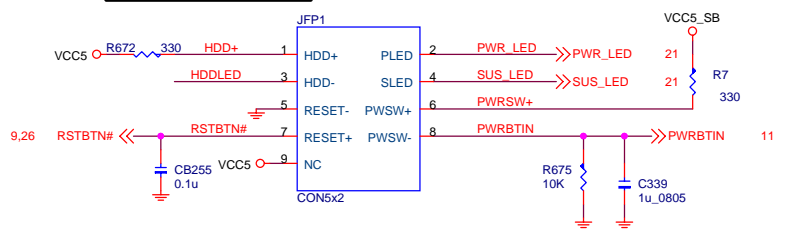
Wide Trace

Micro-Star	Title	MS-6743	Rev	600
Document Number		ACPI (MS-5)		
Last Revision Date:		Thursday, September 30, 2004		
Sheet	21	of	30	

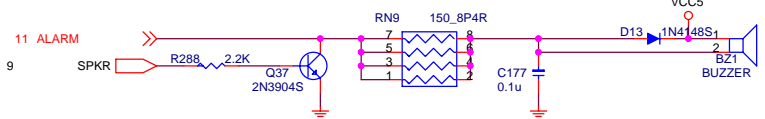
ATX CONNECTOR



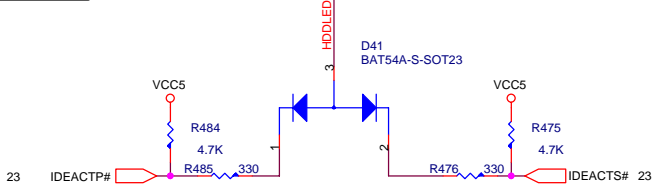
Intel Front Panel



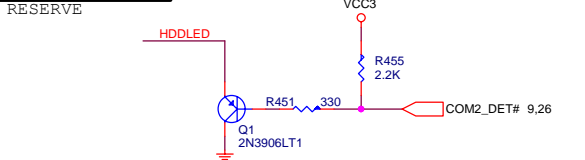
BUZZER



IDE LED

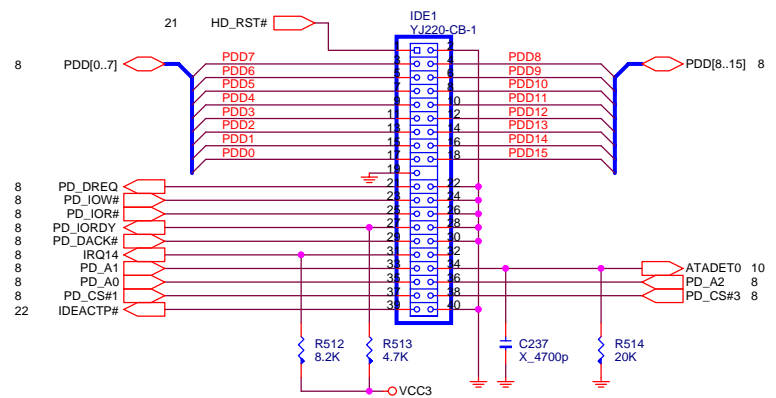


SERIAL ATA LED

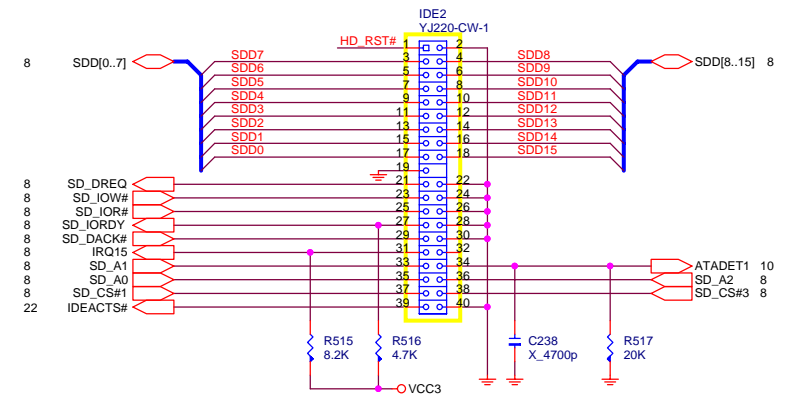


Micro-Star	Title MS-6743	Rev 600
Document Number ATX Connector & Front Panel		
Last Revision Date: Thursday, September 30, 2004		Sheet 22 of 30

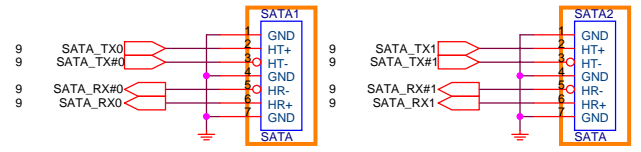
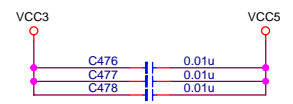
PRIMARY IDE BLOCK



SECONDARY IDE BLOCK

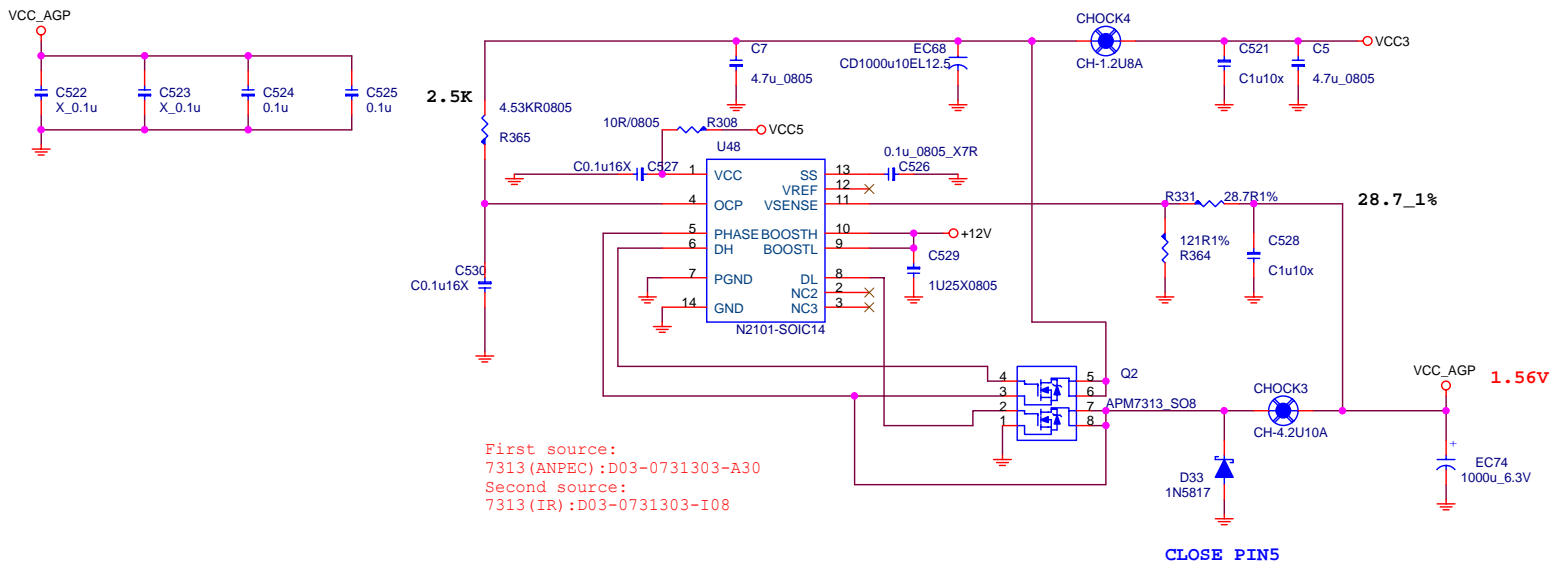


SERIAL ATA CONNECTOR BLOCK



20:5:7:5:20<5"

Micro-Star	Title MS-6743	Rev 600
Document Number IDE& SATA CONNECTORS		
Last Revision Date: Thursday, September 30, 2004	Sheet 23 of 30	

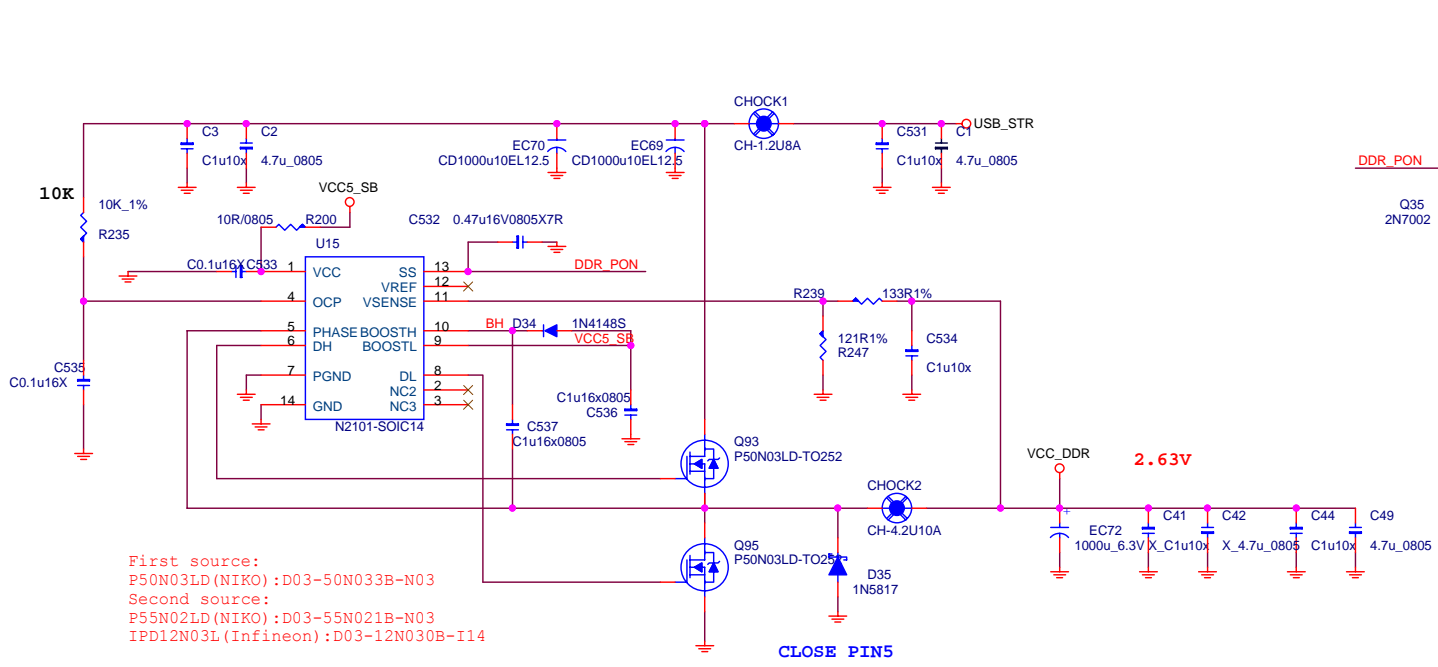
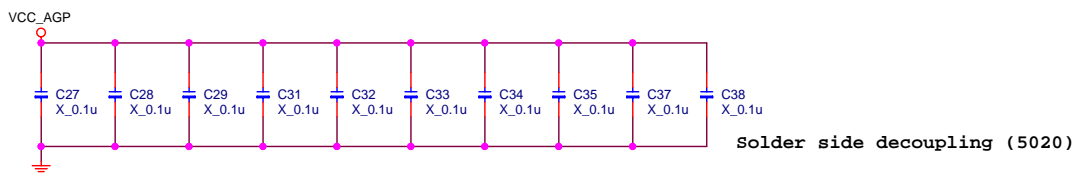


AGP Power

1.5V / 4A (NB) + 1A (SB) + 2A (AGP)

First source:
7313 (ANPEC) :D03-0731303-A30
Second source:
7313 (IR) :D03-0731303-I08

CLOSE PINS

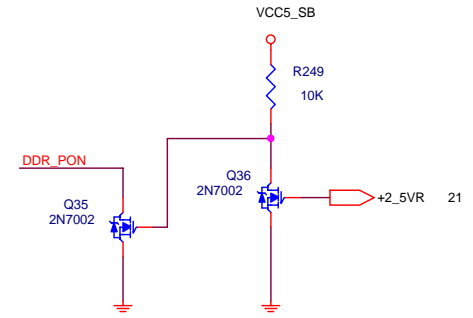


DDR Power

2.5V / 7A (DIMM) + 5.1A (NB)

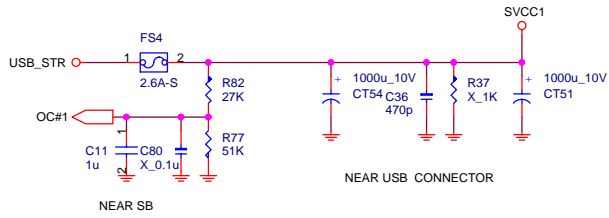
First source:
P50N03LD (NIKO) :D03-50N033B-N03
Second source:
P55N02LD (NIKO) :D03-55N021B-N03
IPD12N03L (Infineon) :D03-12N030B-I14

CLOSE PINS

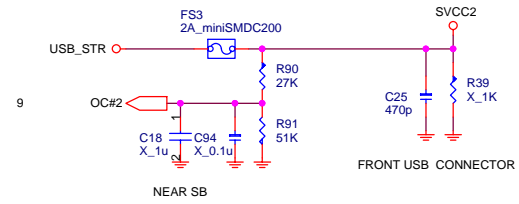


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Document Number		AGP & DDR POWER		
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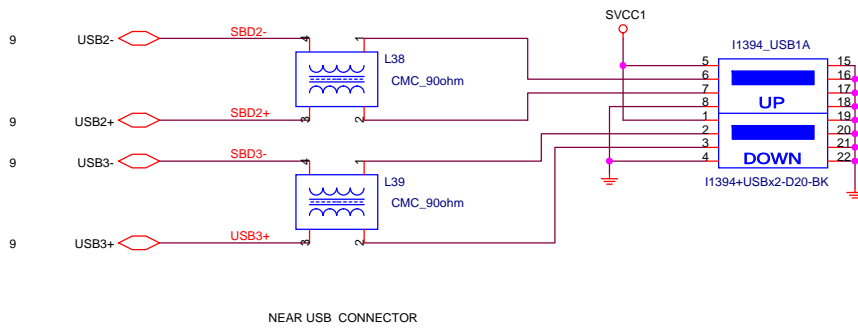
POWER CIRCUIT FOR USB PORT 0,1,2,3



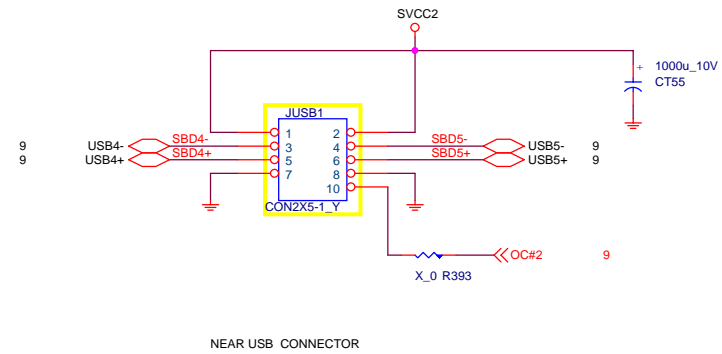
POWER CIRCUIT FOR USB PORT 4,5,6,7



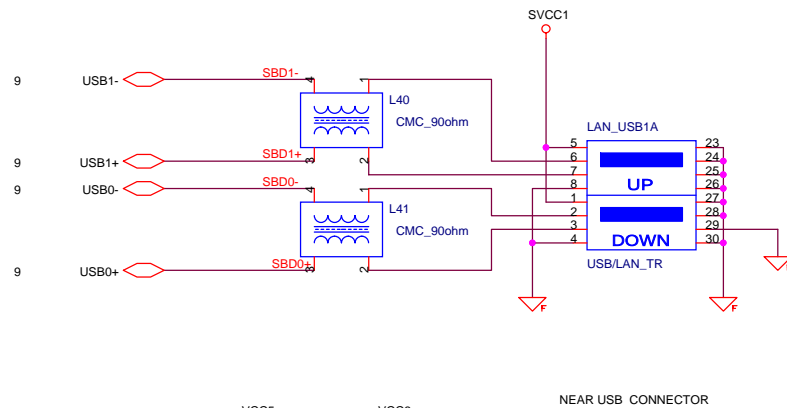
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



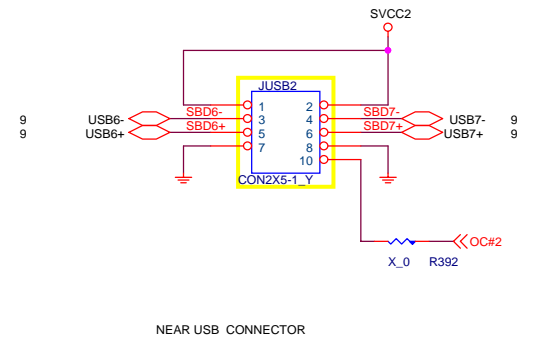
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



REAR PANEL USB CONNECTOR FOR USB PORT 2,3



FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



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ICH5

GPIO Pin	Type	Function	Power well
GPIO 0	I	PREQ#A	MAIN
GPIO 1	I	PREQ#B	MAIN
GPIO 2	I	PIRQ#E	MAIN
GPIO 3	I	PIRQ#F	MAIN
GPIO 4	I	PIRQ#G	MAIN
GPIO 5	I	PIRQ#H	MAIN
GPIO 6	I	GPI6	MAIN
GPIO 7	I	GPI7	MAIN
GPIO 8	I	SIO_PME#	RESUME
GPIO 9	I	OC4#	RESUME
GPIO 10	I	OC5#	RESUME
GPIO 11	I	TEMP_THERM#	RESUME
GPIO 12	I	SIO_SMI#	RESUME
GPIO 13	I	GPI13	RESUME
GPIO 14	I	OC#6	RESUME
GPIO 15	I	OC#7	RESUME
GPIO 16	O	PGNT#A	MAIN
GPIO 17	O	PGNT#B	MAIN
GPIO 18	O	GPO18	MAIN
GPIO 19	O	GPO19	MAIN
GPIO 20	O	GPO20	MAIN
GPIO 21	O	GPO21	MAIN
GPIO 22	OD	GPO22	MAIN
GPIO 23	O	BIOS_WP#	MAIN
GPIO 24	I/O	GPIO24	RESUME
GPIO 25	I/O	LAN_DISABLE#	RESUME
GPIO 27	I/O	GPIO27	RESUME
GPIO 28	I/O	GPIO28	RESUME
GPIO 32	I/O	GPIO32	MAIN
GPIO 33	I/O	COM2_DET#	MAIN
GPIO 34	I/O	GPIO34	MAIN
GPIO 40	I	PREQ#4	MAIN
GPIO 41	I	GPI41	MAIN
GPIO 48	O	PGNT#4	MAIN
GPIO 49	OD	CPU_GD	MAIN

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQG PIRQH PIRQE PIRQF	PCI_REQ#0 PCI_GNT#0	AD26	PCICLK0
PCI Slot 2	PIRQF PIRQG PIRQH PIRQE	PCI_REQ#4 PCI_GNT#4	AD25	PCICLK1
PCI Slot 3	PIRQE PIRQF PIRQG PIRQH	PCI_REQ#2 PCI_GNT#2	AD28	PCICLK2
1394	PIRQD	PCI_REQ#3 PCI_GNT#3	AD27	1394_CLK
LAN	PIRQH	PCI_REQ#1 PCI_GNT#1	AD24	LAN_CLK

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM 2	A2H	MCLK_A3/MCLK_A#3 MCLK_A4/MCLK_A#4 MCLK_A5/MCLK_A#5
DIMM 3	A4H	MCLK_B0/MCLK_B#0 MCLK_B1/MCLK_B#1 MCLK_B2/MCLK_B#2
DIMM 4	A6H	MCLK_B3/MCLK_B#3 MCLK_B4/MCLK_B#4 MCLK_B5/MCLK_B#5

JUMPER SETTING

JBAT1	(1-2) NORMAL	(2-3) CLEAR
JAUD1	(5-6) W/O FRONT AUDIO (9-10) AUDIO	WITH FRONT AUDIO

SIO

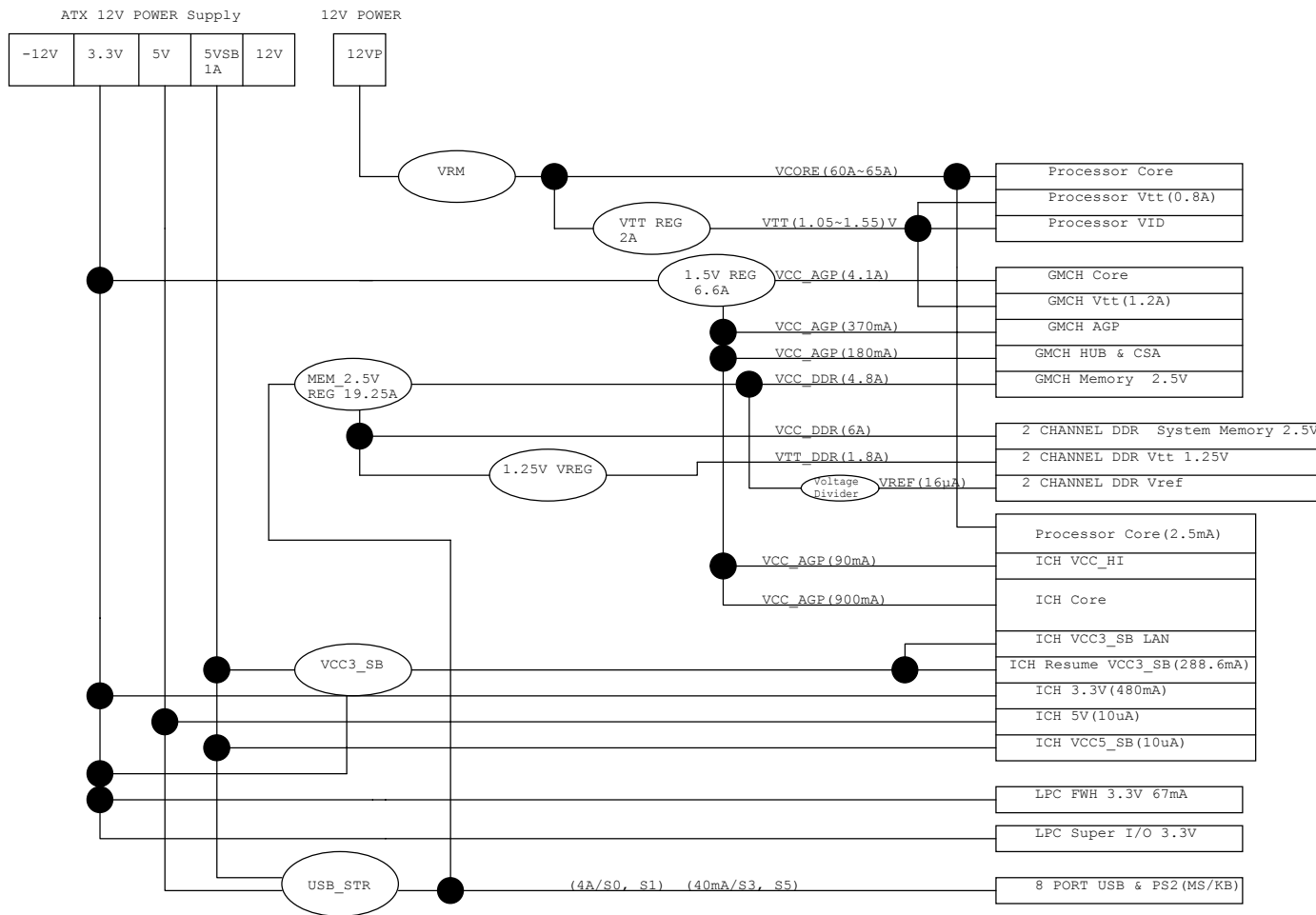
PIN NAME	USAGE	Input/Output	NOTES
GPIO10	UNUSED	INPUT	
GPIO11	UNUSED	INPUT	
GPIO12	UNUSED	INPUT	
GPIO13	UNUSED	INPUT	
GPIO14	UNUSED	OUTPUT	
GPIO15	VID5	INPUT	Low: VID add 0.0125V , High :by pass
GPIO16	UNUSED	OUTPUT	
GPIO17	UNUSED	OUTPUT	
GPIO20	UNUSED	OUTPUT	
GPIO21	SMBCLK_ISO	INPUT	SMBUS CLOCK
GPIO22	SMBDATA_ISO	INPUT /OUTPUT	SMBUS DATA
GPIO23	POWER_LED	OUTPUT	Default used MS-5
GPIO24	UNUSED	OUTPUT	
GPIO25	UNUSED	OUTPUT	IRRX
GPIO26	UNUSED	OUTPUT	
GPIO27	UNUSED	OUTPUT	
GPIO30	SLP_S3#	INPUT	S3 state indicator signal
GPIO31	PS_ON#	OUTPUT	Connector to Power Supply to turn on Power
GPIO32	UNUSED	OUTPUT	
GPIO33	UNUSED	OUTPUT	
GPIO34	UNUSED	OUTPUT	
GPIO35	UNUSED	OUTPUT	

PCI RESET DEVICE

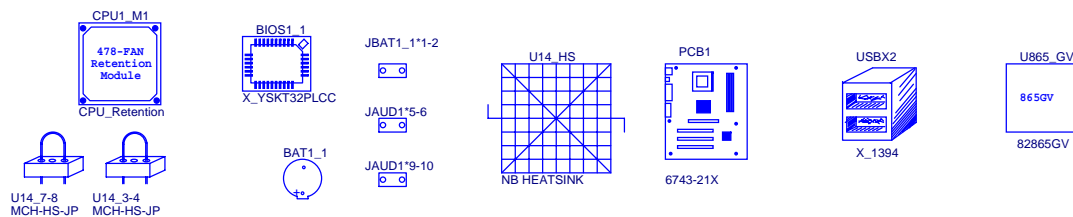
Signals	Target
PCIRST#1	PCI slot 1-3, 1394
PCIRST#2	Super I/O, AGP slot
PCIRST_ICH5#	Northbridge , FWH
HDDRST#	Primary, Scondary IDE

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POWER DELIVERY MAP



6743L1-L PART



For GV
 (-)C155,C524,C525,CB72,CB77
 (-)CB80
 (-)Q18,Q19
 (-)Q22
 (-)R196
 (-)R189,R194,R195,R225
 (-)R190
 (-)R31
 (-)R231
 (-)AGP1
 (-)EC74

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Revision History (Changes from Rev 20C)

Sheet	Description
11	Winbond Super I/O : Add R2362 0 ohm between pin102 and pin103
13	Intel Front Audio Connector Add R631 10K
14	Change LAN RTL8110S/8101C LAN Connector with Tranformer/Common Choke
15	VRM Support VRM10.0 FMB 1.5
22	Tyco New S-ATA Connector Change SATA footprint for LG request Add S-ATA HDD LED
23	Remove 1394-NEC PD72874
29	Remove Printer Port Protection Diode Add 4 pics Cn and 1 pic Cap for Protection Remove HP Printer Port / Keep Circuit
	6743v210 Forbidden :YAGEO-CN For LG C12-2711013-Y01(Location:CN4) C12-1811013-Y01(Location:CN1.CN2)

Revision History (Changes from Rev 210)

Sheet	Description
11	Winbond Super I/O : 83627HF To 83627THF
13	Audio Codec CMI9739A to CMI9761A

Revision History (Changes from Rev 21A)

Sheet	Description
11	Super I/O Temp Sense Circuit Modify
	Mechanical Issue
	EMI Issue
15	Add PCI NEC 1394

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