Harris Semiconductor

APPNOTE

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Harris Wireless Products

PRISM™ DSSS PC Card Wireless LAN Description

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Introduction

The PRISM™ PC Card Wireless LAN Kit is provided with two reference wireless LAN PC Cards. This note will detail the RF and analog design of these cards. The physical layer (PHY) sections of these PC Cards are described in detail in the following sections. The medium access control (MAC) section of the PC Cards is described in detail in the pending AMD application note titled "Wireless LAN DSSS PC Card Reference Design" [1].

Figure 1 shows a block diagram of the reference radio design. This radio has been designed to conform to the draft IEEE 802.11 specification but does not include the antenna diversity selection.

The specifications of the PC Card wireless LAN are as follows:

Receive Specifications

- Frequency Range . . . . . 2.4GHz - 2.4835GHz
- Step Size 1MHz
- Cascaded Noise Figure 6.8dB
- Sensitivity . . . . . -93dBm, 1 MBPS, 8E-2 FER (Note 1)
-90dBm, 2 MBPS, 8E-2 FER (Note 1)
- Input Intercept Point . . . . . -17dBm
- IF Frequency 280MHz
- IF Bandwidth 17MHz
- Image Rejection 80dB
- Adjacent Channel Rejection . . . . . >35dB
- Supply Voltage . . . . . 2.7V - 5.5V

Transmit Specifications

- Frequency Range . . . . . 2.4GHz - 2.4835GHz
- Step Size 1MHz
- Output Power . . . . . +18dBm
- Spurious Outputs . . . . . Targeting ISM/802.11
- Transmit Spectral Mask . . . . . -32dBr at First Side-Lobe
- IF Frequency 280MHz
- Supply Voltage . . . . . 2.7V - 5.5V

General Specifications

- Targeted Standard . . . . . IEEE 802.11
- Data Rate . . . . . 1 MBPS DBPSK
2 MBPS DQPSK
- Range . . . . . 400ft Indoor (Note 2)
3700ft Outdoor (Note 2)
- RX/TX Switching Speed 2µs
- Power Savings Modes
  - Mode 1: 190mA at 1µs Recovery (Notes 3, 4)
  - Mode 2: 70mA at 25µs Recovery (Notes 3, 4)
  - Mode 3: 60mA at 2ms Recovery (Notes 3, 4)
  - Mode 4: 30mA at 5ms Recovery (Notes 3, 4)
- Average Current
(Without Power Savings Modes) . . . . . 298mA (Note 5)
- Average Current
(With Power Savings Modes) . . . . . 60mA (Note 6)

NOTES:

1. FER = Frame Error Rate or Packet Error Rate.
2. Range Test using AND-C-107 omnidirectional antenna.
3. Supply current includes AM79C930 MAC Processor.
4. Recovery time is for the PRISM™ 2.4GHz Chip Set only and does not include programming latency of the AM79C930 MAC Processor.
5. Based on average current consumption for "typical" application.
6. Power savings modes refer to AN9665. Average radio current consumption for "typical" application.

Receive Processing

Referring to the block diagram in Figure 1, a single antenna is used. Up to two antennas are supported in the HSP3824[2] Baseband Processor to implement diversity, countering the adverse effects of multi-path fading. From the antenna, the received input is applied to FL1, a Toko TDF2A-2450T-10 two pole dielectric bandpass filter, which is used to provide image rejection for the receiver. The IF frequency is 280MHz, and low-side injection is used, thereby placing the received image 560MHz below the tuned channel. FL1 also provides protection for the RF front-end from out of band interfering signals.

TABLE 1. PRISM™ CASCADED FRONT-END ANALYSIS

STAGE	G	GC	F	FC	IP30	IP30C	IP3IC
FL1 RF FILTER	- 2.0	- 2.0	2.0	2.0	100.0	100.0	102.0
HFA3925 T/R SWITCH	- 1.2	- 3.2	1.2	3.2	34.0	34.0	37.2
HFA3424 LNA	13.0	9.8	2.0	5.2	11.1	11.0	1.2
ATTENUATOR	- 5.0	4.8	5.0	5.5	100.0	6.0	1.2
HFA3624 LNA	15.6	20.4	3.8	6.0	15.0	14.1	- 6.3
FL2 RF FILTER	- 3.0	17.4	3.0	6.0	100.0	11.1	- 6.3
HFA3624 MIXER	3.0	20.4	12.0	6.3	4.0	3.6	- 16.8
FL3 IF FILTER	- 10.0	10.4	10.0	6.4	100.0	- 6.4	- 16.8
HFA3724[6] IF STRIP	0.0	10.4	7.0	6.8	100.0	- 6.4	- 16.8

Cascaded Gain = 10.4dB
Cascaded NF = 6.8dB
Cascaded Input IP3 = -16.8dBm

NOTE: G (individual stage gain, dB), GC (cumulative gain, dB), F (NF, dB), FC (cumulative NF, dB), IP3O (individual stage output IP3, dBm), IP3OC (cumulative output IP3, dBm), IP3IC (cumulative input IP3, dBm)

The T/R switch is integrated in the HFA3925[3] RF Power Amplifier (RFPA). The HFA3925 RFPA operates from the unregulated 5V PC Card supply. Following the T/R switch, the HFA3424[4] Low Noise Amplifier (LNA) is used to set the receiver noise figure. The HFA3424 LNA operates from a regulated 3.5V supply.

A trade-off between noise figure and input intercept point exists in any receiver, to balance these conflicting requirements in the PRISM™ radio, an attenuator follows the HFA3424 LNA. The attenuation chosen is 5dB. To improve noise figure, this attenuation may be reduced; alternatively, to improve input intercept point, this attenuation may be increased. The cascaded front-end noise figure and input intercept point analysis is shown in Table 1.

Next, the signal enters the HFA3624[5] RF/IF Converter LNA section, which aids in setting receiver NF. FL2 is used to suppress image noise generated in both the HFA3424 LNA and the HFA3624 LNA, and is a Murata LFJ30-03B2442B084 two pole monolithic LC bandpass filter. Only modest attenuation at the image frequency is required. The insertion loss is not critical, since at this point in the receiver, component loss or NF is offset by the preceding gain stages. All sections of the HFA3624 RF/IF Converter operate from a regulated 3.5V supply.

Down-conversion from the 2.4GHz - 2.5GHz band is performed in the HFA3624 RF/IF Converter mixer section. As previously mentioned, the IF center frequency is 280MHz, and low-side local oscillator (LO) injection is used. A discrete LC matching network is used at the mixer output to differentially combine the IF outputs, as well as impedance match to a 50Ω environment. A trimmer capacitor is used as part of the narrow-band matching network. An alternative, broadband matching network is described in the HFA3624 RF/IF Converter application note, and does not require any tunable elements. A direct impedance match to the IF filter, FL3 could be implemented if desired. The 50Ω environment was chosen to allow ease in measurement of portions of the radio with external test equipment.

The IF receive filter, FL3, is a Toyocom TQS-432 SAW bandpass filter. The center frequency is 280MHz, the 3dB bandwidth is 17MHz, and the differential group delay is less than 100ns. Insertion loss is typically 6dB, making it ideal for single-conversion systems. The impedance of the SAW is 270Ω, and a series 33nH inductor is used to match the filter input to 50Ω. The SAW output is matched directly to the IF input of the HFA3724 Quadrature IF Modulator/Demodulator, using a shunt 56nH inductor. This presents a 250Ω source impedance to the limiter input, thereby optimizing the limiter's NF.

In the receive mode, the HFA3724 Quadrature IF Modulator/Demodulator provides two limiting amplifiers, a quadrature baseband demodulator, and two baseband low pass filters. All sections of the HFA3724 operate from a regulated 3.5V supply. The first limiting amplifier establishes the NF of the IF strip at approximately 7dB. A discrete one pole LC differential filter, FL4, is placed between the two limiters to restrict the noise bandwidth of the first limiter. As both limiters exhibit a broadband response, with over 400MHz bandwidth, a noise bandwidth reduction filter is appropriate to ensure that the second limiter is fully limiting on the front-end noise within the signal bandwidth, as opposed to the broadband noise generated by the first limiter. This filter has a center frequency of 280MHz, and a 3dB bandwidth of 50MHz. It consists of a fixed 10nH inductor and a fixed 20pF capacitor, as described in the HFA3724 data sheet.

At the output of the limiters, a 200mV$_{P-P}$ differential signal level is maintained under all input conditions. This limited signal is then mixed in quadrature to baseband in the HFA3724 Quadrature IF Modulator/Demodulator. The LO needed for the quadrature mixing is applied at twice the IF frequency, or

560MHz. A divide by two circuit then provides an accurate quadrature LO for the mixers. The baseband outputs of the quadrature mixers are AC coupled off-chip to the integrated fifth order Butterworth filters. The output levels of the low pass filters are nominally 500mV$_{P-P}$ single-ended, and are intended to be AC coupled to the HSP3824 Baseband Processor. The AC coupling time constant is approximately 25 times longer than the symbol period, and is implemented with 0.01µF series capacitors. These coupling capacitors must be taken into account, however, when estimating the time it takes to power up or awaken from sleep mode.

At the input to the HSP3824 Baseband Processor, the quadrature signals are analog to digital converted in wideband 3 bit converters. The signals are spread spectrum with no DC term, so it is feasible to AC couple the signals to the ADCs and avoid DC bias offsets. The signal at this point has been limited to a constant IF amplitude and then passed through two separate mixer and low pass filter paths. The component variations in these two paths can introduce offsets in amplitude and phase and can also use up some of the headroom in the ADCs. The maximum amplitude variation is 2dB and the maximum phase balance variation is 4 degrees. Since the signal is limited, the IF signals will have low peak to average ratios even with noise as an input. The I and Q signals will have sinusoidal properties with PSK modulation imposed. It is their combined vector magnitude that is limited, not their individual amplitudes. To optimize the demodulator's performance, the ADCs are operated at the point where they are at full scale on either I or Q one third of the time. To maintain this operating point in the face of component variations, there is an active adjustment of the ADC reference voltage by feedback. This avoids the necessity of allowing extra headroom for the variation. The adjustment circuit is very slow and averages the energy from the two channels over both packet and noise conditions.

The HSP3824 Baseband Processor correlates the PN spreading to remove it and to uncover the differential BPSK or QPSK data. The processor initially uses differential detection to identify and lock onto the signal. It then makes measurements of the carrier and symbol timing phase and frequency and uses these to initialize tracking loops for fast acquisition. Once demodulating and tracking, the processor uses coherent demodulation for best performance. Since this radio uses a spread spectrum signal, the signal to noise ratio (SNR) in the chip rate bandwidth is about 0dB when the demodulator is at the desired bit error rate in BPSK. The radio operates with about 2.5dB of implementation loss relative to theoretical performance and achieves a sensitivity of -93dBm with BPSK.

The HSP3824 Baseband Processor provides differential decoding and descrambling of the data to prepare it for the Media Access Controller (MAC). The MAC is an AMD AM79C930 PCnet™-Mobile controller. All packet signals have a preamble followed by a header containing a start frame delimiter (SFD), other signal related data and a cyclic redundancy check (CRC). The MAC processes the header data to locate the SFD, determine the mode and length of the incoming message and to check the CRC. The MAC then processes the packet data and sends it on through the PC Card interface to the host computer. The MAC checks the packet data CRC to determine the data purity. If corrupted data is received, a retransmission is requested by the MAC which handles the physical layer link protocols.

Transmit Processing

Data from the host computer is sent to the MAC via the PC Card interface. Prior to any communications, however, the MAC sends a Request to Send packet to the other end of the link and receives a Clear to Send packet. The MAC then formats the data by appending it to a preamble and header and sends it on to the HSP3824 Baseband Processor which clocks it in. The HSP3824 Baseband Processor scrambles the packet and differentially encodes it before applying the spread spectrum modulation. The data can be either DBPSK or DQPSK modulated at 1 MSPS and is a baseband quadrature signal with I and Q components. The spreading is an 11 chip Barker sequence that is clocked at 11MHz and is modulated with the I and Q data components. These are then output to the HFA3724 as CMOS logic signals.

Transmit quadrature single-bit digital inputs are applied to the HFA3724 Quadrature IF Modulator/Demodulator from the HSP3824 Baseband Processor. These inputs are attenuated by 1/7 and DC coupled to the fifth order Butterworth low pass filters, which are used to provide shaping of the phase shift keyed (PSK) signal. The required transmit spectral mask, at the antenna, is -30dBc at the first side-lobe relative to the main-lobe. An unfiltered PSK waveform would have the first side-lobe suppressed only -13dBc. The fifth-order filters are tuned to an approximate 7.7MHz cutoff, using a 909Ω resistor external to the HFA3724.

In the PC Card wireless LAN, the goal is to control the regrowth of the side-lobes, with the HFA3925 RFPA dominating the regrowth. This will result in maximum transmitted power available. To achieve this goal, once the PSK waveform is filtered at baseband, all remaining transmit elements are operated at a 6dB back-off from compression, except for the HFA3925 RFPA, which is operated at less back-off.

The low pass filters provide initial shaping of the PSK waveform. Final shaping is provided by a transmit IF filter, FL5, a Toyocom TQS-432 SAW bandpass filter. The low pass filter outputs are off-chip AC coupled to the quadrature up-converter in the HFA3724. As in the receive mode, the baseband AC coupling time constant is approximately 25 times longer than the symbol period, and is implemented with 0.01µF series capacitors. The same twice IF frequency LO used previously is also used in this up-conversion. The IF output of the HFA3724 is reactively matched to FL5, with a 250Ω resistive load presented to the HFA3724. A shunt 47nH inductor, in parallel with a 316Ω resistor, is used to provide this match, negate the effects of board and component capacitance, and provide a DC return to V_{CC} to prevent saturation in the IF output stage of the HFA3724.

The output of FL5 is terminated in a 200Ω potentiometer that is used for transmit gain control. A shunt 47nH inductor is used to negate the effects of parasitic board and component shunt capacitance, as well as match the SAW output to the potentiometer. This potentiometer has it's center wiper

connected to the HFA3624 RF/IF Converter transmit IF input, which has an input resistance of approximately 3kΩ. By varying the potentiometer, the gain of the transmit chain is controlled, allowing for precise control of the signal back-off at the HFA3925 RFPA. Therefore, this potentiometer is adjusted to achieve the desired compromise between transmit output power and the main-lobe to side-lobe ratio of the output PSK waveform, typically -32dBc to -35dBc.

Upconversion to the 2.4GHz - 2.5GHz band is performed in the HFA3624 RF/IF Converter transmit mixer. The mixer output is filtered with FL6, a Murata LFJ30-03B2442B084 two pole monolithic LC bandpass filter. This filter suppresses the LO feedthrough from the mixer, and selects the upper sideband. The transmit buffer in the HFA3624 RF/IF Converter preamplifies the selected sideband, easing the requirement for HFA3925 RFPA gain.

FL7, a Toko TDF2A-2450T-10 two pole dielectric bandpass filter, is used to further suppress both the transmit LO leakage and the undesired sideband.

The HFA3925 RFPA amplifies the transmit signal to a level of approximately +20dBm, as measured at the T/R switch output. This represents a back-off from 1dB compression of approximately 4.5dB. Transmit side-lobe performance is approximately -32dBc to -35dBc with this level of back-off.

The HFA3925 RFPA is the only physical layer component that operates directly from the 5V PC Card supply. To supply the needed negative gate bias to the HFA3925 RFPA, a ICL7660SIBA[7] charge pump is used. A second potentiometer is used to adjust the drain current on the third stage of the HFA3925 to a quiescent operating current of 90mA, as measured through a one ohm sense resistor.

A logic-level PMOS switch, RF1K49093[8], is used to control the drain supply voltage to the HFA3925 RFPA, and implement a power down mode when receiving. As the RF1K49093 is a dual device, the other PMOS switch is used to control the supply voltage to the HFA3424 LNA and implement a power down mode when transmitting. A 2N2222 NPN transistor is used to level shift the 3.5V logic level from the AM79C30 MAC to drive the 5V PMOS switch gates, as well as the 5V HFA3925 RFPA T/R control gate.

Following the T/R switch, FL1 is reused in the transmit mode to attenuate harmonics generated in the HFA3925 RFPA, as well as providing additional suppression of the LO. As the loss of FL1 is approximately 2dB, the amount of transmit power available at the antenna is approximately +18dBm.

Synthesizer Section

The dual frequency synthesizer section uses the HFA3524[9] Synthesizer and two voltage controlled oscillators to provide a tunable 2132MHz - 2204MHz first LO, and a fixed 560MHz second LO. Both feedback loops use a 1MHz reference frequency that is derived from a 22MHz MF Electronics T3391-22.0M crystal oscillator. This crystal oscillator currently limits the operating temperature range of the radio to 0°C to 70°C. Both passive loop filters were designed to have loop bandwidths of 10kHz, and phase margins of 50 degrees. The feedback loop analysis is described in the HFA3524 Synthesizer evaluation board documentation. All components in the synthesizer section operate from a regulated 3.5V supply.

The tunable 2132MHz to 2204MHz first LO oscillator is a Z-Communications SMV2100L VCO. To ensure operation at low tuning voltages, a start-up circuit was added to force the tuning voltage from the HFA3524 Synthesizer RF charge pump to a high state for a short period (~1ms) following HFA3524 programming. A 2N2907 PNP transistor was used to implement this function, and the AM79C930 MAC device provides the control signal. The output level of the first LO to the HFA3624 RF/IF Converter is attenuated to approximately -3dBm.

The fixed 560MHz second LO oscillator is a discrete design, using a Phillips BFR505 transistor and a Siemens BBY51 varactor, as described in the HFA3524 Synthesizer evaluation board documentation. The output level of the second LO to the HFA3724 Quadrature IF Modulator/Demodulator is attenuated to approximately -6dBm and a three pole low pass filter is included to preserve the duty cycle of the output. High even order components in the second LO can result in offsets from a 50% duty cycle, and will degrade the quadrature phase accuracy of the HFA3724. A transconductance network is used at the HFA3724 LO input to convert the second LO voltage into a current, as recommended in the HFA3724 data sheet. As the HFA3524 Synthesizer auxiliary IF input covers the 560MHz range, the internal divide-by-two LO buffer output of the HFA3724 is disabled, as recommended in the HFA3724 data sheet.

Regulator Section

Linear voltage regulators are used to provide filtering and isolation from the 5V PC Card input supply. An additional advantage of using voltage regulators is a savings in overall supply current, as all of the components that are regulated consume less current at a 3.5V operating point, as opposed to a 5V operating point. The only components operating directly from the 5V supply are the HFA3925 RFPA, in order to maximize RF output power, and the PC Card interface. Sections of the AM79C930 MAC controller, as well as the host computer may use 5V logic levels.

A total of three regulators, 3.5V Toko TK11235MTL, are used in the PC Card wireless LAN. One regulator is devoted to the HSP3824 Baseband Processor and AM79C930 MAC devices. The remaining two regulate the RF and IF sections of the radio. One regulator supplies voltage to the synthesizer section, the HFA3424 LNA, and the HFA3624 RF/IF Converter. The second regulator supplies voltage to the HFA3724 Quadrature IF Modulator/Demodulator.

References

[1] *AMD Application Note, Wireless LAN DSSS PC Card Reference Design*, application note # pending.

[2] *HSP3824*, data sheet, AnswerFAX document #4064, 407-724-7800.

[3] *HFA3925*, data sheet, AnswerFAX document #4132, 407-724-7800.

[4] *HFA3424*, data sheet, AnswerFAX document #4131, 407-724-7800

[5] *HFA3624*, data sheet, AnswerFAX document #4066, 407-724-7800.

[6] *HFA3724*, data sheet, AnswerFAX document #4067, 407-724-7800.

[7] *ICL7660S*, data sheet, AnswerFAX document #3179, 407-724-7800.

[8] *RF1K49093*, data sheet, AnswerFAX document #3969, 407-724-7800.

[9] *HFA3524*, data sheet, AnswerFAX document #4062, 407-724-7800.

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