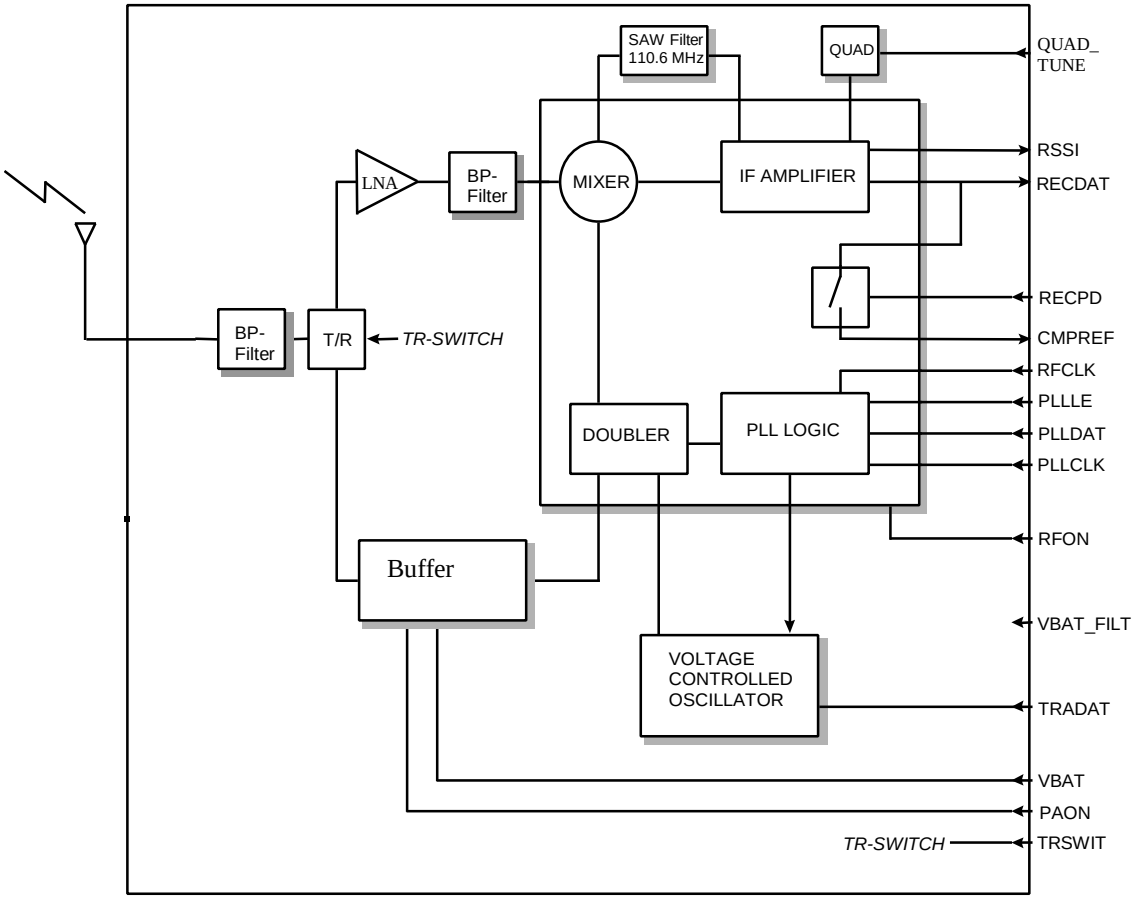
Circuit Description for the RF part

This document describes the functionality of the RF part of Activa. The RF is based on the LMX 3162 single chip RF from National Semiconductor. Two to other main components are the ALPS UREA630 VCO.



1.1.1 The Receive path

The receiver is a single conversion receiver with an IF frequency centered at 110.592 MHz. From the antenna the signal pass through a low loss ceramic filter and a TX/RX switch. After amplification in a bipolar LNA and further filtering in ceramic filter the signal is downconverted in a mixer in the LMX3162. A SAW filter is used after the mixer to perform the channel selection filtering.
An limiter discriminator demodulator is used. After the demodulation the signal is filtered. The detection is performed with a comparator.

1.1.2 The Frequency Synthesizer part

The frequency synthesizer consists of a VCO operating at half the wanted frequency controlled by an synthesizer in the LMX 3162. The VCO signal is doubled in a doubler in the LMX 3162 and split to the TX buffer and as LO signal for the receiver mixer. The TX modulation is performed as open loop modulation on the VCO.

1.1.3 The TX path

The signal from the doubled is amplified in a bipolar transistor buffer. The final amplification is performed by the buffer T108. The burst control is performed by an PNP transistor. After the PA the TX signal is feed through the TX/RX switch and the antenna filter.

2 VCO circuit

The VCO is a band switch VCO from ALPS (UREA630).

To avoid frequency drift and offset when the PA is turned on a separate 3.0 voltage regulator (LP2980) is used. The VBAT and VBAT_2 voltage typical drops 0.1 – 0.2 V when the PA is on.

The band switch signal (VCO_BND) is used to switch the VCO between RX (1172.8437 – 1213.1529 MHz) and TX (1200.4917 – 1240.8009 MHz). It is important that there is no voltage jump on the VCO_BND signal when the PA is turned on, as this will cause frequency drift.

The voltage on the CTR pin of the VCO determines the frequency of the VCO. This voltage comes from the synthesizer output and is filtered in the loop filter.

The used loop filter (C140=680pF,C141=2.2nF and R118=3.3kΩ) ensures that the lock time for the synthesizer is short (approx. 50 µs-100µs).

The VCO uses the open loop modulation scheme. This means that during transmission of a burst is the synthesizer powered down and the loop voltage is only hold by the capacitors in the loop filter. Due to this it is important that there is no leakage current in the capacitors. This can be fulfilled by using NP0 type capacitors.

In the open loop state, the modulation signal (TRADAT) is injected on the MOD pin of the VCO. The MOD signal shall have the same DC value during lock in as during the transmission burst. The TRADAT signal is gaussian shaped from the BMC. It is also possible to adjust the amplitude of the TRADAT signal in the BMC.

3 Doubler filter and Buffer amplifier

The primary purpose of the doubler filter (C159, L4) is to remove the fundamental frequency of the frequency doubled signal. Also the 3rd harmonic of the VCO frequency is attenuated.

The attenuation at 900 MHz is around 25dB and the attenuation at 2.8GZ is approx. 10 dB. The filter is designed as a wideband filter with a pass band of approx. 1.5- 2.0 GHz. This is to ensure that the attenuation of the wanted signal at 1880-1930 MHz is less than approx. 1dB taking worst case parameters into account.

The buffer amplifier (T108) has a collector current of 7mA and 7-8dB of small signal gain. The transistor is driven into saturation and gives approx. +2 dBm of output power. This signal is feed directly to the output.

The buffer and doubler are turned on during the blind slot before the burst to avoid any pulling of the VCO Thereby, it is also achieved that the buffer has an input signal before it is turned on.

4 Buffer amplifier with control circuit

The buffer amplifier is a BFP820. In order to match the output and perform some filtering of the harmonics a lowpass filter (C175, L7) is included between the IC and the TX/RX switch.

The control circuit is based on a PNP transistor with a LP filter (R130, C183). This circuit shapes the rising and falling edge of the power ramp.

5 TX/RX switch

The TX/RX switch consists of two PIN diodes (D3 D2) .
In TX mode the control voltage TRSWT is high. The control signal is feed into the diodes through a line. So D3 in conducting mode with a low resistance. This means that the power can flow from the Buffer to the antenna. The network and the length of the line acts like an quarterwave length transmission line.

In receive mode the control voltage is low and D3 diodes in off state and RXVreg is high so D2 is in on state. Thus, the impedance seen towards the PA is high while there is only a small attenuation of the RX signal. The current through the diodes is determined by R18 and R24 and is approximately 3mA.

6 Receiver Front End

After passing trough the first bandpass filter and the TX/RX filter the received signal is amplified in the LNA. The LNA is based on a BFP420 bipolar transistor. The LNA has about 14dB of gain and a noise figure on approx. 1.5dB. The DC current is approx. 4mA and is controlled by R28 and R26. C101 is used to obtain the input matching. The output matching is done by the coil L2.

After the LNA the a ceramic filter is used to obtain the full rejection on the image frequency and other frequencies.

7 IF and demodulator circuit

The IF chain consist of a SAW filter, an IF amplifier, a wideband limiter/demodulator and an active lowpass filter.

The SAW filter has a center frequency of 110.592 MHz. The bandwidth of the filter is important, as the wanted signal should pass through without too much attenuation and distortion while the adjacent channels should be suppressed.

C109,C107,C108, L104, L105 performs the matching of the SAW filter to the LMX 3162. These values gives a good compromise between signal distortion and good adjacent channel suppression.

C111 and R106 is inserted to give around 8 dB of attenuation between the IF amplifier and the limiter. This is to obtain a linear RSSI curve.

To avoid instability the decoupling of the power supply is critical. This should be taken into consideration during layout.

The quadrature tank circuit consists of L108,C115,C134,D10. The tank circuit is tuned by the varicap D10. The control voltage to the varicap is a DAC output signal that is filtered in the RC lowpass filter consisting of R25, C47, R45 and C51.

The output level from the demodulator has an amplitude of approximately 500 $mV_{pp.}$ When no DC offset is programmed into the LMX the optimum voltage of the demodulator output is 1.5 – 1.7V. An DC offset in steps of 0.125V can be programmed via the microwire bus.

After the demodulator the signal is filtered in an active lowpass filter. This filter rejects some of the wideband noise from the demodulator and suppresses the adjacent channels. The filter makes the eye opening smaller but the filter design is compromise between not distorting the signal and suppressing the noise and interference. An important parameter for the filter is the group delay ripple. To have a good bit clock recovery the group delay ripple should be small compared to the bit time. This filter has a group delay ripple of approx. 40ns in the 0-600 kHz. The 3-dB frequency of the filter is approx. 600 kHz.

8 Data Slicer

The analog output signal from the lowpass filter is transformed into a digital signal in the comparator in the BMC. The reference value for the comparator is found using different approaches in the base and handset. In the handset the reference signal (CMPREF) is generated using a DAC on the BMC. The value for the DAC is found from the duty cycle of the received signal.

In the base a sample and hold circuit is used. The output signal from the lowpass filter is filtered further in a RC network (R11, C24). After the filter there is a buffer amplifier and a switch. After the switch, there is a hold capacitor C 121. The received signal is sampled during the first 16 bits of the preamble which contains a 010101 sequence. After the preamble the switch is opened and the CMPREF signal is held on C121. The component values is chosen as a compromise between a fast acquisition time and a good suppression of the ripple of the CMPREF signal.