APPENDIX 4

PLL DATA SHEETS

FROM: MR. Mok Total: 12 pages.

SANYO No. 4797A

CMOS LSI

LC72322

Single-Chip Microcontroller with PLL and LCD Driver

Overview

The LC72322 is a single-chip microcontroller for use in electronic tuning applications. It includes on chip both LCD drivers and a PLL circuit that can operate at up to 150 MHz. It features a large-capacity ROM, a highly efficient instruction set, and powerful hardware.

Functions

- Stack: Eight levels
- Fast programmable divider
- General-purpose counters: HCTR for frequency measurement and LCTR for frequency or period measurement
- LCD driver for displays with up to 56 segments (1/2 duty, 1/2 bias)
- Program memory (ROM): 4 k words by 16 bits
- Data memory (RAM): 256 4-bit digits
- All instructions are single-word instructions
- Cycle time: 2.67 µs, 13.33 µs, or 40.00 µs (option)
- Unlock FF: 0.55 µs detection, 1.1 µs detection
- Timer FF: 1 ms, 5ms, 25ms, 125ms
- Input ports*: One dedicated key input port and one high-breakdown voltage port
- Output ports*: Two dedicated key output ports, one high-breakdown voltage open-drain port
  Two CMOS output ports (of which one can be switched to be used as LCD driver outputs)
  Seven CMOS output ports (mask option switchable to use as LCD ports)
- I/O ports*: One switchable between input and output in four-bit units and one switchable between input and output in one-bit units

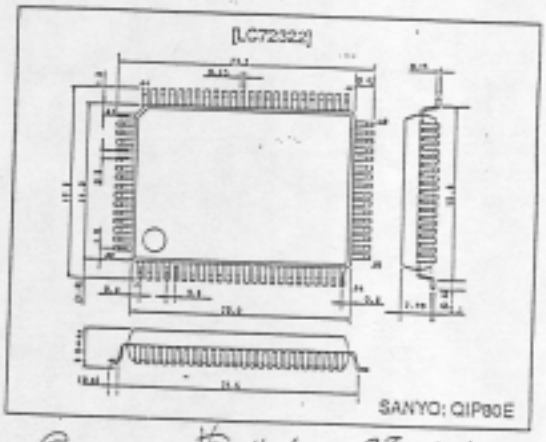
Note: * Each port consists of four bits.

- Program runaway can be detected and a special address set (Programmable watchdog timer).
- Voltage detection type reset circuit
- One 6-bit A/D converter
- Two 8-bit D/A converters (PWM)
- One external interrupt
- Hold mode for RAM backup
- Sense FF for hot/cold startup determination
- PLL: 4.5 to 5.5 V
- CPU: 3.5 to 5.5 V
- RAM: 1.3 to 5.5 V

Package Dimensions

unit: mm

3174-QFP80E



SANYO 莫先生, 孫小姐
TEL: 2311 1198

Doh
June 22, 1998.

June 23, 1998.

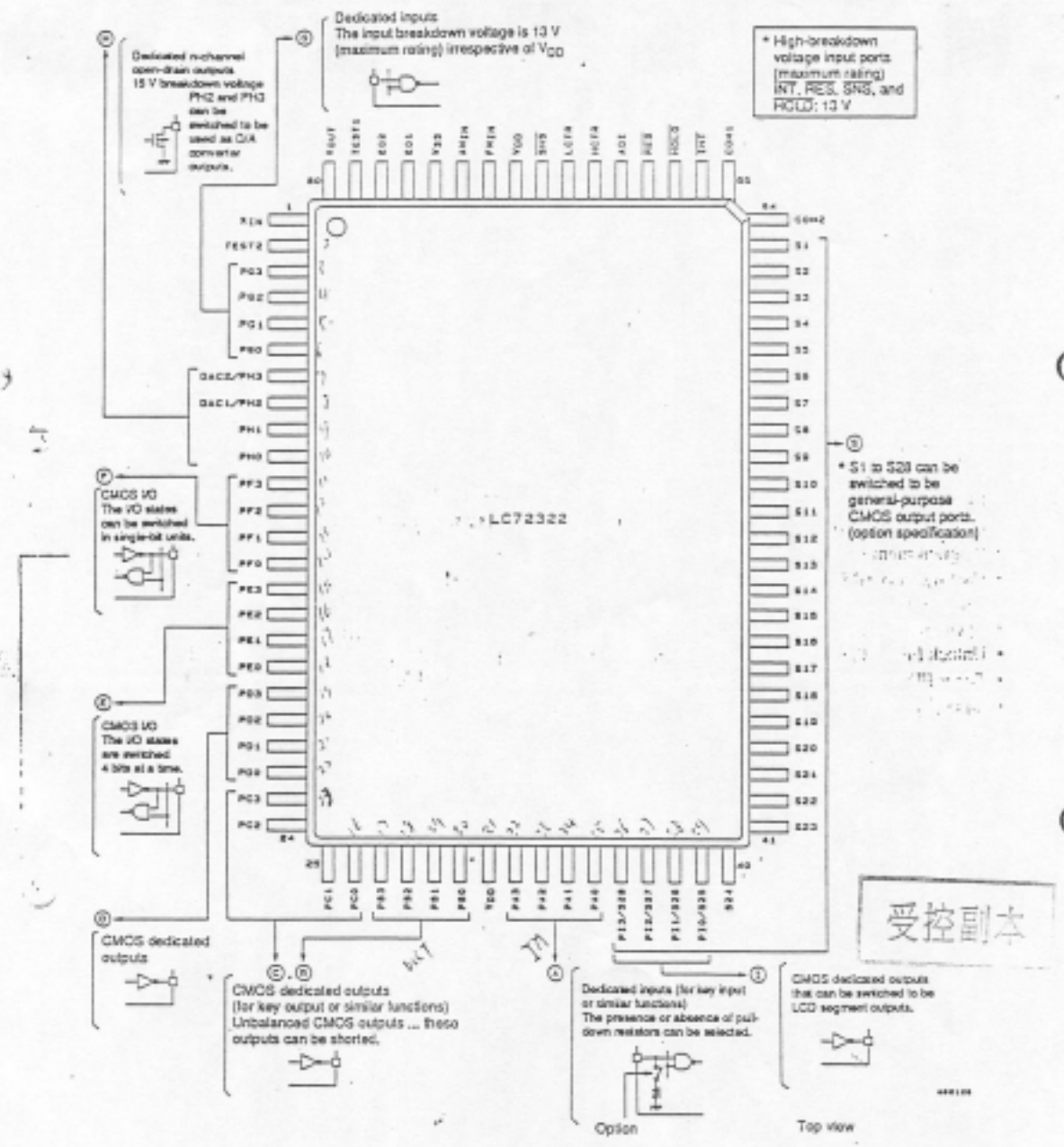
This LSI can easily use CCB that is SANYO's original bus format.

CCB

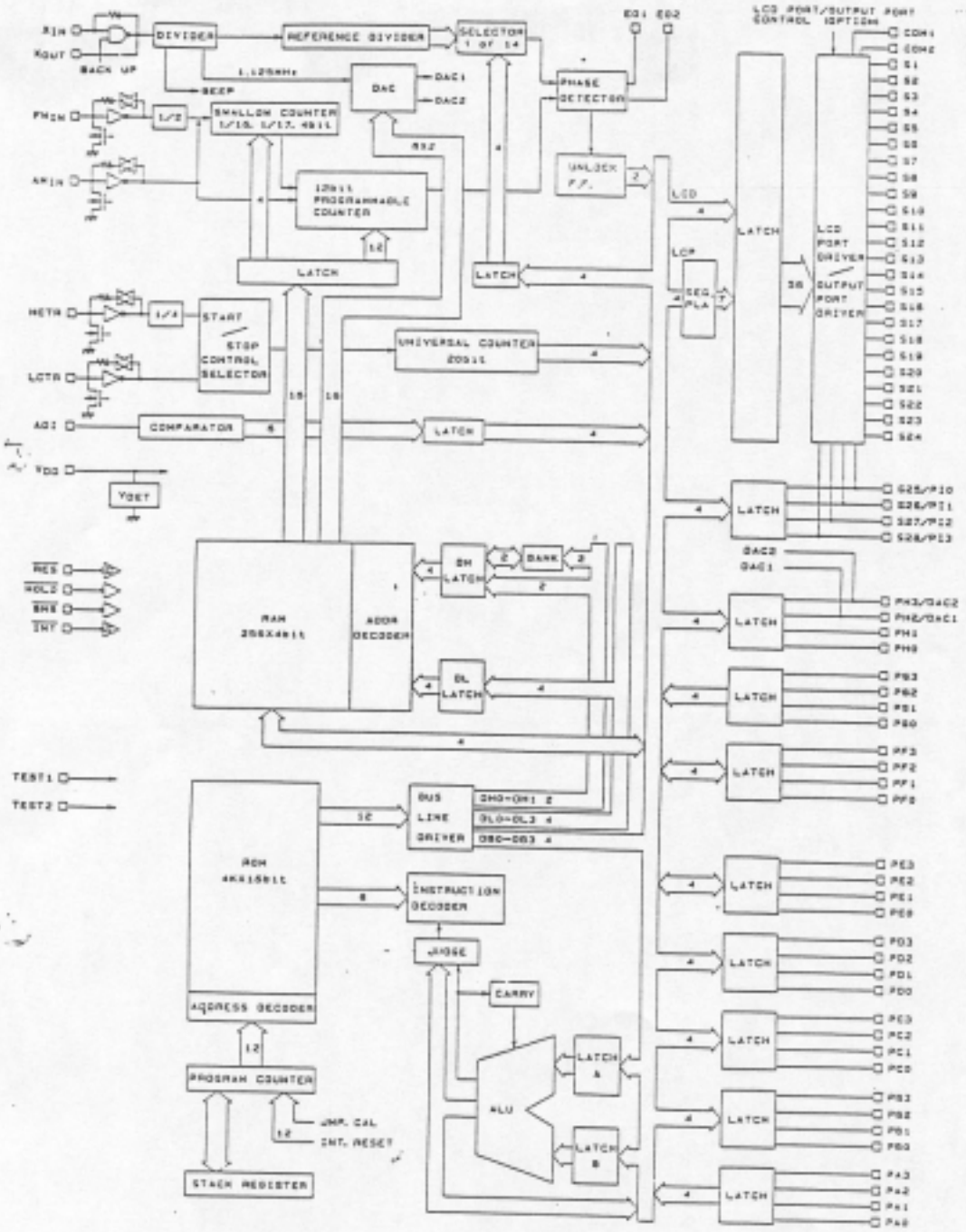
- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus

SANYO Electric Co., Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

Pin Assignment



Block Diagram



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		−0.3 to +6.5	V
Input voltage	$V_{IN}1$	HOLD, INT, RES, ADI, SNS, and the G port	−0.3 to +13	V
	$V_{IN}2$	Inputs other than $V_{IN}1$	−0.3 to V_{DD} + 0.3	V
Output voltage	$V_{OUT}1$	H port	−0.3 to +15	V
	$V_{OUT}2$	Outputs other than $V_{OUT}1$	−0.3 to V_{DD} + 0.3	V
Output current	$I_{OUT}1$	All D and H port pins	0 to 5	mA
	$I_{OUT}2$	All E and F port pins	0 to 3	mA
	$I_{OUT}3$	All B and C port pins	0 to 1	mA
	$I_{OUT}4$	S1 to S28 and all I port pins	0 to 1	mA
Allowable power dissipation	Pd max	Ta = −40 to +85°C	300	mW
Operating temperature	Topr		−40 to +85	°C
Storage temperature	Tstg		−45 to +125	°C

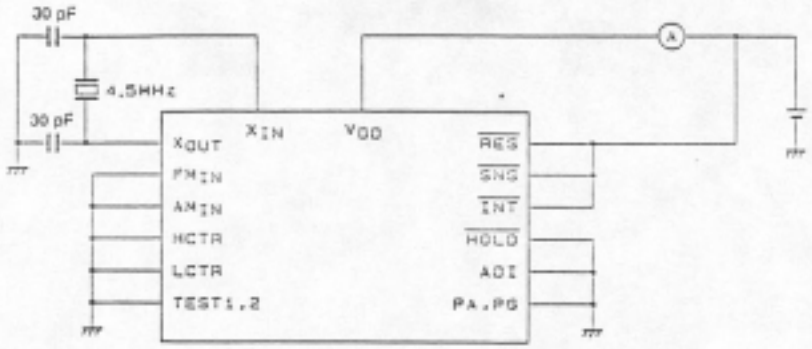
Allowable Operating Ranges at Ta = −40 to +85°C, V_{DD} = 3.5 to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}1$	CPU and PLL operating	4.5		5.5	V
	$V_{DD}2$	CPU operating	3.5		5.5	V
	$V_{DD}3$	Memory retention voltage	1.3		5.5	V
Input high level voltage	$V_{IH}1$	G port	0.7 V_{DD}		8.0	V
	$V_{IH}2$	$\overline{RES}$, $\overline{INT}$, $\overline{HOLD}$	0.8 V_{DD}		8.0	V
	$V_{IH}3$	$\overline{SNS}$	2.5		8.0	V
	$V_{IH}4$	A port	0.8 V_{DD}		V_{DD}	V
	$V_{IH}5$	E, F port	0.7 V_{DD}		V_{DD}	V
	$V_{IH}6$	LCTR (period measurement), $V_{DD}1$, PE1, PE3	0.8 V_{DD}		V_{DD}	V
Input low level voltage	$V_{IL}1$	G port	0		0.3 V_{DD}	V
	$V_{IL}2$	$\overline{RES}$, $\overline{INT}$, PE1, PE3	0		0.2 V_{DD}	V
	$V_{IL}3$	$\overline{SNS}$	0		1.3	V
	$V_{IL}4$	A port	0		0.2 V_{DD}	V
	$V_{IL}5$	PE0, PE2, F port	0		0.3 V_{DD}	V
	$V_{IL}6$	LCTR (period measurement), $V_{DD}1$	0		0.2 V_{DD}	V
	$V_{IL}7$	$\overline{HOLD}$	0		0.4 V_{DD}	V
Input frequency	$f_{IN}1$	XIN	4.0	4.5	5.0	MHz
	$f_{IN}2$	FMIN, $V_{IN}2$, $V_{DD}1$	10		130	MHz
	$f_{IN}3$	FMIN, $V_{IN}3$, $V_{DD}1$	10		150	MHz
	$f_{IN}4$	AMIN (L), $V_{IN}4$, $V_{DD}1$	0.5		10	MHz
	$f_{IN}5$	AMIN (H), $V_{IN}5$, $V_{DD}1$	2.0		40	MHz
	$f_{IN}6$	HCTR, $V_{IN}6$, $V_{DD}1$	0.4		12	MHz
	$f_{IN}7$	LCTR (frequency), $V_{IN}7$, $V_{DD}1$	100		500	kHz
	$f_{IN}8$	LCTR (frequency), $V_{IN}6$, $V_{IL}6$, $V_{DD}1$	1		20×10^3	Hz
Input amplitude	$V_{IN}1$	XIN	0.50		1.5	Vrms
	$V_{IN}2$	FMIN	0.10		1.5	Vrms
	$V_{IN}3$	FMIN	0.15		1.5	Vrms
	$V_{IN}4, 5$	AMIN	0.10		1.5	Vrms
	$V_{IN}6, 7$	LCTR, HCTR	0.10		1.5	Vrms
Input voltage range	$V_{IN}3$	ADI	0		V_{DD}	V

Electrical Characteristics for the Allowable Operating Ranges

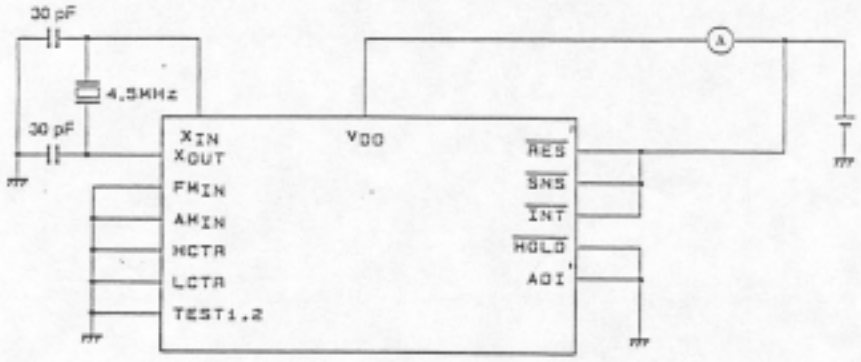
Parameter	Symbol	Conditions	Ratings min	Ratings typ	Ratings max	Unit
Hysteresis	V_H	LCTR (period), $\overline{RES}$, $\overline{INT}$, PE1, PE3	0.1 V_{DD}			V
Rejected pulse width	P_{REJ}	$\overline{SNS}$			50	µs
Power-down detection voltage	V_{DET}		2.7	3.0	3.3	V
Input high level current	$I_{IH}1$	$\overline{INT}$, $\overline{HOLD}$, $\overline{RES}$, ADI, $\overline{SNS}$, and the G port: V_I = 5.5 V			3.0	µA
	$I_{IH}2$	A, E, and F ports: E and F ports with outputs off, A port with no R_{PD}, $V_I = V_{DD}$			3.0	µA
	$I_{IH}3$	XIN: $V_I = V_{DD}$ = 5.0 V	2.0	5.0	15	µA
	$I_{IH}4$	FMIN, AMIN, HCTR, LCTR: $V_I = V_{DD}$ = 5.0 V	4.0	10	30	µA
	$I_{IH}5$	A port: With an R_{PD}, $V_I = V_{DD}$ = 5.0 V		50		µA
Input low level current	$I_{IL}1$	$\overline{INT}$, $\overline{HOLD}$, $\overline{RES}$, ADI, $\overline{SNS}$, and the G port: $V_I = V_{SS}$			3.0	µA
	$I_{IL}2$	A, E, and F ports: E and F ports with outputs off, A port with no R_{PD}, $V_I = V_{SS}$			3.0	µA
	$I_{IL}3$	XIN: $V_{IN} = V_{SS}$	2.0	5.0	15	µA
	$I_{IL}4$	FMIN, AMIN, HCTR, LCTR: $V_I = V_{SS}$	4.0	10	30	µA
Input floating voltage	V_{IF}	A port: With an R_{PD}			0.05 V_{DD}	V
Pull-down resistance	R_{PD}	A port: With an R_{PD}, V_{DD} = 5.0 V	75	100	200	kΩ
Output high level off leakage current	$I_{OFFH}1$	EO1, EO2: $V_O = V_{DD}$		0.01	10	nA
	$I_{OFFH}2$	B, C, D, E, F, and I ports: $V_O = V_{DD}$			3.0	µA
	$I_{OFFH}3$	H port: V_O = 13 V			5.0	µA
Output low level off leakage current	$I_{OFFL}1$	EO1, EO2: $V_O = V_{SS}$		0.01	10	nA
	$I_{OFFL}2$	B, C, D, E, F, and I ports: $V_O = V_{SS}$			3.0	µA
Output high level voltage	$V_{OH}1$	B and C ports: I_O = 1 mA	V_{DD} – 2.0	V_{DD} – 1.0	V_{DD} – 0.5	V
	$V_{OH}2$	E and F ports: I_O = 1 mA	V_{DD} – 1.0			V
	$V_{OH}3$	EO1, EO2: I_O = 500 µA	V_{DD} – 1.0			V
	$V_{OH}4$	XOUT: I_O = 200 µA	V_{DD} – 1.0			V
	$V_{OH}5$	S1 to S28 and the I port: I_O = –0.1 mA	V_{DD} – 1.0			V
	$V_{OH}6$	D port: I_O = 5 mA	V_{DD} – 1.0			V
	$V_{OH}7$	COM1, COM2: I_O = 25 µA	V_{DD} – 0.75	V_{DD} – 0.5	V_{DD} – 0.3	V
Output low level voltage	$V_{OL}1$	B and C ports: I_O = 50 µA	0.5	1.0	2.0	V
	$V_{OL}2$	E and F ports: I_O = 1 mA			1.0	V
	$V_{OL}3$	EO1, EO2: I_O = 500 µA			1.0	V
	$V_{OL}4$	XOUT: I_O = 200 µA			1.0	V
	$V_{OL}5$	S1 to S28 and the I port: I_O = 0.1 mA			1.0	V
	$V_{OL}6$	D port: I_O = 5 mA			1.0	V
	$V_{OL}7$	COM1, COM2: I_O = 25 µA	– 0.3	0.5	0.75	V
	$V_{OL}8$	H port: I_O = 5 mA, $V_{DD}1$	(150 Ω) 0.75		(400 Ω) 2.0	V
Output middle level voltage	V_M1	COM1, COM2: V_{DD} = 5.0 V, I_O = 25 µA	2.0	2.5	3.0	V
A/D conversion error		ADI: $V_{DD}1$	–1/2		1/2	LSB
Current drain	$I_{DD}1$	$V_{DD}1$, $f_{IN}2$ = 130 MHz		15	20	mA
	$I_{DD}2$	$V_{DD}1$, PLL stopped, CT = 2.67 µs (HOLD mode, Figure 1)		1.5		mA
	$I_{DD}3$	$V_{DD}1$, PLL stopped, CT = 13.33 µs (HOLD mode, Figure 1)		1.0		mA
	$I_{DD}4$	$V_{DD}1$, PLL stopped, CT = 40.00 µs (HOLD mode, Figure 1)		0.7		mA
	$I_{DD}5$	V_{DD} = 5.5 V, oscillator stopped, Ta = 25°C (BACK UP mode, Figure 2)			5	µA
		V_{DD} = 2.5 V, oscillator stopped, Ta = 25°C (BACK UP mode, Figure 2)			1	µA

Test Circuits



Note: PB to PF, PH, and PI are all open. However, PE and PF are output selected.

Figure 1 $I_{DD}2$ to $I_{DD}4$ in HOLD Mode



Note: PA to PI, S1 to S4, COM1, and COM2 are all open.

Figure 2 $I_{DD}5$ In BACK UP Mode

COPY OF PLL DATA SHEETS
FCC ID: BBO75WXSTA
APPENDIX 4