BTR-800 Operational Description

A. General

This product contains two identical transmitters operating simultaneously on different frequencies and modulated by two different audio signals. The carriers are combined to feed a single antenna. In the following text the A channel will be described and the corresponding B channel component designator will be in parentheses.

B. Mixer

Audio from various inputs arrive at the transmit mixer U22A (U44A) where they are summed into one signal.

C. Modulation Limiter

U23A (U45A) is configured as a variable gain amplifier and U24 (U46) is configured as a window detector. When the audio fed into U24 (U46) exceeds the preset threshold, U24A (U46A) pulls low on negative peaks and U24B (U46B) pulls low on positive peaks. This discharges C48 (C118) and reduces the gain of U23A (U45A) until the input to U24 (U46) is just at the threshold of limiting.

D. Compressor

U23C (U45C) is a linear compressor that is used to improve the system signal to noise ratio. A complementary expander is used at the receiver.

E. Pre-emphasis

U23B (U45B) provides pre-emphasis which begins at 100 microseconds and ends at 15 microseconds. The output of U23B (U45B) feeds the modulation limiter.

F. Low Pass Filter

U23D (U45D) is a 3 pole low pass filter with a cutoff frequency of 10 kHz.

G. PLL

HY801 (HY802) is a VCO operating on the output frequency. U802 (U803) is a phase locked loop that controls HY801 (HY802). U802 and U803 are serially loaded with frequency data by U9??. The modulating signal is fed into the loop via VR801 (VR802), which is used to set the frequency deviation.

H. Output Amplifiers

Q802, Q803, Q807 and Q809 (Q811, Q812, Q816 and Q818) amplify the signal from HY801 (HY802) and provide reverse isolation. Q806 (Q815) is used to turn these stages on only after the loop has achieved lock. C831, C832, C833, L809 and L810 (C865, C866, C867, L819 and L820) provide impedance matching and harmonic suppression.

I. Combiner

U1001 and U1002 amplify and isolate the two carriers which are then combined by T1001. The combiner is kept off until both PLL's achieve lock. Additional harmonic suppression is provided by C1006, C1007 and L1001.

BTR-800 Receiver, Operational Description.
Preliminary Information
12-13-00
Rev PB

The BTR-800 Receiver is a component of the BTR800 Transmitter/ Receiver combination. The receiver is used to receive transmissions From four TR-800 Portables associated with the system.

Frequency range for the system is 518-608 and 614-746 MHz. Selected bands, 18 MHz wide, within the above range are used to form Base Transmit and Base Receive frequencies for four full duplex systems.

Signals from the antenna system are routed to connector J1.
The receiver front end consists of 3 pre-tuned ceramic resonators (Z301,302 and 303) to provide selectivity against out of band interference to RF Amplifier U301. Selectivity following U301 is provided by Z304 and Z305. The signal then flows to the 1st mixer U303. Also flowing to the mixer is the LO signal.

Transistor Q301 Along with Crystal Y1 oscillates at 1/6 th of the LO frequency and The Q301 signal is fed to Q302 through C48. Q302 operates as a Frequency tripler and the 3rd harmonic of Y1 is tuned by VC306, L305, L306 and VC307 combination. The third harmonic is then routed to Q303 where the frequency is doubled. The LO signal is then tuned byVC308, L307, VC306 and L308 combination. The 1st LO signal then flows through C317 to the mixer IC U303.

The RF and LO signals are mixed in U303 and are converted to IF signals Within a 65 to 83 MHz IF range. The IF signals are then routed to the 1st IF broadband pre-amplifier Q304. T301 and the combination of L309, 310 and 311 form a broadband filter ahead of Q304. The IF signals are then fed to splitter transformer T302, T303 and T304 Where the IF signals are split four ways and are routed to individual IF strips where each signal is filtered out and processed into audio.

The entire front end assembly can be considered a down converter and Is used to set the band of frequencies received but not individual frequencies. The frequency of the LO is determined by adding 83 MHz to the high end of the desired 18 MHz wide band. (high side injection). Example: Desired band is 482 to 500 MHz. 500 + 83 =583 MHz=LO. Y301 then = LO/6 = 583/6 = 97.16666 MHz. Individual frequencies will be determined later.

For this paper, only one IF strip will be described. The remaining three operate the same except for the 1st IF frequency, which is variable. IF signals enter the IF strip through C401 and are filtered by the combination of L403, 404 and C407/408 befor entering 1st IF amplifier U401. The signals are amplified by U401 and applied to another filter combination L409, 410 and C422/423. These filter combinations are switched to one of four IF bands, depending on the IF frequency chosen. This 1st IF signal is then fed to the 2nd mixer U403 where it is mixed with the 2nd LO.

The 2nd LO is generated by Q403 which is phase locked to the reference oscillator. U402 is the PLL circuit. The LO signal is buffered by Q404 and flows to the 2nd mixer through C453 and C462. The 2nd LO and the 2nd IF are then mixed in U403 to form the 2nd IF signal on 10.7 MHz. The second LO signal is always 10.7 MHz above the 1st IF. The 10.7 MHz signal then flows through T401, FL401, Q405, FL402, Q408, U404A and FL403 to the Limiter/Detector IC U404B. The filtered and amplified signal is then limited by U404B, then detected as an FM signal by a quadrature detector tuned by L418. The audio signal appears at U404B-6 and flows through amplifier U405 and gate U406.
Squelch signals appear at U404B-7 and are fed through Q406 to Q407 where amplified noise is frequency selected by C485/L419 combination. The noise is rectified by D412 and is applied to squelch comparator U407 and the internal squelch level is set by VR401. The U407 squelch signal then controls the audio output through gate U406. RSSI signals are available from U404B-5.
U304/Q401/402 control the band 1st IF band selection signals from the processor.

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